8V19N490

Phase Deterministic Procedure – Sysref Internal Trigger

Abstract

This document provides a register write sequence for the 8V19N490 phase deterministic on each power-up. The 8V19N490 can be QCLK to QCLK phase deterministic and Sysref to QCLK phase deterministic. The Sysref can be either an internal or external trigger. The procedure for the internal trigger is provided in this document. The 8V19N490 Sysref general procedure steps are provided then followed by an example.

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1. General Register Write Sequence Steps

For phase deterministic between the QCLKx, follow Steps 1 and 2 after power-on. For phase deterministic between QCLKx and Sysref, follow Steps 1, 2, and 3 after power-on.

1. **(**After this step, you should see a QCLKx output signal. The QCLKx phase is not aligned. Sysref output is not active.)
   Load general data for required information such as I/O frequencies, Feedback Divider, and Icp. The data can be dumped from 0x00 to 0x76 with the bits that are set as follows:
   a. For example: Sysref Pulse generator set to Internal Trigger, SRG = 0, (R0x1C, D1 = 0), and Continuous mode SRO = 1, (R0x1C, D0 = 1)
   b. FVCV = 0, VCXO Normal operation, (R0X10 D6 = 0)
   c. INIT_CLK = 1 (R0x71, D7 = 0)
   d. RELOCK = 1 (R0x72, D7 = 0)
   e. PB_CAL = 1 (R0x73, D7 = 1)
   f. Sysref Pulse Initiate, RS = 0 (Register 0x70h, D7 = 0)
   g. nBIAS_r = 0 (Registers, 0x2C, 0x2D, 0x2E, 0x3C, 0x3D, 0x4C, 0x4D, 0x5C Bit D5 = 0)
2. (This step should phase align the QCLKx outputs. Sysref is not active.)
   Initialization by writing a 1 to the following bits, these bits are self cleared.
   a. INIT_CLK = 1 (R0x71, D7 = 1)
   b. RELOCK = 1 (R0x72, D7 = 1)
3. (This step should generate the Sysref signal.) Write SysRef Pulse Initiate, RS = 1 (Register 0x70h, D7 = 1), this bit is self cleared.

2. Program Sequence Register Example

1. General I/O Configuration for data loading. The data can vary depending on the application.

The gray shaded areas in Table 1 are key required settings for Step 1. The reserved registers can be skipped.

Table 1. General I/O Configuration Data

Register Address (Decimal)	Register Address (HEX)	Register Data (HEX)	Register Data (Binary)	Descriptions
0	0	C4	11000100	
1	1	0	00000000	
2	2	0	00000000	
3	3	0	00000000	
4	4	80	10000000	
5	5	80	10000000	
6	6	0	00000000	
7	7	0	00000000	
8	8	0	00000000	

Register Address (Decimal)	Register Address (HEX)	Register Data (HEX)	Register Data (Binary)	Descriptions
9	9	10	00010000	
10	A	0	00000000	
11	B	0	00000000	
12	C	0	00000000	
13	D	0	00000000	
14	E	0	00000000	
15	F	0	00000000	
16	10	5	00000101	
17	11	0	00000000	
18	12	42	01000010	
19	13	0	00000000	
20	14	0	00000000	
21	15	0	00000000	
22	16	0	00000000	
23	17	0	00000000	
24	18	75	01110101	
25	19	62	01100010	
26	1A	0	00000000	
27	1B	0	00000000	
28	1C	0	00000000	D1 = SRG = 0, Internal Trigger D0 = SRO = 0, Continuous
29	1D	0	00000000	
30	1E	0	00000000	
31	1F	0	00000000	
32	20	36	00110110	
33	21	0	00000000	
34	22	0	00000000	
35	23	0	00000000	
36	24	6	00000110	

Register Address (Decimal)	Register Address (HEX)	Register Data (HEX)	Register Data (Binary)	Descriptions
37	25	0	00000000	
38	26	0	00000000	
39	27	0	00000000	
40	28	36	00110110	
41	29	0	00000000	
42	2A	0	00000000	
43	2B	0	00000000	
44	2C	6	00000110	PD = D7 = 0, nBIAS_r = D5 = 0
45	2D	0	00000000	PD = D7 = 0, nBIAS_r = D5 = 0
46	2E	0	00000000	PD = D7 = 0, nBIAS_r = D5 = 0
47	2F	0	00000000	PD = D7 = 0, nBIAS_r = D5 = 0
48	30	22	00100010	
49	31	0	00000000	
50	32	0	00000000	
51	33	0	00000000	
52	34	6	00000110	
53	35	0	00000000	
54	36	0	00000000	
55	37	0	00000000	
56	38	12	00010010	
57	39	0	00000000	
58	3A	0	00000000	
59	3B	0	00000000	
60	3C	6	00000110	PD = D7 = 0, nBIAS_r = D5 = 0
61	3D	0	00000000	PD = D7 = 0, nBIAS_r = D5 = 0
62	3E	0	00000000	
63	3F	0	00000000	
64	40	16	00010110	
65	41	0	00000000	

Register Address (Decimal)	Register Address (HEX)	Register Data (HEX)	Register Data (Binary)	Descriptions
66	42	0	00000000	
67	43	0	00000000	
68	44	6	00000110	
69	45	0	00000000	
70	46	0	00000000	
71	47	0	00000000	
72	48	16	00010110	
73	49	0	00000000	
74	4A	0	00000000	
75	4B	0	00000000	
76	4C	6	00000110	PD = D7 = 0, nBIAS_r = D5 = 0
77	4D	0	00000000	PD = D7 = 0, nBIAS_r = D5 = 0
78	4E	0	00000000	
79	4F	0	00000000	
80	50	30	00110000	
81	51	0	00000000	
82	52	0	00000000	
83	53	0	00000000	
84	54	6	00000110	
85	55	0	00000000	
86	56	0	00000000	
87	57	0	00000000	
88	58	6	00000110	
89	59	0	00000000	
90	5A	0	00000000	
91	5B	0	00000000	
92	5C	6	00000110	PD = D7 = 0, nBIAS_r = D5 = 0
93	5D	0	00000000	
94	5E	0	00000000	

Register Address (Decimal)	Register Address (HEX)	Register Data (HEX)	Register Data (Binary)	Descriptions
95	5F	0	00000000	
96	60	0	00000000	
97	61	0	00000000	
98	62	0	00000000	
99	63	0	00000000	
100	64	0	00000000	
101	65	0	00000000	
102	66	0	00000000	
103	67	0	00000000	
104	68	0	00000000	
105	69	0	00000000	
106	6A	1F	00011111	
107	6B	27	00100111	
108	6C	38	00111000	
109	6D	38	00111000	
110	6E	0	00000000	
111	6F	20	00100000	
112	70	0	00000000	D7 = RS = 0
113	71	0	00000000	D7 = INIT_CLK = 0
114	72	0	00000000	D7 = RELOCK = 0
115	73	80	10000000	D7 = PB_CAL = 1
116	74	FF	11111111	
117	75	0	00000000	
118	76	FF	11111111	Enable the QREF_r outputs

2. Initialize.

Table 2. Registers 113 and 114 Initialization Information

Register Address (Decimal)	Register Address (HEX)	Register Data (HEX)	Register Data (Binary)	Descriptions
113	71	80	10000000	D7 = INIT_CLK = 1
114	72	80	10000000	D7 = RELOCK = 1

3. Activate Sysref.

Table 3. Register 112 Sysref Activation

Register Address (Decimal)	Register Address (HEX)	Register Data (HEX)	Register Data (Binary)	Descriptions
112	70	80	10000000	D7 = RS = 1

3. Revision History

Revision Date	Description of Change
Oct.29.20	Initial release.

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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

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