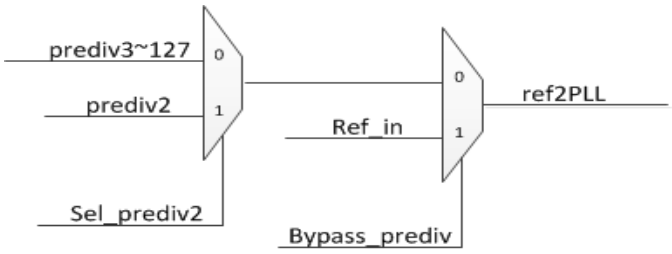
Introduction

This application note details the calculations required to set the registers of the IDT5P49V5901. For the device pin out, block diagram, I2C interface, power up sequence, OTP programming and register map, please consult the IDT document *VersaClock 5® - 5P49V5901 Programming Guide*.

PLL Pre-Divider Options

The reference presented to the fractional PLL can be either directly connected, divided by two or divided by the any value from the range of three to 127 as set in the register Ref_Div[6:0]. The phase detector of the PLL has a maximum frequency of 50 MHz, therefore the default is to bypass the pre-divider by setting Bypss_prediv = 1. For the functionality of Sel_prediv2 and bypss_prediv bits, see Figure 1.

Figure 1. PLL Pre-Divider Options



PLL Fractional Feedback Divider

The PLL feedback divider M is composed of a 12 bit integer portion, FB_intdiv[11:0] and a 24 bit fractional portion, FB_frcdiv[23:0].

$$M = INT(M) + FRAC(M) = \frac{F_{VCO}}{F_{REF2PLL}} \quad (1)$$

Convert FRAC(M) to hex with Eq.2 where ROUND2INT means to round to the nearest integer. The round-off error of M in ppm is the VCO frequency error in ppm.

$$\text{FB\_frcdiv}[23:0] = DEC2HEX(ROUND2INT[2^{24} * FRAC(M)]) \quad (2)$$

Fractional Output Dividers and Spread Spectrum

Spread spectrum capability is contained within the Fractional-N output dividers associated with each output clock. When applied, triangle wave modulation of any spread spectrum amount, $SS\%_{AMT}$, from ±0.25% to ±2.5% center spread and -0.5% to -5% down spread between 30 and 63kHz may be generated, independent of the output clock frequency. Five variables define Spread Spectrum in FODx (see Table 1).

Table 1: Spread Spectrum Variables in FODx

Name	Function	Register Length	Note
ODx_sscex	Spread spectrum control enable	1	If ODx_sscex = 0, contents of ODx_period and ODx_step are Don't Care.
ODx_intdiv	Integer portion of the FODx divider, N	12	
ODx_period	Spread spectrum modulation period	13	Defined as half the reciprocal of the modulation frequency and measured in cycles of the FODx output frequency. See Eq 5 below.
ODx_step	Modulation step size	24	Sets the time rate of change or time slope of the output clock frequency
ODx_offset	Spread spectrum modulation offset, which defines down spread or center spread	30	ODx_offset is the actual spread spectrum offset subtracted from the Fractional portion of the FODx divider N. It is the fractional portion of the FODx divider and accounts for the fact that there is no ODx_frcdiv in the memory map.

To calculate the spread spectrum registers, first determine the value in decimal of the FOD output divider, N, for the nominal output frequency without spread spectrum. The VCO frequency is divided by two to account for a fixed divide by 2 between the VCO output and the input to the FOD. Convert the integer portion into hex to define ODx_intdiv.

$$N(dec) = INT(N) + FRAC(N) = \frac{\left(F_{VCO}/_2\right)}{F_{OUT}} \quad (3)$$

$$\text{ODx\_intdiv}[11:0] = \text{DEC2HEX}(\text{INT}(\text{N})) \quad (4)$$

If no spread is to be applied to FODx (ODx_sscex =0) then ODx_period and ODx_step registers are Don't Care and it is permissible to skip to Eq. 9. Convert FRAC(N) to 30 bits in accordance with Eq. 10.

When the ODx_period and ODx_step registers are calculated below, ODx_period and ODx_step are explicitly set to 0 if ODx_sscex will always be 0. This is done for reasons of style, it reinforces the fact that there is no spread spectrum invoked when ODx_sscex =0. If down spread is to be turned on by just setting ODx_sscex =1, then ODx_period and ODx_step must be calculated and registered. See Eq. 9 to see why changing only ODx_ssce works only for down spread.

Consider one cycle of down spread triangular modulation; the output divider, N, is ramped up linearly from the non-spread value of N followed by a linear ramp back down to the non-spread value of N. N is always greater than or equal to the non-spread value of N, therefore the output frequency is always less than or equal to the non-spread frequency.

As normally defined, ODx_period (dec) would be 1/ F_{SS}, but the modulation period is defined instead as ½*1/ F_{SS} for the most direct calculation of ODx_step as will be seen below. An added benefit is that the up ramp and the down ramp are guaranteed to be symmetric. Note that ODx_period does not have units of time; it is the dimensionless number of F_{OUT} periods that fit in a half period of F_{SS}.

$$\text{ODx\_period(dec)} = \begin{Bmatrix} 0 & if\ ssce = 0 \\ \frac{1}{2} * \frac{F_{OUT}}{F_{SS}} & if\ ssce = 1 \end{Bmatrix} \quad (5)$$

$$\text{ODx\_period}[12:0] = \text{DEC2HEX(ROUND2INT(ODx\_period(dec)))} \quad (6)$$

Calculate the step size.

$$\text{ODx\_step(dec)} = \begin{Bmatrix} 0 & if\ \text{ssce} = 0 \\ \dfrac{SS_{\%AMT}/100 * N}{\text{ODx\_period}} & if\ \text{ssce} = 1 \end{Bmatrix} \quad (7)$$

$$\text{ODx\_step}[23:0] = \text{DEC2HEX}(\text{ROUND2INT}(2^{24} * \text{ODx\_step(dec)})) \quad (8)$$

Since the spread spectrum ramp as implemented only decreases the frequency of FOUT, then the actual offset for down spread is zero. But if the spread is to be centered, an offset equal to half the peak modulation, SS%AMT *N, is to be subtracted from the value of FRAC(N).

$$ODx\text{\_offset(dec)} = \begin{Bmatrix} FRAC(N) & if\ \text{ssce} = 0\ or\ Down\ spread \\ FRAC(N) - \dfrac{SS_{\%AMT}/100 * N}{2} & if\ \text{ssce} = 1\ and\ Center\ spread \end{Bmatrix} \quad (9)$$

$$ODx\text{\_offset}[29:0] = DEC2HEX(ROUND2INT[2^{24} * ODx\text{\_offset(dec)}]) \quad (10)$$

If FRAC(N) is a small positive value, it is possible that after the center spread offset is subtracted ODx_offset will be negative. In this case, retain only the lower 30 bits of the 32 bit hex value and assign them to ODx_offfset[29:0].

In this manner it can be seen that ODx_offset is the value of FRAC(N), appropriately adjusted should center spread be enabled.

Skew

Skew is not implemented with a parallel load of the count of the output divider as is commonly done with non-fractional divides. Instead skew is accomplished by increasing the value of the fractional output divider for only the very first clock cycle. The divide is increased by the number of VCO cycles required to delay the completion of the first output clock cycle by the desired skew. For the second and all subsequent output cycles, hardware changes the output divider to the value for the proper steady state output frequency.

To illustrate, suppose there are two output clocks defined as four cycles of Fvco/2 per FOD output clock cycle, that is N=4. OUT2 is to be delayed by 90 degrees relative to OUT1 and the power on reset phase aligns the output clocks out of reset.

Table 2: OUT1 and OUT2 Clock Cycle Duration Measured in Fvco/2 Cycles

	FOD Cycle 1	FOD Cycle 2	FOD Cycle 3	FOD Cycle n
OUT1	4	4	4	4
OUT2	5	4	4	4

The integer and fractional components of skew are calculated as follows.

$$INT(Skew)(\text{dec}) = INT\left(\left[1 + \frac{Degrees\ of\ Skew}{360}\right] * N\right) - INT(N) \quad (11)$$

$$ODx\_\text{intskew}[11:0] = DEC2HEX\big(INT(Skew)\big) \quad (12)$$

$$FRAC(Skew)(\text{dec}) = \left[1 + \frac{Degrees\ of\ Skew}{360}\right] * N - INT(N) - INT(skew) \quad (13)$$

$$ODx\_\text{frcskew}[5:0] = DEC2HEX(INT[2^6 * FRAC(Skew)]) \quad (14)$$

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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

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