Introduction

This application note will discuss how an IDT transceiver handles T1/E1/J1 signaling, alarms, and errors.

T1/E1/J1 Frame Alignment

A T1 frame consists of 1 frame alignment bit (F-Bit) and 192 payload bits (24 time slot x 8 bit/time slot). SF and ESF are the two commonly used frames. In some systems, SLC-96 frame is used. T1 DM is rarely inquired among customers.

SF frame, also called D4 frame, or F12 frame, consists of 12 “basic” 193-bit frames. Its frame structure is shown Table 1.

Table 1: Structure of SF Frame

Frame Index	F-Bit		Bits Utilization of Time Slot	
	Ft	Fs	Data Bits	Signaling Bit
1	1		1–8	–
2		0	1–8	–
3	0		1–8	–
4		0	1–8	–
5	1		1–8	–
6		1	1–7	A (Bit 8, LSB
7	0		1–8	–
8		1	1–8	–
9	1		1–8	–
10		1	1–8	–
11	0		1–8	–
12		X	1–7	B (Bit 8, LSB)

Note: **Ft**–Terminal frame bit; **Fs**–Signaling framing bit; **X**–0 for T1 and 0 or 1 for J1.

The frame alignment pattern for SF frame is “100011011100” for T1 and “10001101110x’ for J1. The frame synchronization is declared if two consecutive frame alignment patterns are received error free in the data stream without a mimic pattern.

ESF frame consists of 24 basic 193-bit frames. Its frame structure is shown in Table 2.

Table 2: Structure of ESF Frame

Frame Index	F-Bit			Bits Utilization of Time Slot	
	Pattern	Data Link	CRC	Data Bits	Signaling Bit
1		DL		1–8	–
2			C1	1–8	–
3		DL		1–8	–
4	0			1–8	–
5		DL		1–8	–
6			C2	1–7	A (Bit 8, LSB)
7		DL		1–8	–
8	0			1–8	–
9		DL		1–8	–
10			C3	1–8	–
11		DL		1–8	–
12	1			1–7	B (Bit 8, LSB)
13		DL		1–8	–
14			C4	1–8	–
15		DL		1–8	–
16	0			1–8	–
17		DL		1–8	–
18			C5	1–7	C (Bit 8, LSB)
19		DL		1–8	–
20	1			1–8	–
21		DL		1–8	–
22			C6	1–8	–
23		DL		1–8	–
24	1			1–7	D (Bit 8, LSB)

The frame alignment pattern coming from F-bit of Frame 4, 8, 12 and 16 is “001011”. F-bit from Frame 2, 6, 10, 14, 18 and 22 are called CRC bits, which are for error checking. The remaining F-bit are called Data Link bits used for carrying in-band messages for trunk management. The ESF synchronization is acquired if a single correct frame alignment pattern and a single correct CRC-6 based on this correct frame alignment pattern are found.

SLC-96 frame consists of 72 basic 193-bit frames. It is often referred to as an F72 frame because of that. This frame format only applies to T1. Its frame structure is shown in Table 3.

Table 3: Structure of ESF Frame

Frame #	F-Bit (Ft)	Bits Utilization		Frame #	F-Bit (Ft)	Bits Utilization	
		Data Bits	Signaling			Data Bits	Signaling
1	1	1–8	–	2	0	1–8	–
3	0	1–8	–	4	0	1–8	–
5	1	1–8	–	6	1	1–7	A
7	0	1–8	–	8	1	1–8	–
9	1	1–8	–	10	1	1–8	–
11	0	1–8	–	12	0	1–7	B
13	1	1–8	–	14	0	1–8	–
15	0	1–8	–	16	0	1–8	–
17	1	1–8	–	18	1	1–7	C
19	0	1–8	–	20	1	1–8	–
21	1	1–8	–	22	1	1–8	–
23	0	1–8	–	24	C1	1–7	D
25	1	1–8	–	26	C2	1–8	–
27	0	1–8	–	28	C3	1–8	–
29	1	1–8	–	30	C4	1–7	A
31	0	1–8	–	32	C5	1–8	–
33	1	1–8	–	34	C6	1–8	–
35	0	1–8	–	36	C7	1–7	B
37	1	1–8	–	38	C8	1–8	–
39	0	1–8	–	40	C9	1–8	–
41	1	1–8	–	42	C10	1–7	C
43	0	1–8	–	44	C11	1–8	–
45	1	1–8	–	46	SP1 (0)	1–8	–
47	0	1–8	–	48	SP2 (1)	1–7	D
49	1	1–8	–	50	SP3 (0)	1–8	–
51	0	1–8	–	52	M1	1–8	–
53	1	1–8	–	54	M2	1–7	A
55	0	1–8	–	56	M3	1–8	–
57	1	1–8	–	58	A1	1–8	–
59	0	1–8	–	60	A2	1–7	B
61	1	1–8	–	62	S1	1–8	–
63	0	1–8	–	64	S2	1–8	–
65	1	1–8	–	66	S3	1–7	C
67	0	1–8	–	68	S4	1–8	–
69	1	1–8	–	70	SP4 (1)	1–8	–
71	0	1–8	–	72	0	1–7	D

Note: C1-11 – Concentrator bits; **M1-3** – Maintenance bits; **S1-4** – Switch bits. **SP1-4** – Spoiler bits; **A1-2** – Alarm bits

SLC-96 frame alignment pattern is “001000110111001000110111” in 24 consecutive F-bit from frame 71-72 and frame 1-22. The frame synchronization is acquired when the frame alignment pattern is found in 24 consecutive F-bit positions in the data stream.

T1/E1/J1 Signaling

T1 trunks use what is called “robbed bit signaling” to carry signaling messages for voice applications. The least significant bit of all time slots in every 6th frame is robbed as the signaling bits. See the right-most column in Tables 1–3 above for signaling details for SF frame, ESF frame and SLC-96 frame, respectively.

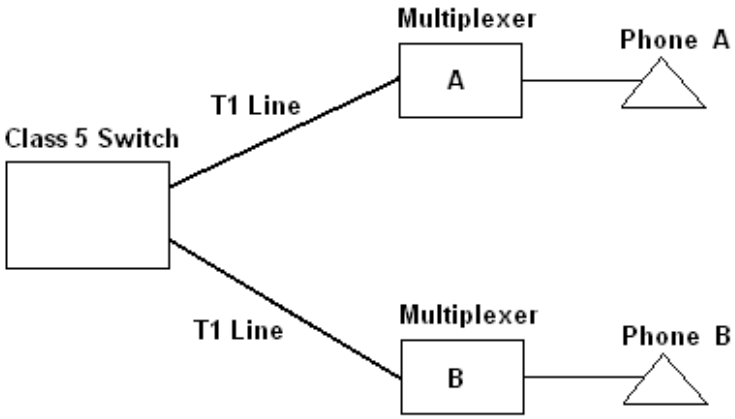
In SF format, A, B bits can define up to 4 signaling states. In application level, there are two signaling schemes–CAS and CCS. In CAS (channel associated signaling), each channel's signaling is carried by its own time slot every 6th frame. In CCS (Common channel signaling), use a dedicated channel, usually time slot 24, to carry the signaling messages for the entire trunk.

In ESF format, twice as many robbed bits from 6th, 12th 18th and 24th frames can be utilized for signaling, defining up to 16 signaling states. The four bits are called A, B, C, D bit, respectively. Sometimes this type of signaling is called ABCD Signaling.

In ESF format, besides for frame alignment, F-bit is utilized for two other purposes–Data Link and CRC bits. Data link bits are from every other frame of 24 ESF frames, totaling 12 bits. This creates a 4 kbps data link called Facility Data Link (FDL) used for delivering maintenance information and supervisory control for the trunk.

CRC bits are from 2nd, 6th, 10th, 14th, 18th and 22nd frame of ESF frames. Since there are in total 6 of these bits, it is denoted as CRC-6, which provides a mechanism to monitor the transmission quality of the DS1 facility.

Figure 1. ABCD Signaling in a Voice Application System



Call setup procedures:
[1] Phone A goes off-hook;
[2] Switch sends dial tone to Phone A;
[3] Phone A dials the number of Phone B;
[4] Phone B rings.
[5] Phone B goes off-hook and conversation starts.

Before a call is setup, suppose both phones are in on-off state. Both multiplexers send on-hook signaling ABCD = 0000 to the switch through T1 lines.

In Figure 1 Step [1], Multiplexer A will send the signaling ABCD = 0101 to the switch through T1 line that Phone A goes off-hook from on-hook state; In Step [4], the switch sends the signaling ABCD = 1111 to Multiplexer B for it to ring Phone B. In Step [3], if Phone B was already off-hook while Phone A is dialing its number, the switch would send a busy signaling ABCD = 0111 to Multiplexer A for it to send a busy tone to Phone A.

SLC-96 (TR-08) is a signaling scheme proprietary to AT&T aiming at enhancing the efficiency of T1 line utilization when T1 facility was precious resources. It is similar to D4/SF framing with respect to signaling. There is an A bit that appears in the least significant bit position of the time slots in Frame #6 and the B bit is in the least significant bit position of the time slots in Frame #12, and so on.

A and B bits permit nine possible signaling states via a three-level (tri-level) logic system:

1. Continuously zero;
2. Continuously one;
3. Alternating between zero and one. For example, 1/0 or 0/1 in alternating signaling frames.

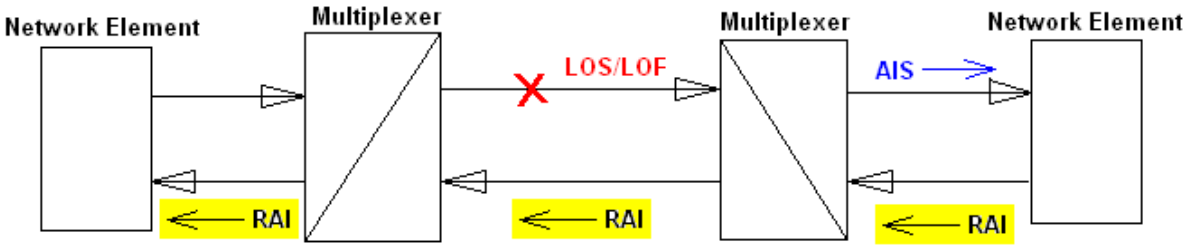
Example: the signaling for Positive Coin Check (sent to RT) is A = 0, B = 1/0. What that means is that all signaling frames within a SLC-96 super frame sending A-bit (Frame #6, #18, #30, #42, #54 and #60) will signal “continuously 0”; all signaling frames sending B-bit will be alternating: Frame #12 for “1”, Frame #24 for “0”, Frame #36 for “1”, Frame #48 for “0”, and so on.

Like ESF format, SLC-96 frame format uses its F-bit for frame alignment and other purposes. In 72 frame bits, 36 bits are the normal Ft pattern as well as 12 bits of the normal Fs pattern. The remaining 24 bits are used into different message fields: (1) Concentrator Bits C1-C11. (2) Maintenance Bits M1-M3. (3) Switch bits S1-S4. (4) Alarm bits A1-2. (5) Spoiler bits SP1-4.

T1/E1/J1 Alarms and Errors

T1 alarms include red alarm, yellow alarm and “blue alarm”. Alarms generation and pass-on can be illustrated as the following diagram in Figure 2 (color is used to denote the nature of alarm).

Figure 2. Initiation and Flow Direction of T1 Alarms



When there is a connection break between the two multiplexers, the one on the right (downstream) will detect a loss of signal (and a loss of frame) and flag a “red” alarm. Meanwhile, it will also send a RAI alarm (“yellow” alarm) to its counterpart multiplexer (upstream) and forward an AIS alarm (“blue” alarm) to its downstream network element.

RAI stands for Remote Alarm Indication. The transmission of RAI in T1 facility varies between SF format and ESF format. In SF format, RAI is transmitted by setting the Bit #2 position of every time slot in the trunk to “0”. In ESF format, RAI is transmitted by transmitting the 16-bit pattern “1111111100000000” in its data link bit (J1 SF/ESF RAI transmission is different.

AIS stands for Alarm Indication Signal. It is indicated by transmitting an unframed “all ones” bit stream to the downstream device. The reception of such stream indicates that the transmitting device of such stream is on “blue” alarm status.

Types of Errors on a T1 link include the following:

- Bipolar Violation (BPV): Two consecutive pulses are received with the same polarity.
- Loss of Signal (LOS): No signal transitions on a T1 link within a certain time window.
- Loss of Frame (LOF): T1 frame out of synchronization. With or without LOS.
- Excessive Zeros (EXZ): Eight (8) consecutive zeros appear on the link.

- “1”s Density Violations: Violation to the “Ones Density Rule” which states that in every 24 bits of information to be transmitted, there must be at least three pulses and no more than 15 zeros may be transmitted consecutively. Similar to EXZ error.
- Incorrect Pulse Widths: The pulse widths at the output of the customer network channel terminating equipment are out of specifications.
- Incorrect Signal Levels: The pulse amplitudes at the output of the customer network channel terminating equipment are out of specifications.

Incorrect pulse width or incorrect pulse amplitude or both will cause the pulse template mask to be violated.

IDT SuperJet Transceiver's Handling of Signaling, Alarms and Errors

Handling of T1 Signaling

In receive direction, signaling bits are extracted from incoming bit stream. Extracted A, B, C and D signaling bits are (1) stored in the Extracted Signaling Data/Extract Enable register (see indirect registers RCRB); (2) output on the RSIGn/MRSIGA/B pins of the chip.

Conversely, there are two ways to provide A, B, C and D signaling bits in transmit direction to outgoing bit stream: (1) data programmed into A, B, C and D of Signaling Trunk Conditioning Registers (indirect registers); (2) data provided by TSIGn/MTSIGA/B pins.

Handling of T1 Alarms

Alarm Detection: The status of the Red alarm, Yellow alarm and Blue alarm are indicated by the corresponding status bit. T1/J1 Alarm Status register keeps a static status of Red, Yellow and Blue alarms. T1/J1 Alarm Indication register will be logged whenever there is a status transition change (from “0” to “1” or from “1” to “0”) of T1/J1 Alarm Status bits. T1/J1 Alarm Control register controls whether any of the alarms will initiate an interrupt.

In addition, for each of the three types of alarms, there are Declare and Clear Threshold registers which configure the threshold for these alarms to be declared or cleared.

Alarm Generation:

- **Generation of AIS** – upon LOS, the port will automatically transmit an unframed all ones' data pattern, if so configured.
- **Generation of LOS** – if received signal meets corresponding standards, the receiver will declare Loss of Signal (LOS) alarm indicated by both internal status register bits and dedicated pin.
- **Generation of LOF** – Red alarm includes both LOS and LOF. LOS is described above. If received data stream loses framing pattern threshold, LOF will be indicated by status registers.
- **Generation of RA**I – RAI is transmitted by transmitting the 16-bit pattern “1111111100000000” in its data link bit.

Handling of T1 Errors

IDT SuperJET transceivers are built with a set of indirect registers for performance monitoring (PMON). PMON provides counters to count the following 7 types of errors/events for T1/J1 and 8 types for E1, on a per-channel basis.

Table 4: Types of Error/Event Counters for T1/J1

Address	PMON Indirect Register	Address	PMON Indirect Register
00H	CRCE Counter Mapping 0	06H	PRGD Counter Mapping 0
01H	CRCE Counter Mapping 1	07H	PRGD Counter Mapping 1
02H	FER Counter Mapping 0	08H	LCV Counter Mapping 0
03H	FER Counter Mapping 1	09H	LCV Counter Mapping 1
04H	COFA Counter Mapping	0AH	DDSE Counter Mapping 0
05H	OOF Counter Mapping	0BH	DDSE Counter Mapping 1

Table 5: Types of Error/Event Counters for E1

Address	PMON Indirect Register	Address	PMON Indirect Register
00H	CRCE Counter Mapping 0	08H	LCV Counter Mapping 0
01H	CRCE Counter Mapping 1	09H	LCV Counter Mapping 1
02H	FER Counter Mapping 0	0AH	TCRCE Counter Mapping 0
03H	FER Counter Mapping 1	0BH	TCRCE Counter Mapping 1
04H	COFA Counter Mapping	0CH	FEBE Counter Mapping 0
05H	OOF Counter Mapping	0DH	FEBE Counter Mapping 1
06H	PRGD Counter Mapping 0	0EH	TFEBE Counter Mapping 0
07H	PRGD Counter Mapping 1	0FH	TFEBE Counter Mapping 1

Refer to device datasheet for indirect registers details.

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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan

www.renesas.com

Contact Information

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