Introduction

A VCXO is a crystal oscillator with the property that the output frequency (Fout) can be offset from the nominal in either direction, over a continuous range of frequencies by the application of an analog voltage to its Control Voltage pin (V_C). The control voltage is tied to a varactor diode. This type of diode has a variable capacitance that is a function of the voltage applied. In Figure 1 and Figure 2, notice that as V_C changes it causes changes in C_L (capacitive loading). Changes in C_L cause a change in Fout. As seen in Figure 2, ideally there is an linear relationship between V_C and Fout.

Figure 1. Typical VCXO

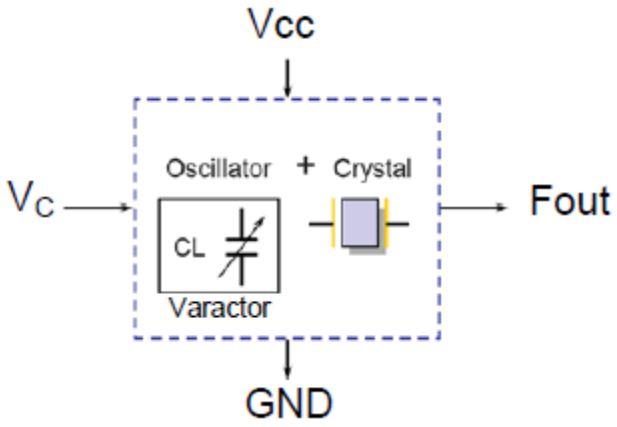
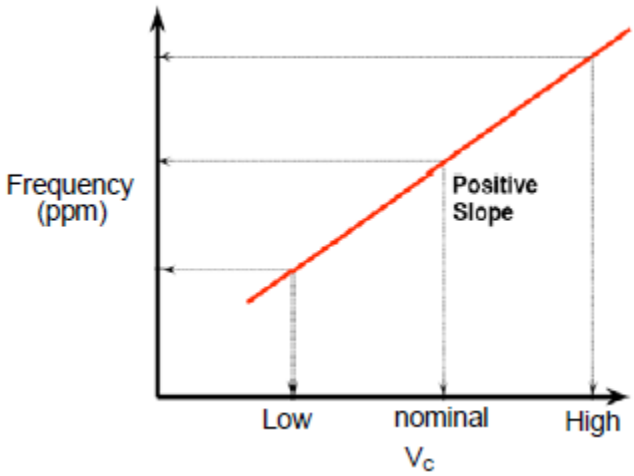


Figure 2. Typical Pull Range Curve



Definition of APR

APR–The guaranteed plus and minus frequency deviation of a VCXO from the nominal frequency when the control voltage is set to the maximum and minimum value. It is guaranteed over manufacturing tolerances, supply voltage, operating temperature and aging.

APR is calculated by subtracting the Total Pull Range from the Total Stability of the VCXO. The Total Pull Range is the maximum variation in VCXO frequency over changes in control voltage under constant supply voltage and temperature. Total Stability is the variation in VCXO frequency when the control voltage is held at the nominal value over changes in manufacturing tolerances, supply voltage, operating temperature and aging. This difference results in the frequency variation that can be guaranteed due to the control voltage independent of all other conditions and variations.

Example of an APR Calculation

APR is derived from an output frequency range budget for a VCXO that accounts for all factors that contribute to the frequency deviation of the VCXO. Refer to the example calculation.

$$\text{APR} = (\text{Total Pull Range}) - (\text{Total Stability})$$

$$\text{APR} = \text{Total Pull Range } (\pm 160) - \begin{cases} \text{Frequency Tolerance at } 25^{\circ}\text{C} \pm 5^{\circ}\text{C} = (\pm 20 \text{ ppm}) \\ \text{Frequency Stability from } -40^{\circ}\text{C to } -85^{\circ}\text{C} = (\pm 20 \text{ ppm}) \\ \text{Supply Voltage Tolerance (Vcc} \pm 5\%) = (\pm 10 \text{ ppm}) \\ \text{10 years Aging Tolerance} = (\pm 10 \text{ ppm}) \end{cases}$$

$$\text{APR} = \pm 100$$

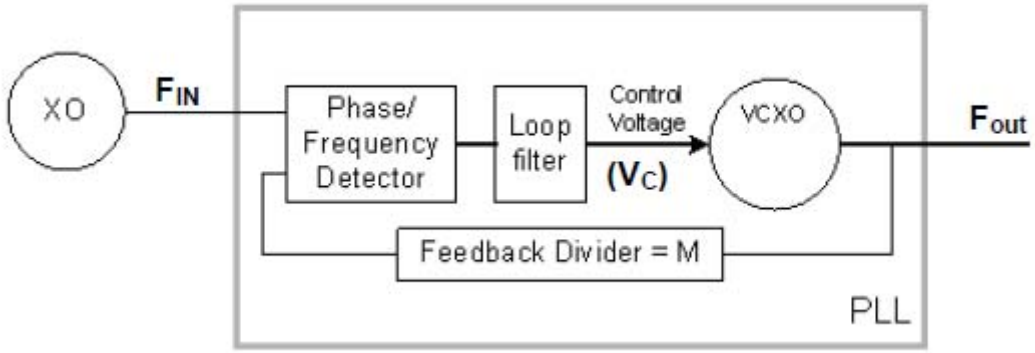
In this example, a VCXO characterized by an APR of ±100 ppm means that a PLL that uses this VCXO can lock to an input reference with as much as ±100 ppm of variation of its nominal center frequency.

APR Applied to PLL design

A phase-locked loop (PLL) is a an example of a control system using negative feedback that generates an output clock signal that has a fixed relation to the phase of a reference clock signal (FIN). The PLL was developed as a solution to a fundamental problem; that if a clock is required which of a higher frequency than an existing clock or of the same frequency but lower jitter, or both higher frequency and lower jitter, then no linear operation on the existing clock will be able to transform the existing clock to the required clock. Instead a new oscillator is required, which has to exactly match the frequency and phase of the existing clock. The phase matching requirement requires a negative feedback loop.

The PLL creates an error signal by dividing the VCXO clock frequency and phase by the value of feedback divider (M), and comparing it with the phase and frequency of the input clock frequency and phase, FIN, in the Phase/Frequency Detector. The output of the Phase/Frequency detector is low pass filtered by the Loop Filter to generate the Control Voltage (VC) adjustment of FOUT, thus closing the loop. When locked, the PLL output frequency (FOUT) is exactly M times the input frequency (FIN) and is phase aligned with the input reference clock. If Fout has to be equal to Fin, then a post divider of value M is added or M is set to 1.

Figure 3. Basic PLL Building Blocks



The input reference frequency, FIN, has a ± ppm tolerance due to the crystal oscillator (XO) manufacturing variations. This includes tolerance, stability, supply voltage and aging. The frequency of the VCXO has to have a guaranteed tunable range of at least the same ppm variation in order to track and maintain phase and frequency lock over the frequency variations of the input reference. Since the VCXO is itself an oscillator, its frequency is subject to the same variation due to manufacturing tolerance, stability, power supply voltage and aging. These variations must be guaranteed and should be subtracted from the total pull range. If the VCXO does not have sufficient APR and the input reference is at one of the frequency extremes, the PLL will not lock and the output frequency will not be M times the input frequency.

In conclusion, a VCXO characterized by an APR frees the PLL designer from accounting for the details of the additional internal variation that affect the center frequency of the VCXO. It is only necessary to be sure that the VCXO APR is as large as the ppm variation of the PLL input reference.

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