

Introduction

The VCXO tuning procedure developed here has two applications. First, in the design phase as a means of selecting a crystal, that when paired with a given VCXO oscillator will yield a VCXO with sufficient pull range for the application. Second, once the selected crystal and oscillator are in the lab and a sample characterized crystal is obtained, the procedure can be used to directly tune the VCXO center frequency with a minimum number of tuning capacitor iterations.

Tuning a VCXO is not as straightforward as tuning a clock generator; a VCXO is not tuned for a single frequency. A VCXO is tuned when the magnitude of the positive pull range from the VCXO center frequency is the same as the magnitude of the negative pull range. But the magnitude of the pull range is not known before hand. Further, the non-linearity of the load curve means that the tuning capacitor that centers the VCXO pull range is not that capacity, when added to the average of the maximum and minimum varactor capacities and all the parasitic capacities, equals the crystal load capacity.

Using the Load Curve to Tune a VCXO

For the purposes of crystal selection and tuning, two sets of information are required. The crystal circuit element values C0, C1, and CLn, and the load curve¹ are shown in Equation 1. CLn is the nominal parallel load capacity that tunes the crystal parallel resonance to the crystal center frequency, FL. In standard usage, this is CL but here the n suffix is added because in the derivation that follows, CL is varied plus or minus about the nominal value of CL.

Also required are the values of the VCXO oscillator's voltage variable capacitors when the control voltage is set to the maximum and minimum values, CVH and CVL. CLn is subtracted from each of these two capacities to form ΔCVH and ΔCVL, which define the largest decrease in the load capacity from CLn and the largest increase in load capacity from CLn respectively. These two deviations in turn describe the range of frequency offsets, ΔFL/FL, from the crystal center frequency when loaded by the varactor capacity across all VXO control voltages.

This information allows the tuning capacitor that centers the VCXO pull range about FL and the positive and negative tuning range to be calculated directly as will be shown below. Note that the fractional frequency offsets have not been converted to ppm; ΔFL and FL are in Hz. The normalization of all capacities by Y=C0+CLn simplifies the tuning derivation that follows.

$$\frac{\Delta F_L}{F_L} = -\frac{1}{2} \frac{C1}{Y} \frac{\frac{\Delta CL}{Y}}{\left(1 + \frac{\Delta CL}{Y}\right)} \quad \text{Equation 1}$$

where

$$Y = C0 + CLn$$

The polarity of the voltage transfer curve of the VCXO is not relevant to the tune procedure. It is immaterial whether the maximum and minimum control voltages correspond to the maximum and minimum VCXO frequencies or vice versa. Further, the varactor capacities being used are the equivalent parallel varactor capacities across the crystal terminals. The varactor capacitors are typically implemented as two shunt capacitors to ground, one on the VCXO oscillator input and on the oscillator output. If these capacitors are provided by the oscillator manufacturer ground referenced, simply divide the values by two to obtain the parallel values of ΔCVH and ΔCVL.

First solve Equation 1 for the normalized parallel load capacity across the crystal for a given ΔFL/FL.

$$\frac{\Delta CL}{Y} = 2 \frac{\frac{Y}{C1} \frac{\Delta F_L}{F_L}}{1 + \frac{Y}{C1} \frac{\Delta F_L}{F_L}} \quad \text{Equation 2}$$

¹ IDT Application Note [AN-831](#), "The Crystal Load Curve"

Equation 2 is used to determine the normalized values of ΔC_{VH} and ΔC_{VL} in terms of the fractional offset frequency errors measured when the control voltage is at the maximum and minimum value respectively in Equation 3 and Equation 4.

$$\frac{\Delta C_{L_{VH}}}{Y} = \frac{\Delta C_{VH}}{Y} = 2 \frac{\frac{Y}{C1} \left[\frac{\Delta F_L}{F_L} \right]_{VH}}{1 + \frac{Y}{C1} \left[\frac{\Delta F_L}{F_L} \right]_{VH}} \quad \text{Equation 3}$$

$$\frac{\Delta C_{L_{VL}}}{Y} = \frac{\Delta C_{VL}}{Y} = 2 \frac{\frac{Y}{C1} \left[\frac{\Delta F_L}{F_L} \right]_{VL}}{1 + \frac{Y}{C1} \left[\frac{\Delta F_L}{F_L} \right]_{VL}} \quad \text{Equation 4}$$

The condition to determine C_{TC} , the parallel tuning capacitor, is that the algebraic sum of the fractional frequency offsets generated is zero when the control voltage of the VCXO is at the maximum and minimum and the tuning capacitor have been added to the crystal load. This condition is shown in Equation 5 below. When the magnitude of the corresponding frequency offsets, $[\Delta F_L/F_L]_{Tuned+}$ and $[\Delta F_L/F_L]_{Tuned-}$, at the maximum and minimum control voltage are equal, the center frequency of the oscillator will also be at the nominal frequency.

$$\left[\frac{\Delta F_L}{F_L} \right]_{Tuned+} + \left[\frac{\Delta F_L}{F_L} \right]_{Tuned-} = -\frac{1}{2} \frac{C1}{Y} \left(\frac{\frac{\Delta C_{VH} + C_{TC}}{Y}}{1 + \frac{\Delta C_{VH} + C_{TC}}{Y}} \right) - \frac{1}{2} \frac{C1}{Y} \left(\frac{\frac{\Delta C_{VL} + C_{TC}}{Y}}{1 + \frac{\Delta C_{VL} + C_{TC}}{Y}} \right) \quad \text{Equation 5}$$

$$= 0$$

Rearranging results in a quadratic in C_{TC} .

$$0 = \frac{\Delta C_{VH} + C_{TC}}{\left(1 + \frac{\Delta C_{VH} + C_{TC}}{Y} \right)} + \frac{\Delta C_{VL} + C_{TC}}{\left(1 + \frac{\Delta C_{VL} + C_{TC}}{Y} \right)}$$

$$= (\Delta C_{VH} + C_{TC})(Y + \Delta C_{VL} + C_{TC}) + (\Delta C_{VL} + C_{TC})(Y + \Delta C_{VH} + C_{TC})$$

$$= Y(\Delta C_{VH} + \Delta C_{VL}) + 2Y C_{TC} + 2(\Delta C_{VH} + C_{TC})(\Delta C_{VL} + C_{TC}) \quad \text{Equation 6}$$

$$0 = Y(\Delta C_{VH} + \Delta C_{VL}) + 2\Delta C_{VH} \Delta C_{VL} + 2(Y + \Delta C_{VH} + \Delta C_{VL})C_{TC} + 2C_{TC}^2$$

Equation 6 can be solved for both roots, but the most positive square root is the physically meaningful solution. This can be checked by substitution back into the load curve, Equation 1.

Since the most positive root is CTC, solving the quadratic can be done directly.

$$\begin{aligned}
 C_{TC} &= -\left(\frac{Y + \Delta C_{VH} + \Delta C_{VL}}{2}\right) + \sqrt{\left(\frac{Y + \Delta C_{VH} + \Delta C_{VL}}{2}\right)^2 - \frac{Y}{2}(\Delta C_{VH} + \Delta C_{VL}) - \Delta C_{VH} \Delta C_{VL}} \\
 &= \frac{Y}{2} \left[-\left(1 + \frac{\Delta C_{VH}}{Y} + \frac{\Delta C_{VL}}{Y}\right) + \sqrt{\left(1 + \frac{\Delta C_{VH}}{Y} + \frac{\Delta C_{VL}}{Y}\right)^2 - 2\left(\frac{\Delta C_{VH}}{Y} + \frac{\Delta C_{VL}}{Y}\right) - 4\frac{\Delta C_{VH} \Delta C_{VL}}{Y}} \right] \\
 &= \frac{Y}{2} \left[-\left(1 + \frac{\Delta C_{VH}}{Y} + \frac{\Delta C_{VL}}{Y}\right) + \sqrt{1 + 2\frac{(\Delta C_{VH} + \Delta C_{VL})}{Y} + \left(\frac{\Delta C_{VH}}{Y} + \frac{\Delta C_{VL}}{Y}\right)^2 - 2\frac{(\Delta C_{VH} + \Delta C_{VL})}{Y} - 4\frac{\Delta C_{VH} \Delta C_{VL}}{Y^2}} \right] \\
 &= \frac{Y}{2} \left[-\left(1 + \frac{\Delta C_{VH}}{Y} + \frac{\Delta C_{VL}}{Y}\right) + \sqrt{1 + \left(\frac{\Delta C_{VH}}{Y}\right)^2 + 2\frac{\Delta C_{VH} \Delta C_{VL}}{Y^2} + \left(\frac{\Delta C_{VL}}{Y}\right)^2 - 4\frac{\Delta C_{VH} \Delta C_{VL}}{Y^2}} \right] \\
 &= \frac{Y}{2} \left[\sqrt{1 - 2\frac{\Delta C_{VH} \Delta C_{VL}}{Y^2} + \left(\frac{\Delta C_{VH}}{Y}\right)^2 + \left(\frac{\Delta C_{VL}}{Y}\right)^2} - \left(1 + \frac{\Delta C_{VH} + \Delta C_{VL}}{Y}\right) \right] \\
 &= \frac{1}{2} \left[\sqrt{Y^2 + (\Delta C_{VL} - \Delta C_{VH})^2} - (Y + \Delta C_{VH} + \Delta C_{VL}) \right]
 \end{aligned}$$

Substituting for Y and removing the CLn offset in the capacities results in a simpler form in terms of physical circuit capacities.

$$\begin{aligned}
 C_{TC} &= \frac{1}{2} \left[\sqrt{Y^2 + (\Delta C_{VL} - \Delta C_{VH})^2} - (Y + \Delta C_{VH} + \Delta C_{VL}) \right] \\
 &= \frac{1}{2} \left[\sqrt{(C0 + CLn)^2 + ((C_{VL} - CLn) - (C_{VH} - CLn))^2} - (C0 + CLn + C_{VH} - CLn + \Delta C_{VL} - CLn) \right]
 \end{aligned}$$

$$C_{TC} = \frac{1}{2} \left[\sqrt{(C0 + CLn)^2 + (C_{VL} - C_{VH})^2} - (C0 + C_{VH} + \Delta C_{VL} - CLn) \right] \quad \text{Equation 7}$$

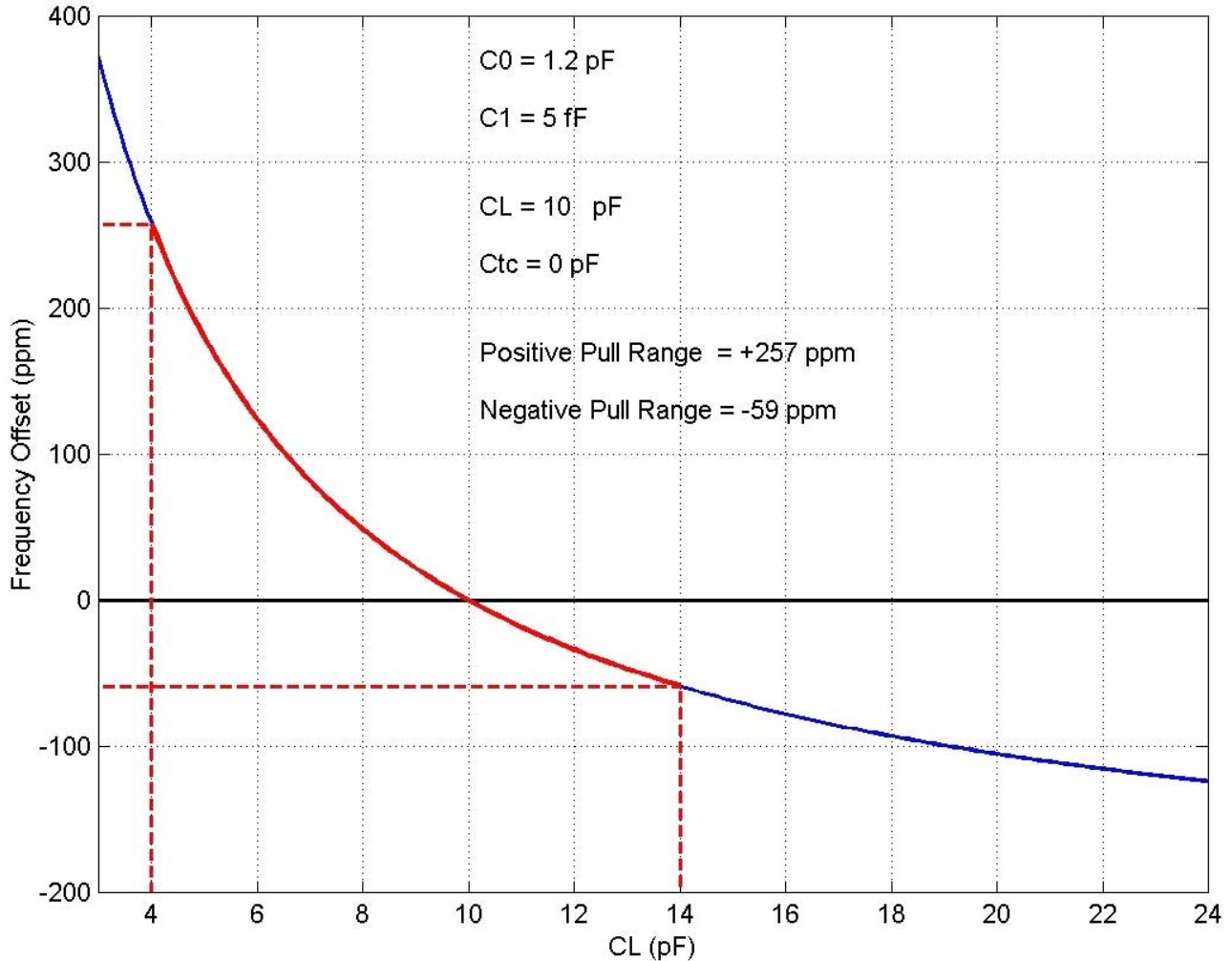
Typically the value of CTC is positive and indicates that the VCXO can be tuned to the center frequency. A negative tuning capacity indicates one of three things:

1. The amount of capacity that must be removed from the PCB in a new board layout if the crystal is to be retained.
2. The amount by the previous tune capacitor was too large.
3. The minimum amount by which the load capacity of the crystal must increased to yield a tunable VCXO. The value of this additional capacity is used to specify a new crystal that can be tuned and used with the existing circuit board.

Example Tune

The steps of the tune procedure are illustrated with a simple hypothetical case of a VCXO and PCB layout with no tuning cap added. The pre-tune characteristics of the VCXO are shown in Figure 1 below; $\Delta C_{VL} = 14\text{pF}$, $C_{VH} = 4\text{pF}$ and therefore $\Delta C_{VL} = +4\text{pF}$, $\Delta C_{VH} = -6\text{pF}$.

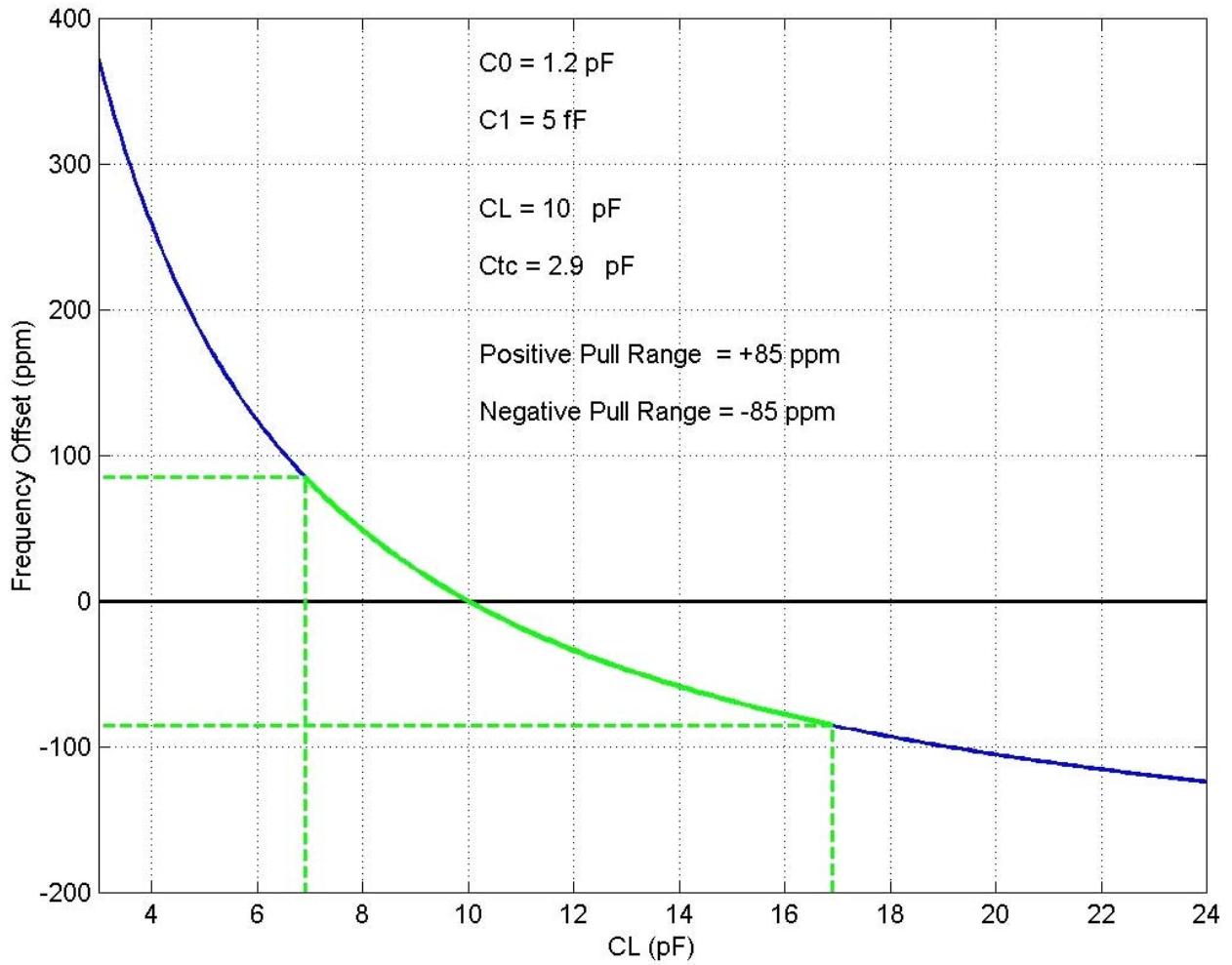
Figure 1. Pre-Trim VCXO Pull Range Example



The value of CTC calculated from Equation 7 is 2.9pF. This value has been added across the crystal leads to center the pull range of the VCXO. The final pull range is shown in Figure 2 where three things can be noted.

1. The change in C_L remains the same; the change in the capacity of the varactor capacitors is unaffected by the addition of the fixed CTC capacity.
2. The reduction in positive pull range is much larger than the gain in negative pull range; a consequence of the non-linearity of the pull curve.
3. The pull range of the VCXO is centered at $C_L=10\text{pF}$.

Figure 2. Post-Trim VCXO Pull Range Example



If this example was for a characterized crystal and an oscillator in the lab, the value of C_{TC} is to be applied to the VCXO. This is accomplished with two tuning capacitors; one applied at the crystal lead connected to the oscillator input and ground and the other applied at the crystal lead connected to the oscillator output and ground. The value of these two new capacitors is twice that of C_{TC} . The doubling comes about because the AC waveforms across the crystal are 180° out of phase. Since the current through each grounded tuning capacitor is the same, the two capacitors can equivalently be placed in series across the crystal leads. The parallel equivalent capacity is then half that of the two grounded capacitors.

Revision History

Rev.	Date	Originator	Description of Change
A	05/12/14	–	Initial release.
B	09/23/14	P. Wissell	<ol style="list-style-type: none"> 1. Added text to section “Using the Load Curve to Tune a VCXO” to eliminate the need to consult AN-831 for some nomenclature definitions. 2. Simplified Equation 7.

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers skilled in the art designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only for development of an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising out of your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Rev.1.0 Mar 2020)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
www.renesas.com/contact/

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.