

Introduction

In order to discuss RMS Phase Jitter, some basics phase noise theory must be understood. Phase noise is often considered an important measurement of spectral purity which is the inherent stability of a timing signal. Phase noise is the frequency domain representation of random fluctuations in the phase of a waveform caused by time domain instabilities called jitter. An ideal sinusoidal oscillator, with perfect spectral purity, has a single line in the frequency spectrum. Such perfect spectral purity is not achievable in a practical oscillator where there are phase and frequency fluctuations. Phase noise is a way of describing the phase and frequency fluctuation or jitter of a timing signal in the frequency domain as compared to a perfect reference signal.

Generating Phase Noise and Frequency Spectrum Plots

Phase noise data is typically generated from a frequency spectrum plot which can represent a time domain signal in the frequency domain. A frequency spectrum plot is generated via a Fourier transform of the signal, and the resulting values are plotted with power versus frequency. This is normally done using a spectrum analyzer.

A frequency spectrum plot is used to define the spectral purity of a signal. The noise power in a band at a specific offset (F_o) from the carrier frequency (F_c) compared to the power of the carrier frequency is called the dBc Phase Noise.

$$\text{dBc Phase Noise} = \frac{\text{Power Level of a 1Hz band at an offset } (F_o)}{\text{Power Level of the carrier Frequency } (F_c)}$$

A Phase Noise plot is generated using data from the frequency spectrum plot. Refer to [Figure 1A](#). Using the dBc phase noise definition and calculating the dBc values for a continuous moving 1Hz band over the frequency offset range of interest generates a phase noise plot. A phase noise plot is simply these dBc values plotted versus the offset frequency (F_o). Refer to [Figure 1B](#). To summarize, phase noise is specified as the ratio of the noise power present in a 1Hz band at a specified offset from the carrier frequency to the power value of the carrier. Generally, a phase noise plot is single side, only one side of the frequency spectrum is plotted. This is due to the assumption that the frequency spectrum plot has a Gaussian profile and that both sides of the distribution are equal. For phase noise measurements which contain deterministic components, special consideration must be taken. Typically, a phase noise plot has the domain axis is in logarithmic format and the range in linear format. Refer to [Figure 1B](#).

A phase noise plot can now be used to relate the time domain RMS jitter specification to the frequency domain spectral purity. The area under the plot is proportional to the RMS jitter squared. An application may only be interested in a range of the phase noise plot and typically will specify that range or apply a mask to identify the area of interest and maximum dBc values permitted. This mask is often called a Jitter Mask. Refer to [Figure 2](#).

Figure 1. Generating a Phase Noise Plot from the Frequency Spectrum Plot

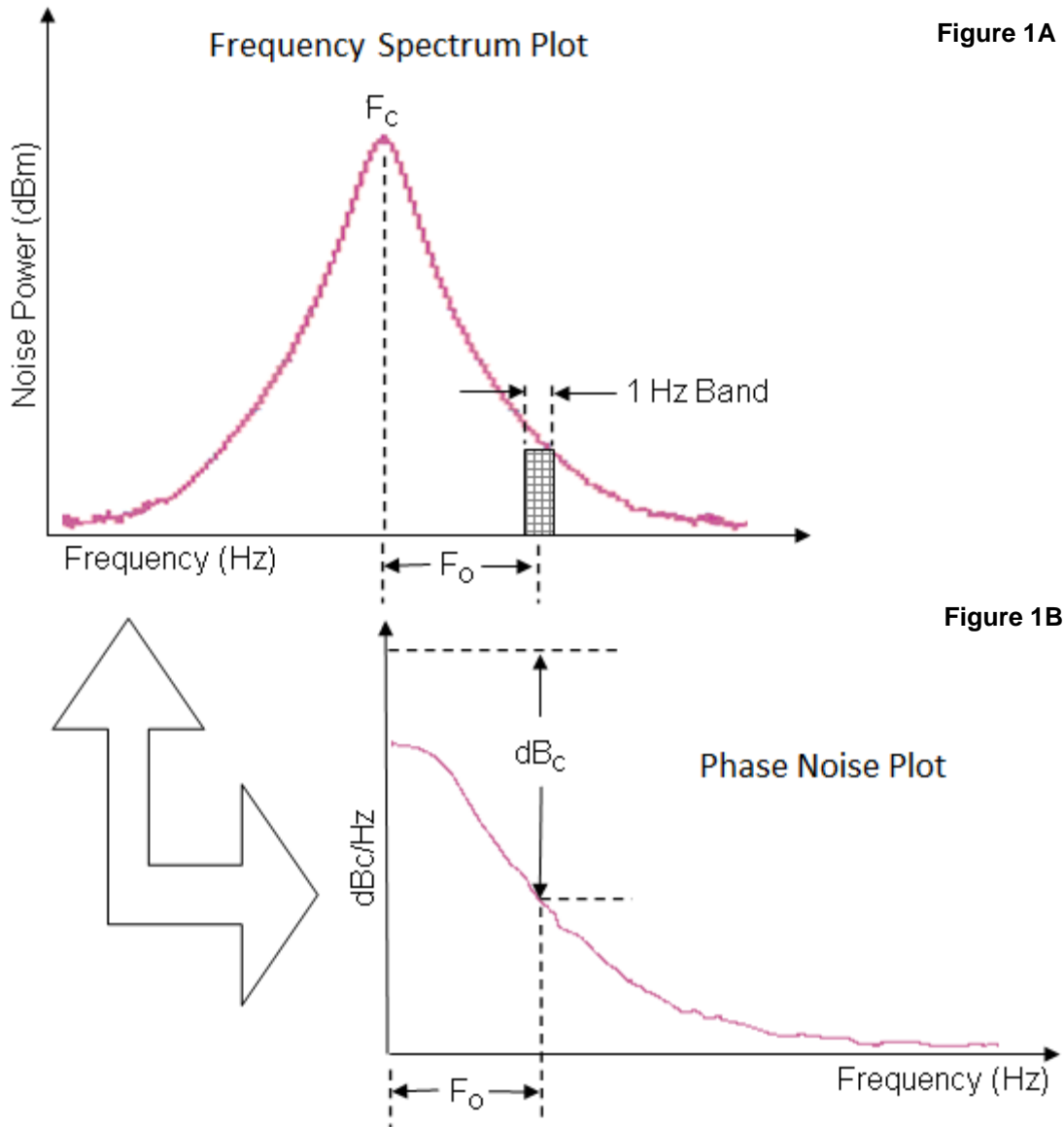
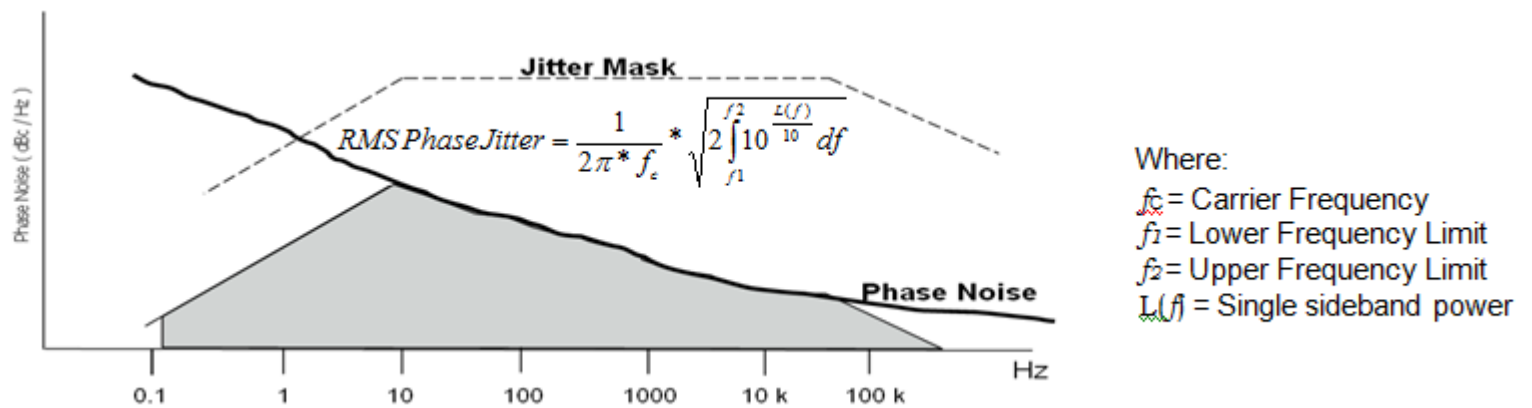
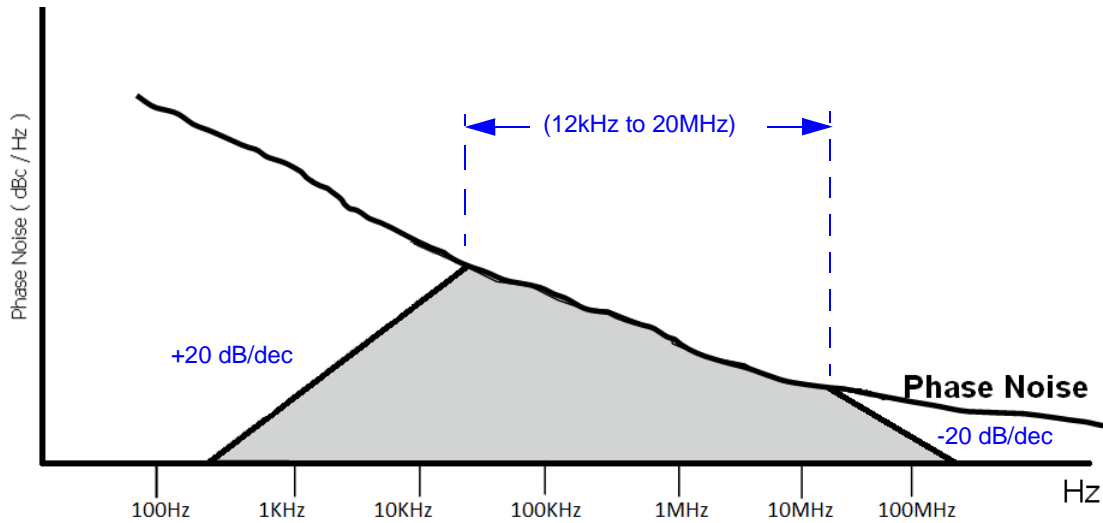


Figure 2. Applied Jitter Mask



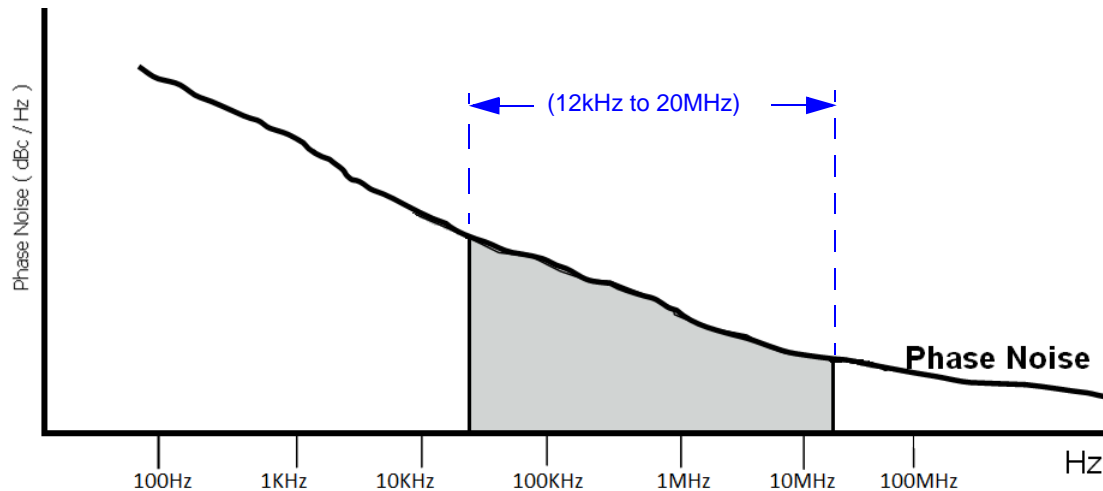
In order to specify a Jitter Mask, a systems transfer function must be analyzed. The jitter mask specifies the clock performance in ways that actually affect the system and will help avoid over-specification of the clock performance. In addition, the jitter mask will provide different weighting of different jitter frequencies. Many of these jitter masks have been predetermined by industry protocols. The most common being the SONET, 12kHz to 20MHz, OC48 Jitter Generation specification for Telcordia GR-253-CORE. Though many of the clocking devices using this specification are not SONET, this jitter mask has become an industry standard of merit for comparing performance. A jitter mask can have a profile of a band-pass, low-pass or high-pass filter with roll offs that vary in dB/decade. Refer to [Figure 3](#).

Figure 3. Filtered Jitter Mask



A jitter mask can also have a “brick-wall” profile. Refer to [Figure 4](#). A brick-wall profile does not have the typical filter response with a gradual roll-off of a few dB/decade slope, but rather has an infinite sloped roll-off. Brick-wall jitter masks are more common due to measurement equipment limitations. Currently, some of the industry standard Phase noise measurement equipment does not have the capability to add a roll-off to the filter, but it can be done with additional software. In most cases, the difference between filtered and brick-wall jitter is negligible, but as RMS jitter requirements continue to become more stringent, this could become an issue in the future.

Figure 4. “Brick-Wall” Jitter Mask



As with most timing specifications, special considerations must be taken when measuring phase noise. The primary issue is the noise floor capability of the measurement system. The noise floor can be defined as the measure of the signal created from the sum of all the noise sources and unwanted signals within a measurement system. If the measurement system does not have the necessary noise-floor performance required by the device under test (DUT), the results will be inaccurate. The phase noise plot will track the noise floor of the equipment instead of the true performance of the DUT. In addition, all precautions must be taken to avoid any additional noises from coupling into the measurement system. Proper shielding must be in place to ensure an accurate measurement. RMS Phase jitter measurements are becoming increasingly important in the characterization and qualification of high-speed computing and communication systems. It is crucial that the proper equipment and procedure be followed.

RMS phase jitter has now become a widely accepted industry standard. In the past, it was most commonly seen in Telecommunication applications, but with the expansion of Ethernet and PCI Express, both phase noise and RMS phase jitter has migrated into Networking and consumer applications. It is important to have a practical and conceptual understanding of Phase noise.

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(Rev.4.0-1 November 2017)

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