Introduction

This application note addresses the possible self oscillation of the differential input due to external termination in certain board level design. Examples of solutions to prevent this type of oscillation are provided. The IDT Netcom product differential clock input is designed to receive signals from high speed differential clock drivers for examples LVDS, LVPECL, LVHSTL, SSTL, and HCSL drivers. To prevent input oscillation when the input pins are floating, the true clock input CLK has a built-in ~51KΩ pull-up resistor and the complement clock input nCLK has a built-in 51KΩ pull-down (or both pull-up and pull-down resistor). Therefore, the CLK pin is held at logic low and the nCLK pin is held at logic high. Using these high impedance internal pull-down/pull-up resistors does not affect the external termination values required by the various driver types.

In general, high speed differential clock drivers require matched load termination near the differential input. The termination generates equal DC potential at the differential input when the clock signal is absent due to tri-stated outputs or floating inputs. This equal potential can cause oscillation at high frequencies which will be prevented by placing a small DC offset input voltage between CLK and nCLK. Several termination examples of self oscillation prevention for various types of termination are provided.

LVDS Interface

A general LVDS interface is shown in Figure 1. In a 100Ω differential transmission line environment, LVDS drivers require a matched load termination of 100Ω across the CLK/nCLK pair. In this case, the LVDS output forces CLK to a logic high and the complementary LVDS output forces nCLK to a logic low, or vice versa. The load termination typically provides sufficient voltage difference to prevent oscillation.

If the CLK/nCLK inputs are driven by a tri-stated output, the 100Ω is negligible compared to the 51KΩ pull-up and pull-down resistors. The voltage drop across R1 is very close to 0V. Therefore, high frequency oscillation at the input circuitry can occur when the driver is tri-stated. This oscillation can be prevented by introduce the DC offset between the CLK and nCLK inputs without affecting the matched load. Figure 2 shows how to add the external pull-up resistor R2 and the external pull-down resistor R3 to increase the DC voltage between CLK and nCLK. Effectively, this prevents oscillation. However, setting this swing too wide will increase the offset between the CLK and nCLK signals during normal operation when the clock signal is present. General equations to determine the R1, R2 and R3 values are provided below. The board designer should consider these trade-offs when choosing the voltage across R1.

R1, R2 and R3 can be determined by using the following equations:

\[
\begin{align*}
R2 &= R3 = \text{Zo_diff} \times \frac{\text{VDD}}{2 \times \text{VR1}} \quad (1) \\
R1 &= \frac{\text{VR1} \times (2 \times R2)}{\text{VDD} - \text{VR1}} \quad (2)
\end{align*}
\]

where,

\[
\begin{align*}
\text{Zo_diff} &\text{ is the differential characteristic impedance of the transmission line.} \\
\text{VR1} &\text{ is the DC voltage drop across R1.}
\end{align*}
\]

For example, if the DC voltage across R1 is 100mV and the differential characteristic of the transmission line is 100Ω, then the following values for R1, R2, and R3 are chosen.

\[
\text{Zo_diff} = 100\Omega, \, \text{VR1} = 50\text{mV}, \, \text{VDD} = 3.3\text{V}
\]

From equation (1), \(R2 = R3 = 100\Omega \times \frac{3.3\text{V}}{2 \times 50\text{mV}} = 3.3\text{K}\Omega\).

Substitute R2 to equation (2), \(R1 = 50\text{mV} \times \frac{2 \times 3.3\text{K}\Omega}{(3.3\text{V} - 50\text{mV})} = 101.5\Omega\).
Figure 1. General LVDS to Differential Input Interface

Figure 2. LVDS Driver with Tri-state to Differential Input Interface. Add small DC offset between CLK and nCLK to prevent oscillation.

LVPECL Interface

A general 3.3V LVPECL driver to differential input interface is shown in Figure 3. In a 50Ω single ended or 100Ω differential transmission line environment, LVPECL drivers require a matched load termination of 50Ω to VCC-2V = 1.3V for each output. In this case, the LVPECL driver output forces CLK to logic high and the complementary LVPECL output forces nCLK to logic low or vice versa. The CLK and nCLK typically have sufficient potential difference to prevent oscillation.

For the CLK/nCLK inputs driven by a tri-state output, the bias resistor will generate the same potential of 1.3V at both CLK and nCLK pins. The voltage between CLK and nCLK is very close to 0V. As a result, high frequency oscillation at the input circuitry can occur when the driver is tri-stated. This oscillation will be prevented by placing a minimum peak-to-peak input voltage between the CLK and nCLK inputs which does not affect the matched load. Figure 4 shows the method for changing the bias resistor values at the CLK input. General equations to determine the R3 and R1 values are provided below. Effectively, this prevents oscillation. However, setting this swing too wide will increase the offset between the CLK and nCLK signals. The board designer should consider these trade-offs when choosing the voltage between CLK and nCLK.

R1 and R3 can be determined by using the following equations:

\[
R3 = \frac{Z_0 \times VDD}{VDD - 2 - Voffset} \quad (3)
\]

\[
R1 = \frac{R3 \times Z_0}{R3 - Z_0} \quad (4)
\]

where,
Zo is characteristic impedance of the transmission line. Voffset is the DC voltage between CLK and nCLK.

For example, if the DC voltage between CLK and nCLK is set to 100mV and the characteristic impedance of the transmission line is 50Ω, then the values for R3 and R1 are as follows:

\[
\begin{align*}
R3 &= 50Ω \times \frac{3.3V}{(3.3V - 2V - 100mV)} = 137Ω \\
R1 &= 50Ω \times \frac{137Ω}{(137Ω - 50Ω)} = 78Ω
\end{align*}
\]

Figure 5 shows general termination for an LVPECL driver with AC coupling. When the clock signal is absent, the bias resistors R1, R2, R3 and R4 will create an equal DC potential for the CLK and nCLK input pair. To prevent oscillation, the small offset described above can be introduced by using equations (3) and (4). An example is shown in Figure 6.

**Figure 3. General LVPECL to Differential Input Interface**

![General LVPECL to Differential Input Interface Diagram](image)

**Figure 4. LVPECL Driver with Tri-state to Differential Input Interface. Add a small offset between CLK and nCLK to prevent oscillation.**

![LVPECL Driver with Tri-state to Differential Input Interface Diagram](image)
Figure 5. General LVPECL Driver with AC couple to Differential Input Interface

![Diagram of LVPECL Driver with AC couple to Differential Input Interface](image1)

Figure 6. LVPECL Driver AC couple to Differential Input Interface with a small offset at the CLK and nCLK to prevent oscillation.

![Diagram of LVPECL Driver with AC couple to Differential Input Interface with offset](image2)

LVHSTL Interface

Figure 7 and Figure 8 show general and AC coupled terminations for an open source LVHSTL interface. Typically, open source LVHSTL drivers do not have tri-state capability. The driver will force one side high and the other side low during reset. If the clock signal is absent for the interface with AC coupling (as shown in Figure 8), oscillation may occur. A small offset between the CLK and nCLK pair can be introduced using equations (3) and (4). An example of this interface is shown in Figure 9.
Figure 7. General LVHSTL to Differential Input Interface

Figure 8. General LVHSTL Driver to Differential Input Interface with AC Coupling

R5, R6 locate near the driver pin.
Figure 9. LVHSTL Driver AC coupled to Differential Input Interface with a small DC offset between the CLK and nCLK to prevent oscillation.

Conclusion

The application note shows how the introduction of a small DC offset voltage between CLK and nCLK was used to prevent oscillation when the input clock signal is absent and the input is floating. Wider DC offset input voltage provides more margin to prevent oscillation. However, setting this DC offset too wide will increase the offset between the true and complementary input signals during normal operation. Board designers should consider these trade-offs when choosing the DC offset voltage.
IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers skilled in the art designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only for development of an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising out of your use of these resources. Renesas’ products are provided only subject to Renesas’ Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Rev.1.0 Mar 2020)

Corporate Headquarters
TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information
For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
www.renesas.com/contact/

Trademarks
Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

© 2020 Renesas Electronics Corporation. All rights reserved.