CLOCK DISTRIBUTION SIMPLIFIED WITH IDT GUARANTEED SKEW CLOCK DRIVERS

APPLICATION NOTE AN-82

By Michel Conrad

INTRODUCTION

In today's world of RISC or CISC microprocessor based systems there is an endless quest for cost effective solutions which offer the best system performance. Faster processors, increased integration and innovations in architecture have resulted in high performance systems which can be packed into smaller and smaller boxes. With processor clock frequencies migrating towards 33, 40 and 50Mhz, clock signals are becoming more and more critical. As the clock period gets shorter, the uncertainty or skew in the clock distribution system becomes more of a problem. Since clocks are used to drive the processors and to synchronize the transfer of data between system components the clock distribution system is an essential part of the system design. A clock distribution system design that does not take skew into consideration may result in a system with degraded performance and reliability.

Designing a clock distribution system which minimizes skew is not a trivial problem. To address this problem IDT has developed the IDT49FCT805 and IDT49FCT806 guaranteed skew clock drivers. These high-speed clock drivers have been designed to minimize skew, thus simplifying the problem of designing a reliable, minimum skew clock distribution system. This application note discusses the issues surrounding clock skew, clock drivers, and clock distribution. It will show how the IDT49FCT805 and IDT49FCT806 can be used to simplify the design of minimum skew clock distribution systems.

What Is Clock Skew?

The term clock skew is used to describe the timing differences between signals in a clock distribution system. The non-ideal characteristics of system components and their connecting circuitry result in uncertainties as to when clock signals trigger their loads. Figure 1 shows a generalized, multiple output clock driver and its associated timing for the low-to-high transition. A common signal drives each input resulting in "n" copies of that signal on the clock driver outputs. The clock skew is the difference in propagation delay between the driver's slowest output and its fastest output. Since output "n" has the minimum propagation delay and output "1" has the maximum propagation delay, the clock skew is the difference or tPLH1 - tPLHn.

In a typical system clock skew has two distinct sources. The first source of skew is the clock driver device itself. The clock driver is a piece of interface logic used to drive clock signal lines. With any given technology the clock driver is an inherent source of skew. In an ideal clock driver all the internal circuit elements of the device are perfectly matched so that propagation delays through equivalent paths are identical. In a practical clock driver there are many variables which can effect the propagation delay through equivalent paths and therefore contribute to skew. The layout and electrical characteristics of the circuit elements, the location of those elements relative to ground and VCC, as well as the parasitics of the package can

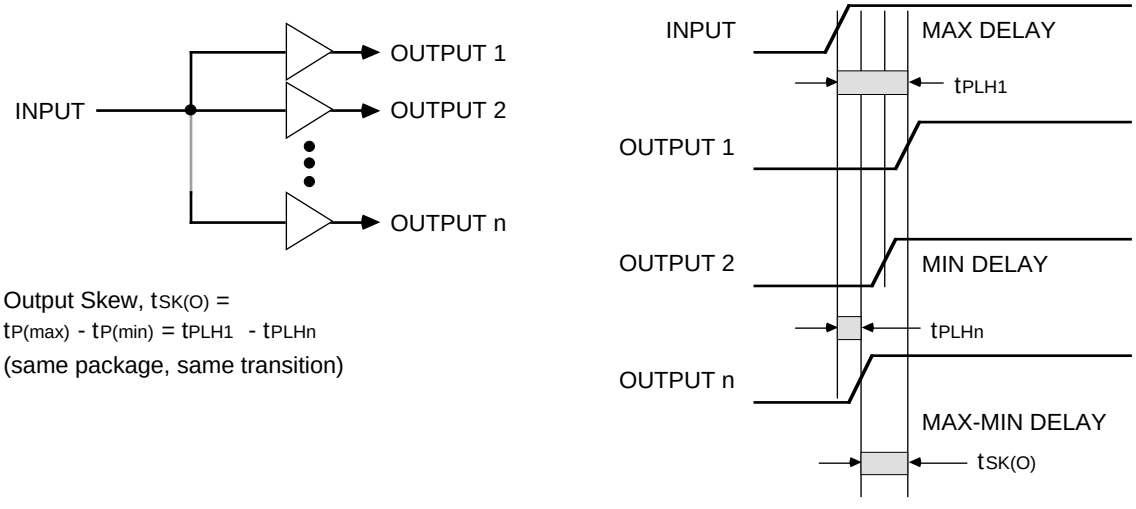


Figure 1. Output Skew tSK(O) Schematic and Timing Diagram

all have an effect on propagation delay. Many of these variables are dependant on manufacturing process parameters, which adds many more variables that can effect the skew characteristics of the device.

The second source of clock skew is the clock distribution system. How the clock driver device is incorporated into the clock distribution system is critical. The issues include the layout of signal lines, device loading, power supply connections and power supply decoupling. Operating conditions such as the power supply voltage and the ambient temperature also play a significant role. Because of the fast edge rates found in today's high speed logic, most PCB traces should be treated as transmission lines. If the design does not address the transmission line effects caused by the fast edge rates, the design may never work as intended.

THE CLOCK SKEW PROBLEM

Clock skew problems arise when the timing requirements of a system component are violated. Many of the common clocking bottlenecks can be categorized into two types of clock skew problems. The first is the synchronization problem caused by skew between multiple copies of a system clock. The second problem is that of meeting the duty cycle requirements of system components which require a controlled duty cycle.

A simple pipeline register can be used to illustrate the synchronization problem (Figure 2). The pipeline is composed of two registers and some clock circuitry. The clock circuit begins with a Master Clock which is buffered into two clock signals, CLK1 and CLK2. CLK1 drives Register X and CLK2 drives Register Y. The registers are configured to pass sequential data on each clock cycle so that the current output of Register Y is the previous cycle's output of Register X. The circuit's timing is shown in Figure 3.

In Figure 3-a the data sample "N" is the input to Register X and data "N-1" is the input to Register Y. For correct operation the input to each register must satisfy the setup and hold time requirements with respect to its clock. Since the output of Register X is the input to Register Y, the hold time tHy should not be greater than tPDx(min). In Figure 3-a CLK1 and CLK2 switch at the same time so that the output of Register X satisfies the setup and hold time requirements of the input to Register Y.

In Figure 3-b CLK2 is delayed relative to CLK1 resulting in a tSKEW between the two clocks. Now, for correct operation the hold time tHy should not be greater than tPDx(min)-tSKEW. As shown, the skew in CLK2 causes a violation of either the hold time requirement of data "N-1" or the setup time requirement of data "N" as input to Register Y. For correct operation data "N-1" must be clocked into Register Y and in Figure 3-b it is unclear whether data "N" or "N-1" is clocked into Register Y. If the timing margin tPDx(min)-tHy is about 2.5ns then a clock skew of 2.5ns or greater is a threat to the reliability of the system

Many microprocessor systems require that the clock have a controlled duty cycle. Guaranteeing a fixed duty-cycle at fast clock rates is difficult because propagation delays for opposite transitions in standard interface logic used for clock distribution are seldom identical. Also, timing differences between transitions do not scale with frequency. If a driver has 3.0ns of pulse skew (see definitions below) the tolerance of a 25ns cycle time (40Mhz) is ±12%. If the clock is pushed to 50Mhz, the tolerance grows to ±15%. A rule-of-thumb is that no more than 10% of the clock cycle be used for clock distribution. It is clear that if standard components are used the rule is easily violated at higher clock frequencies.

CLOCK SKEW DEFINITIONS

With the objective of minimizing skew inherent to the clock driver device, IDT has designed the IDT49FCT805 and IDT49FCT806 clock drivers. These clock drivers are designed to meet very tight skew specifications. The critical parameters are output skew, pulse skew, and package or part-to-part skew.

Output skew tSK(O) is the difference in propagation delay between any two outputs of the same device going through the same transition. This is the type of skew illustrated in

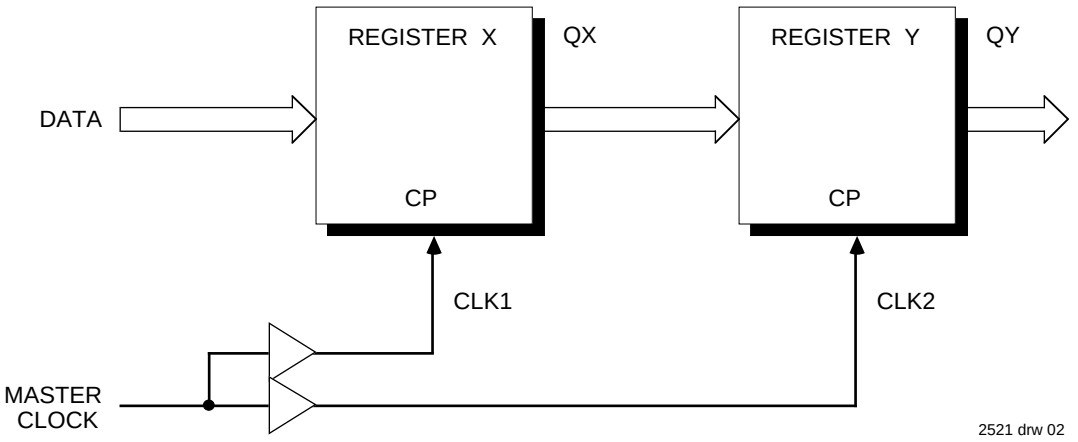


Figure 2. Schematic for a Two Register Pipeline

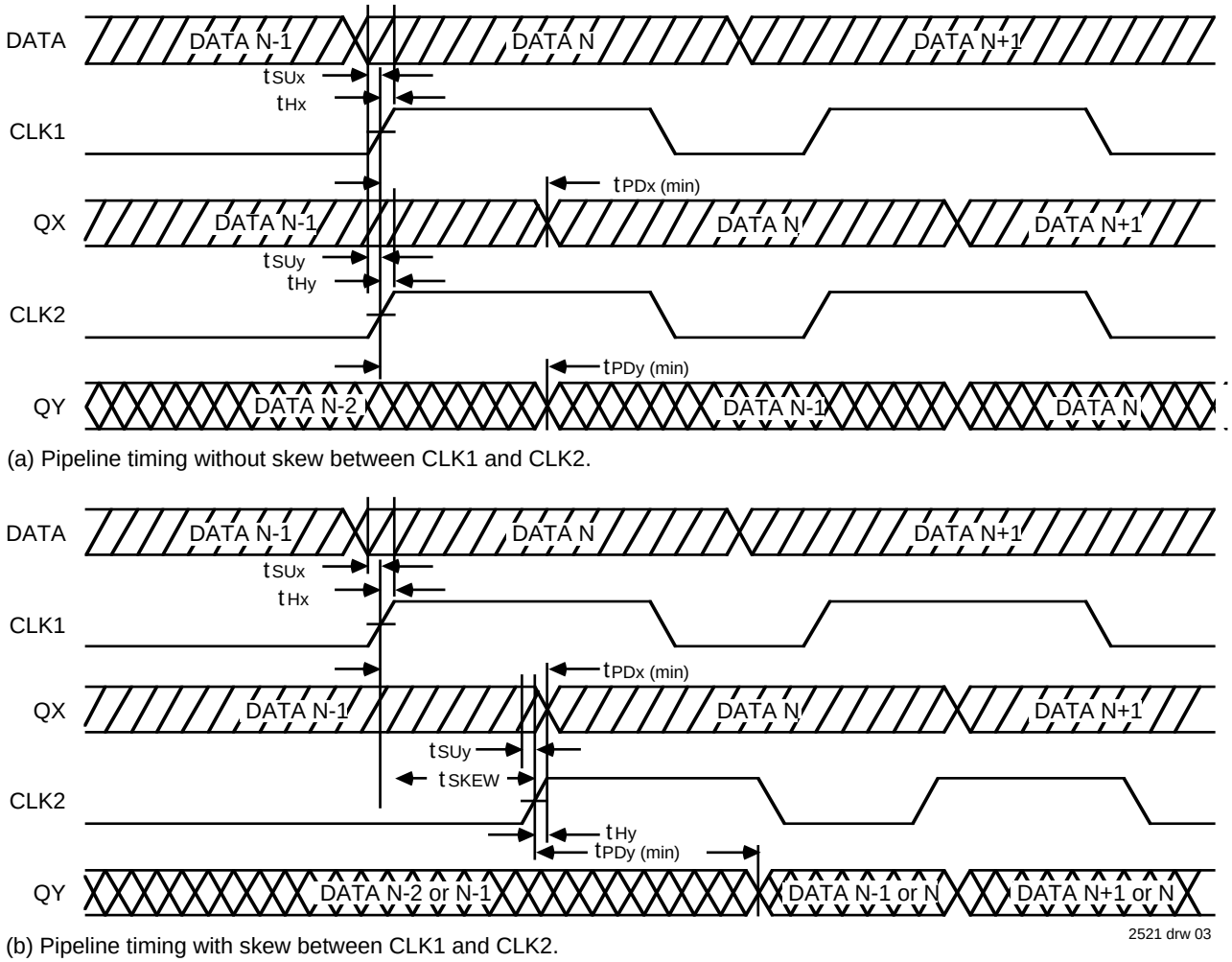


Figure 3. Timing Diagrams for Pipeline Register Example

Figure 1. If the propagation delay of the slowest output (tPLH1) is 5.0ns and the fastest output (tPLHn) is 3.0ns then the output skew is 2.0ns. The tSK(O) parameter applies to all the outputs of a single clock driver chip. It is measured separately for the high-to-low and low-to-high transitions. Figure 4 shows the measured output skew of several IDT49FCT805As for low-to-high and high-to-low transitions. Under typical conditions (VCC=5.0V, TEMP=25°C) the maximum skew is less than 450 picoseconds for both the low-to-high and high-to-low conditions. In the IDT49FCT805/806 data sheet this value is guaranteed to be less than 700 picoseconds over the commercial operating range.

Pulse skew tSK(P) is the difference in propagation delay for low-to-high and high-to-low transitions and is measured on a

49FCT805A OUTPUT SKEW VERSUS TEMPERATURE

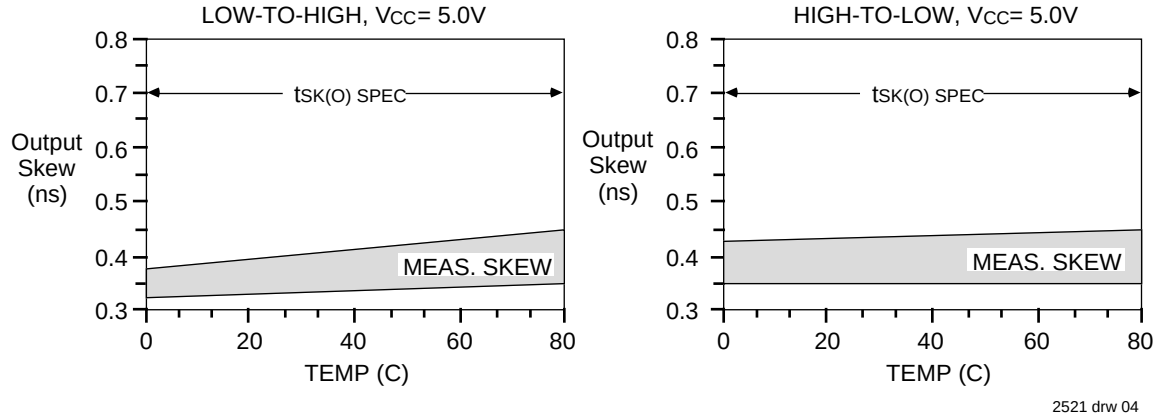
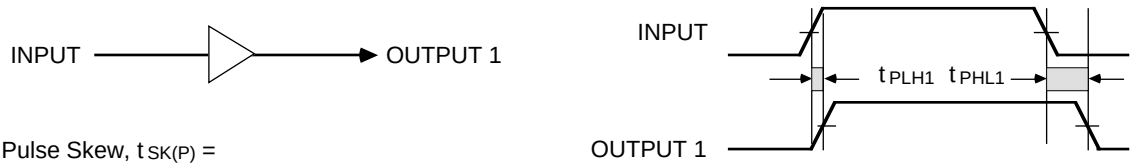


Figure 4. Measured Output Skew tSK(O) of Several IDT49FCT805As



Pulse Skew, $t_{SK(P)}$ =
$|t_{PLH} - t_{PHL}| = t_{PLH1} - t_{PHL1}$
(same output pin)

Pulse skew is the difference in propagation delays between the low-to-high and high-to-low transitions of a single output.

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Figure 5: Pulse Skew tSK(P) Schematic and Timing Diagram.

single output pin. In Figure 5, if tPLH1 is 5.5ns and tPHL1 is 4.0 ns, tSK(P) will be the the difference, or 1.5ns. Pulse skew is also a measure of the duty cycle distortion that the clock driver will contribute to an incoming clock signal. This is an important parameter for applications that use both edges of the clock and where a controlled duty cycle is required. Figure 6 shows the pulse skew measured on several IDT49FCT805As. Under typical conditions the measured pulse skew was less than 825 picoseconds. In the data sheet this value is guaranteed to be less than 1.0 nanosecond over the commercial operating range. For a 40Mhz clock with a period of 25ns, the IDT49FCT805/806 guarantees a maximum of 4% duty cycle distortion.

Part-to-part or package skew tSK(T) is similar to output skew. The difference is that it applies to outputs of two or more

49FCT805A PULSE SKEW VERSUS TEMPERATURE

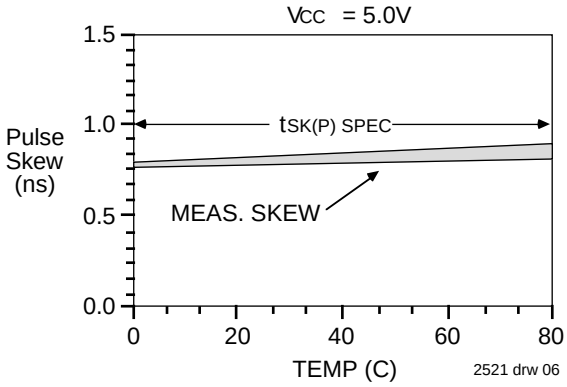
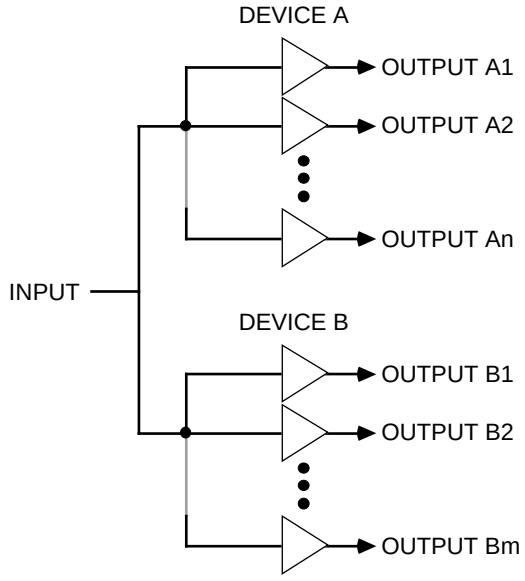
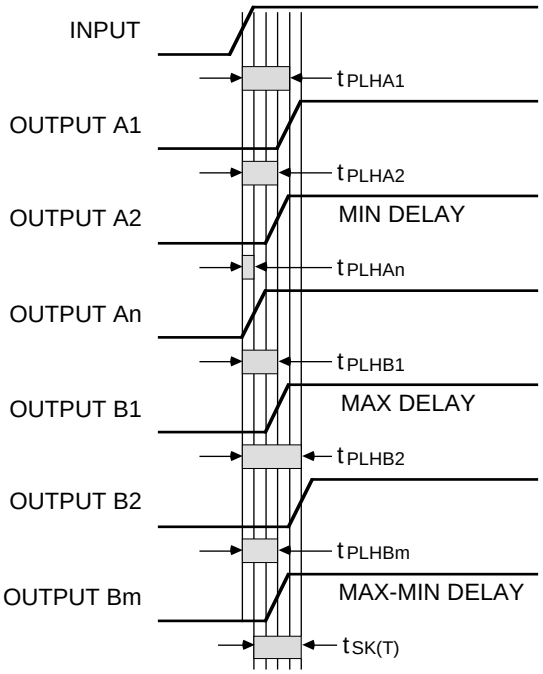


Figure 6. Measured Pulse Skew tSK(P) on Several IDT49FCT805As



Package Skew, $t_{SK(T)}$ =
$t_{P(max\ Device\ B)} - t_{P(min\ Device\ A)}$ =
$t_{PLHB2} - t_{PLHAn}$
(same transition, temperature, supply voltage, loading and package type)



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Package skew is the difference in propagation delay between the fastest and the slowest outputs of two or more devices for the same input and output transition.

Figure 7. Package Skew tSK(T) Schematic and Timing Diagram

devices. The timing diagram in Figure 7 illustrates the case where two generalized clock drivers are driven by a common input. The result is “n” outputs from device A and “m” outputs from device B making the same transition. The package skew is the difference in propagation delay between the slowest output of one device and the fastest output of the other device for the same transition. In this case the output An is the fastest output and the output B2 is the slowest If tPLHAn is 4.0ns and tPLHB2 is 6.0ns the package skew is 2.0ns. Certain conditions must be satisfied for the package skew specification to apply. The devices must have the same VCC, ambient temperature and be assembled in the same package type. Also each device must have equivalent loading and be of the same speed grade.

Part-to-part skew is difficult to specify because it implies that the characteristics every part ever sold will operate within a window of operation. The window of operation ensures that parts that run too fast or too slow do not get sold. Figure 8 shows the measured values of package skew on several IDT49FCT805As under typical conditions. The maximum measured package skew from this sample is 525 picoseconds. In the IDT49FCT805/806 data sheet this value is guaranteed to be less than 1.5 nanoseconds over the commercial operating range.

49FCT805A PACKAGE (PART-TO-PART) SKEW VERSUS TEMPERATURE

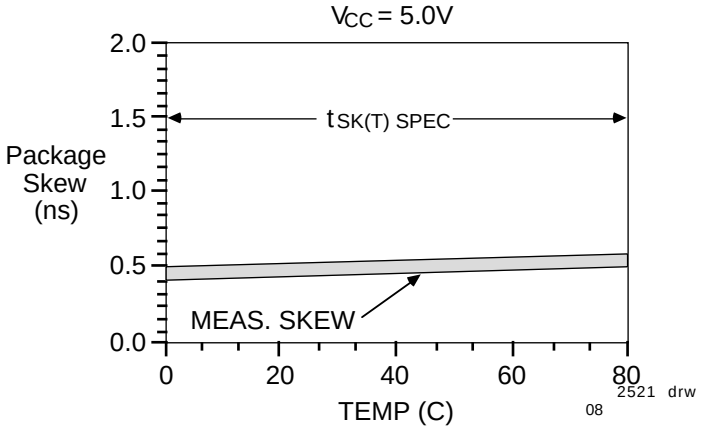


Figure 8. Measured Package Skew tSK(T) for Several IDT49FCT805As

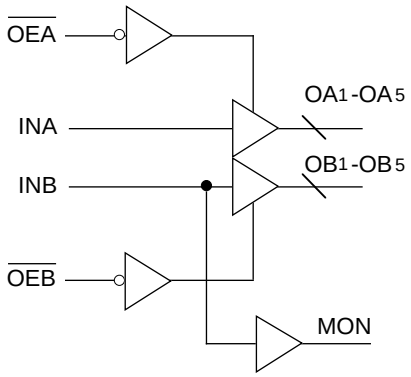
THE IDT49FCT805 & IDT49FCT806 CLOCK DRIVERS

The IDT49FCT805 and 49FCT806 are high-speed guaranteed skew clock driver chips specifically designed to meet the clocking requirements of today’s high-performance systems. The logic diagram and pin configuration of the IDT49FCT805 are given in Figure 9. The IDT49FCT806 is the inverting option of IDT49FCT805.

Skew in the IDT49FCT805/806 is minimized throughout the design process. Careful circuit design and layout in silicon have resulted in a pin configuration that is specifically designed for very low output and pulse skew. Independent power and ground pins reduce the amount of ground bounce and dynamic threshold shift caused by multiple outputs switching. The 1:5 input to output ratio reduces the amount of capacitive loading on the previous stage which simplifies termination and reduces component count when compared to conventional solutions. The devices are optimized for both PDIP and SOIC packages.

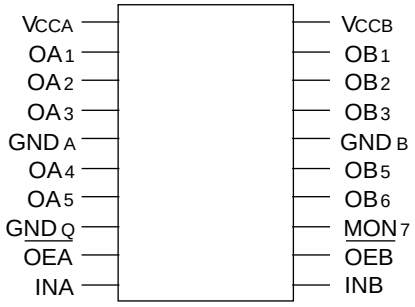
The IDT49FCT805/806 clock drivers consist of two independent banks of drivers. Each bank drives five output buffers from a single standard TTL compatible CMOS input. The input has 200mV of hysteresis for increased immunity to system noise. Independent active low output enable pins ($\overline{OEA}$ and $\overline{OEB}$) control each of the banks, allowing for independent control of the outputs. This feature may be used in applications where clock bussing or a power savings mode is required. The input INB drives the B bank as well as an output called MON (Monitor). The MON output is not controlled by $\overline{OEB}$ and therefore runs continuously. The MON signal can be used for priming phase locked loops or driving diagnostic hardware.

Each IDT49FCT805/806 has 3 ground pins and 2 VCC pins. The ground pins, GNDA and GNDB, are located in the middle of the package to minimize inductance in the ground return path. The two grounds are returns for the A and B bank output buffer and pre-driver currents. The third ground pin, GNDQ (Quiet Ground), provides a ground return for the remaining circuitry. The ground pin arrangement reduces ground bounce on the outputs and noise on the thresholds of the internal logic. Since GNDA and GNDB are completely



LOGIC DIAGRAM

20 - PIN DIP OR SOIC



PIN CONFIGURATION

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Figure 9. Logic Diagram and Pinout of the IDT49FCT805

isolated from each other on the die, switching effects on one bank will have minimal effects on the other bank. The independent VCC pins, VCCA and VCCB, supply power to the two banks.

Each output of the IDT49FCT805/806 clock driver features a high current drive output buffer. These outputs can be used to drive both TTL and CMOS loads. With a typical Vol of 0.3 volts the buffer can sink 64mA. For a typical Voh of 3.8 volts the output buffer can source 24mA. These output buffers are optimized around the 1.5 volts switching threshold which is the standard for TTL compatible logic. These output buffers can easily meet the edge rate requirements of today's microprocessors and peripheral components. Typical edge rates for the IDT49FCT805A are 1.0 volt/nanosecond for risetime and 2.0 volt/nanosecond for falltime

WORKING WITH THE DATA SHEET

In the past, designers have used the minimum and maximum limits of a clock driver's propagation delay specifications to determine skew in their designs. With the IDT74FCT244A (tPHL min=1.5ns and tPHL max=4.8 ns) the difference between the two limits results in a 3.3ns window. With the IDT49FCT805/806, subtracting the minimum from the maximum limit is no longer necessary because the skew is specified in the data sheet. However, because the IDT49FCT805/806 data sheet still specifies a 1.5ns minimum for propagation delay there may be some confusion as to whether or not the skew specifications are real. In the following discussion it will be shown that meeting the skew specifications is not a problem for IDT49FCT805.

The Switching Characteristics (Table 1) for the FCT805A/806A show the maximum propagation delay (tPLH/HL) to be 5.8 ns and the minimum propagation delay to be 1.5ns. If the skew is calculated by subtracting the minimum delay from the maximum delay the result is a number much larger than the tSK(O) spec of 700ps. How can IDT guarantee a 700ps output skew number and still have such a wide range of minimum and maximum propagation delay values?

The range of values between the minimum and maximum propagation delay reflects the wide range of conditions under which the part must operate and the range of manufacturing process parameters. Consider a part that under typical conditions has a median propagation delay of 5.0ns. According to the tSK(O) specification of 700ps, each output of that driver will switch within a 5.0±0.35 ns window. If the median propagation delay drops to 4.0ns, due to variations in VCC or temperature, the specification guarantees that each output will then switch within a 4.0±0.35ns window. In the unlikely event that the operating conditions cause the median delay to drop to 1.85ns, then all outputs will switch within a 1.85±0.35ns window. It is important to recognize that all the devices are assumed to be operating under the same conditions. If one part is running fast because of cold temperature and high VCC, all the other parts will be running fast as well. The following data is provided to show that the IDT49FCT805A does indeed meet its skew specifications over the commercial operating range.

Figure 10 shows the range of output skew measurements for low-to-high and high-to-low transitions with VCCs of 4.75 and 5.25 volts. For both low-to-high and high-to-low transi-

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Conditions [1]	IDT49FCT805/806 Com'l. Min.[2]	IDT49FCT805/806 Com'l. Max.	IDT49FCT805A/806A Com'l. Min.[2]	IDT49FCT805A/806A Com'l. Max.	Unit
t_{PLH} t_{PHL}	Propagation Delay IN_A to OA_n, IN_B to OB_n	C_L = 50pF R_L = 500Ω	1.5	6.5	1.5	5.8	ns
t_{PZL} t_{PZH}	Output Enable Time OE_A to OA_n, OE_B to OB_n		1.5	8.0	1.5	8.0	ns
t_{PLZ} t_{PHZ}	Output Disable Time OE_A to OA_n, OE_B to OB_n		1.5	7.0	1.5	7.0	ns
$t_{SK(O)}$[3]	Skew between two outputs of same package (same transition)		—	0.7	—	0.7	ns
$t_{SK(P)}$[3]	Skew between opposite transitions (t_{PHL}-t_{PLH}) of same output		—	1.0	—	1.0	ns
$t_{SK(T)}$[3]	Skew between two outputs of different package at same power supply voltage and temperature (same transition)		—	1.5	—	1.5	ns

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays
3. Skew guaranteed across temperature range but measured at maximum temparature only. Skew parameters apply to propagation delays only.

Table 1. IDT49FCT805/806 Switching Characteristics

49FCT805A OUTPUT SKEW VERSUS TEMPERATURE

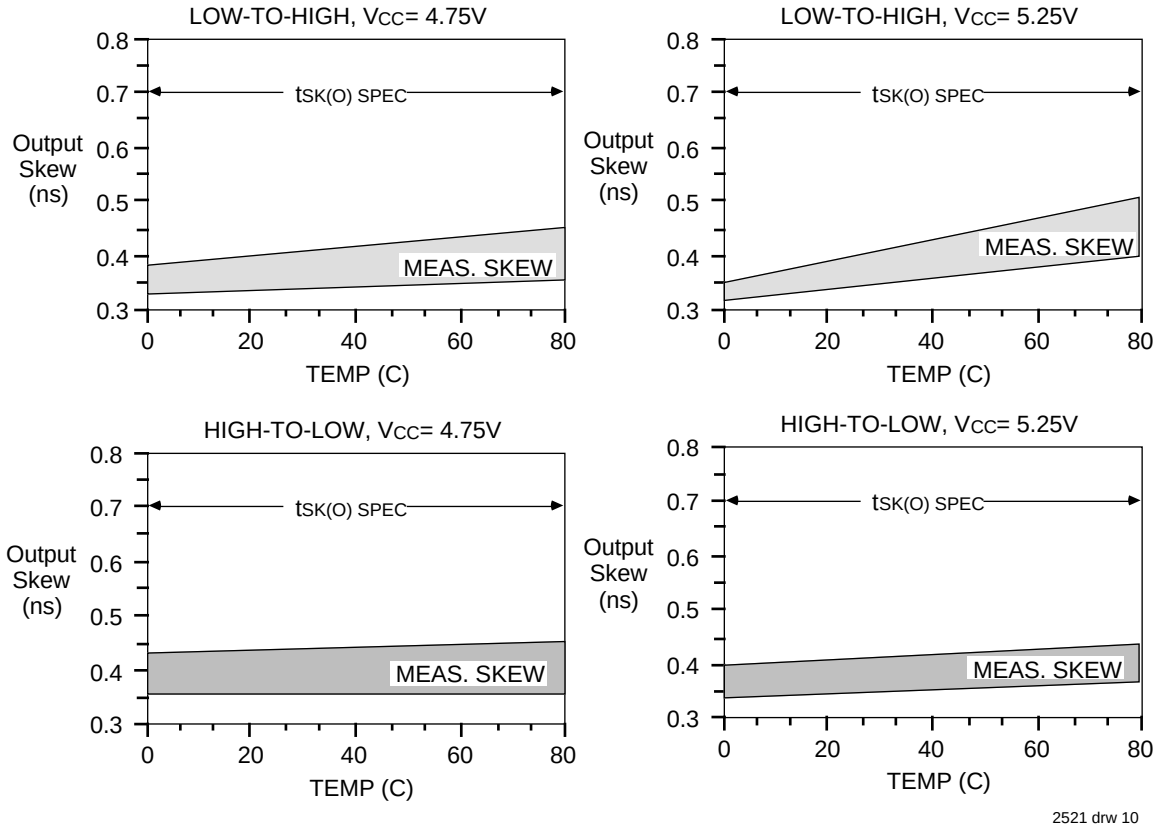

Figure 10. Measured Output Skew tSK(O) for Several IDT49FCT805As over the Operating Range

tions, the graphs show that output skew is maximum at hot temperature (70°C). In each case the skew is well below the data sheet specification of 700ps.

Figure 11 shows the range of pulse skew measurements with VCCs of 4.75 and 5.25 volts. The measured pulse skew peaks at hot temperature and is slightly greater for a VCC of 4.75V. The measured performance is safely within the data sheet specification of 1.0ns.

Figure 12 shows the range of package skew measurements for low-to-high and high-to-low transitions with VCCs of 4.75 and 5.25 volts. For both low-to-high and high-to-low transitions the skew peaks at hot temperature with minimal differences between low and high VCC. Again the measured performance easily meets the data sheet specification of 1.5ns.

49FCT805A PULSE SKEW VERSUS TEMPERATURE

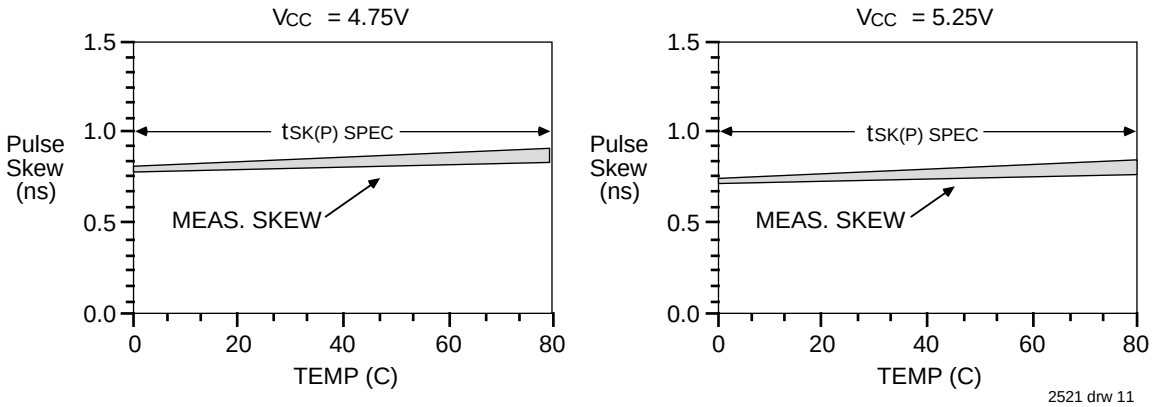

Figure 11. Measured Pulse Skew tSK(P) for Several IDT49FCT805As over the Operating Range

CLOCK DISTRIBUTION SIMPLIFIED

To show how easy it is to design with the IDT49FCT805, consider a hypothetical clock distribution system. The system has a 50Mhz clock source and must drive 75 loads. Each load is a CMOS input connected by 70Ω micro-strip trace at a density of 1 load every 0.5 inches. Assume that all the inputs are positive edge triggered and the objective is to minimize skew.

One approach would be to drive all 75 inputs with a single clock driver output (Figure 13). There are many problems with this approach. The first problem is the large amount capacitance associated with 75 CMOS inputs. Assuming 10pF maximum of capacitance per CMOS input, the total capacitive load is 750pF. A standard clock driver such as the IDT74FCT244A has ΔtPLH of 2ns/100pF for loads above 50pF. If the IDT74FCT244A is used the capacitance alone adds up to 14ns of additional propagation delay. If 75 loads are distributed along a single trace, the trace length is 38 inches (75 X 0.5 inputs/inch). If the PCB trace has an intrinsic delay of 0.15ns/inch (1), the delay from point B to point C is 5.7ns (38" X 0.15 ns/inch). Using a loaded trace delay of 0.37ns/inch (1), the skew between the ends of the trace approaches 15ns (38" X 0.37ns/inch). Given a 20ns cycle time (40 MHz), 14ns of clock skew implies that 70% of the clock cycle is given to clock distribution.

A second approach is the clock tree shown in Figure 14. By adding a level of buffers between the clock source and the 75 loads, the capacitive loading on the buffer outputs is reduced from 750pF to 50pF and the amount of PCB trace associated with each driver is reduced to 2.5". If IDT74FCT244As are used at least three packages (8 drivers per package) will be required. Since the 244's do not specify skew the designer might assume that each device output will switch within a 3.3ns window (tPHLmax-tPHLmin= 4.8ns -1.5ns). If the output transitions at points B, C, and D occur within a 3.3ns window, then the outputs of the second level (point E) may occur within a 6.6ns window. Assuming a 20ns cycle time (50Mhz) the designer has lost 33% of the cycle time to clock distribution without even considering transmission line effects.

A third approach is to use IDT49FCT805As as shown in Figure 15. Since each group of six buffers in Figure 14 can be

49FCT805A PACKAGE (PART-TO-PART) SKEW VERSUS TEMPERATURE

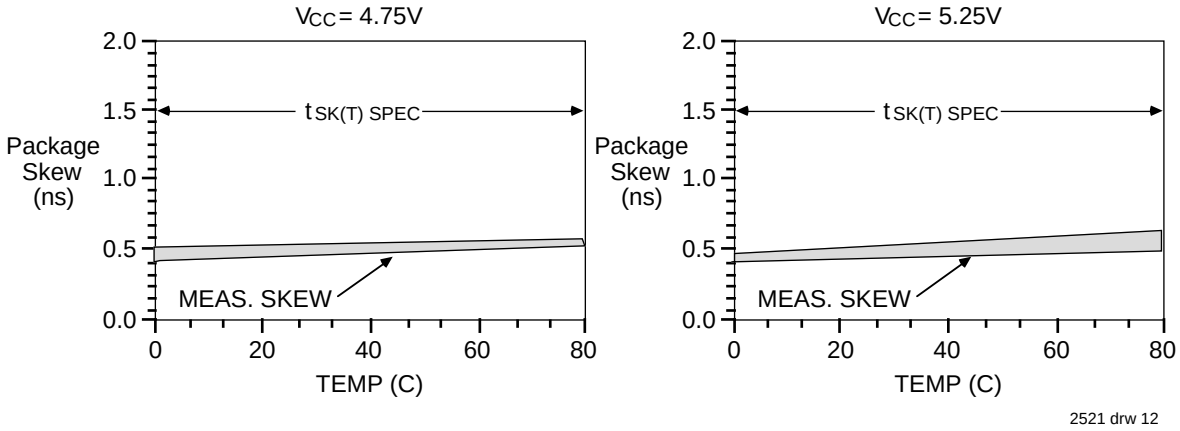

Figure 12. Measured Output Skew tSK(T) for Several IDT49FCT805As over the Operating Range

CLOCK DISTRIBUTION SYSTEM FOR 75 LOADS - SINGLE DRIVER CONFIGURATION -

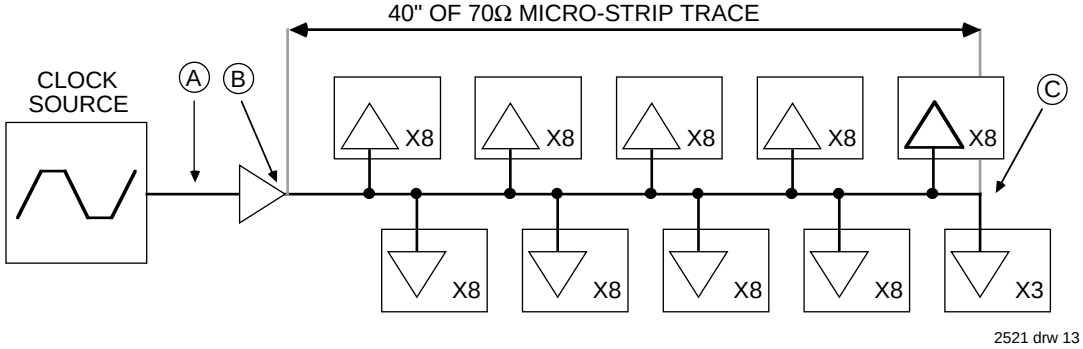

Figure 13. Single Driver Clock Distribution System

CLOCK DISTRIBUTION SYSTEM FOR 75 LOADS
- CLOCK DRIVER TREE CONFIGURATION -

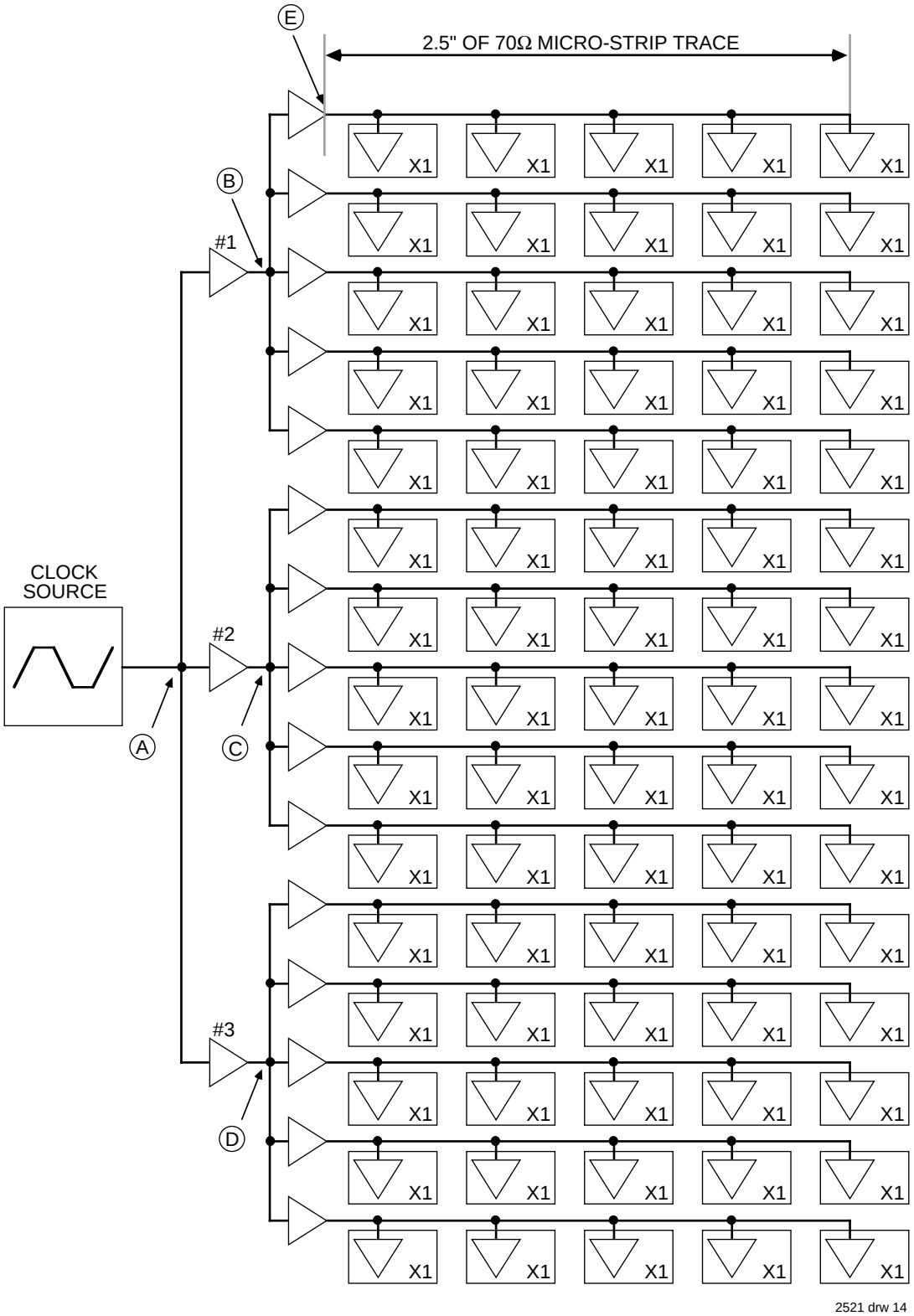

Figure 14. Clock Tree Distribution System Using 244's

CLOCK DISTRIBUTION SYSTEM FOR 75 LOADS
- CLOCK DRIVER TREE CONFIGURATION -

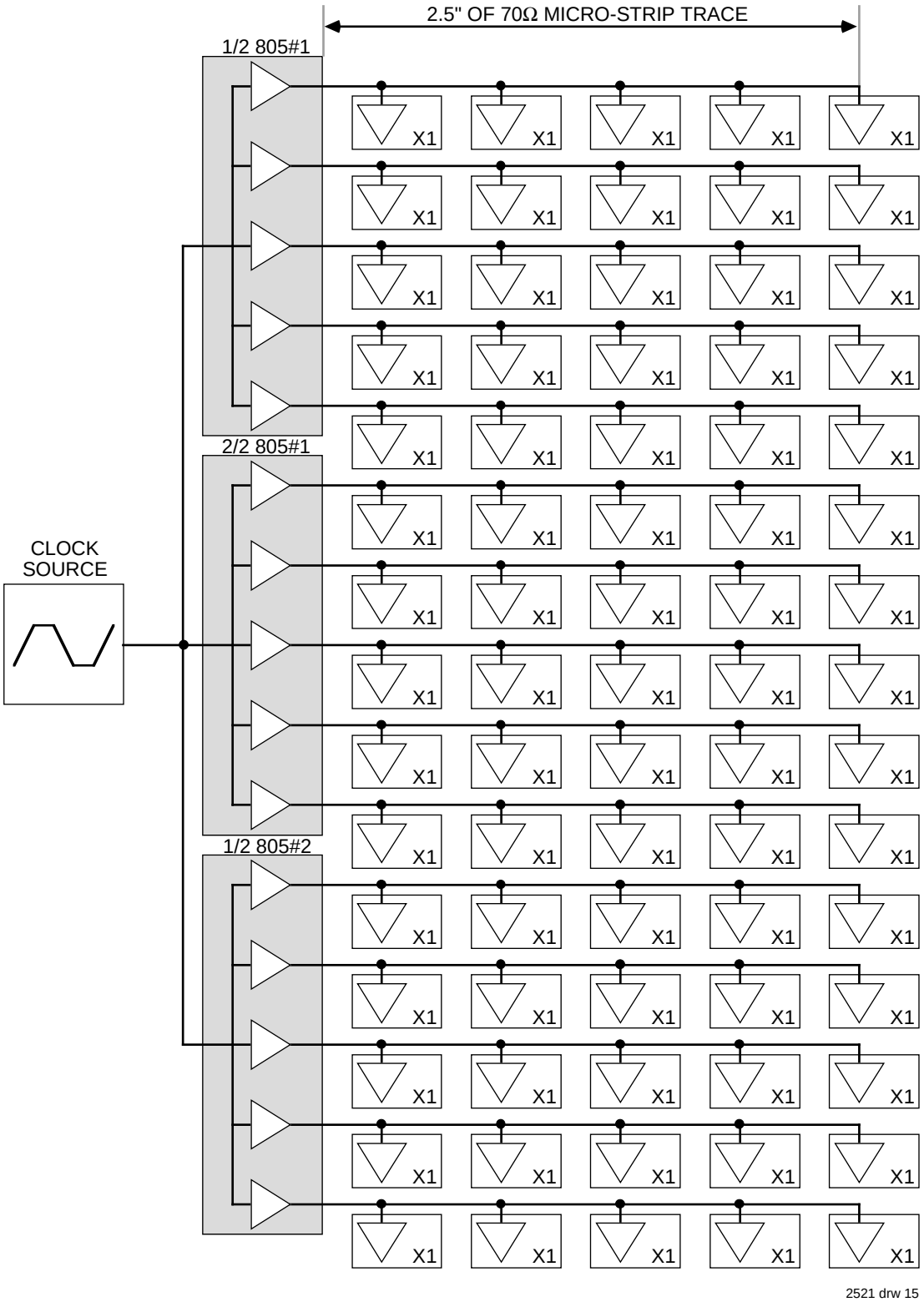

Figure 15. Clock Tree Distribution System Using IDT49FCT805's

replaced by 1/2 of an IDT49FCT805, only two devices are required to implement the design. Using the 1.5ns package skew specification reduces the 6.6ns skew window to a 1.5ns skew window. If 0.925ns of loaded trace delay (2.5" X 0.37 ns/inch) is considered the maximum skew is 2.425ns including a 1st order treatment of transmission line effects. For a 20ns cycle time, the penalty imposed by the clock distribution system is reduced to 12% of the cycle time including transmission line effects. Besides reducing the size of the skew window of the second approach by 77%, the IDT49FCT805 increases the level of integration associated with the clock distribution tree. A significant benefit is the reduced loading on previous stages. Reduced loading helps minimize skew and makes the termination of clock lines clean and simple. The reduced chip count also saves valuable board space and simplifies the layout of the board.

SUMMARY

The following features of the IDT49FCT805/806 address clock driver skew and clock distribution problems:

- Circuit design, chip layout, and pin configuration specifically designed for very low output, pulse and package skew.
- Independent power and ground pins for reduced ground bounce and dynamic threshold shift.
- High current drive capability for driving heavily loaded/terminated PCB traces.
- 1:5 input/output ratio for reduced loading on previous stages.
- 11 outputs reduce the need for additional drivers—saves board space and simplifies PCB layout.
- Multiple grounds and VCCs to minimize ground bounce effects on propagation delay and skew.
- Input Hysteresis for increased immunity to system noise.
- Available in SOICs for increased packing density and reduced lead inductance.

RECOMMENDATIONS

To realize the performance benefits offered by the IDT49FCT805/806 clock drivers, IDT recommends the following high speed design practices:

- Use low impedance power and ground planes.
- Keep loading balanced and light.
- Keep trace lengths short, avoiding sharp bends and discontinuities (eg. use two 45° bends vs one 90° bend).
- Decouple both VCC pins with a combination of capacitors (0.1μF and 0.01μF or 0.005μF) for effective high frequency filtering.
- Use termination for signal lines longer than 3 inches.
- Only use parts of same speed grade (non-A or A speed).

CONCLUSIONS

Clock skew is an important design consideration in today's high-speed systems. For successful and reliable operation, the clock skew must be kept within an acceptably small fraction of the system clock period. The IDT49FCT805 and IDT49FCT806 simplify the design of minimum skew clock distribution networks by specifying guaranteed low-skew performance. The skew specifications allow system designers to control the clock skew at each stage of the design which simplifies the problem of meeting global system requirements. With the IDT49FCT805/806 clock driver and a design methodology that pays close attention to high-speed design issues, maximum system performance can be achieved without risking reliability.

REFERENCES

[1] Application Note AN-49, High-Speed CMOS Logic Design Guide, Integrated Device Technology Corp., November 1989.

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