

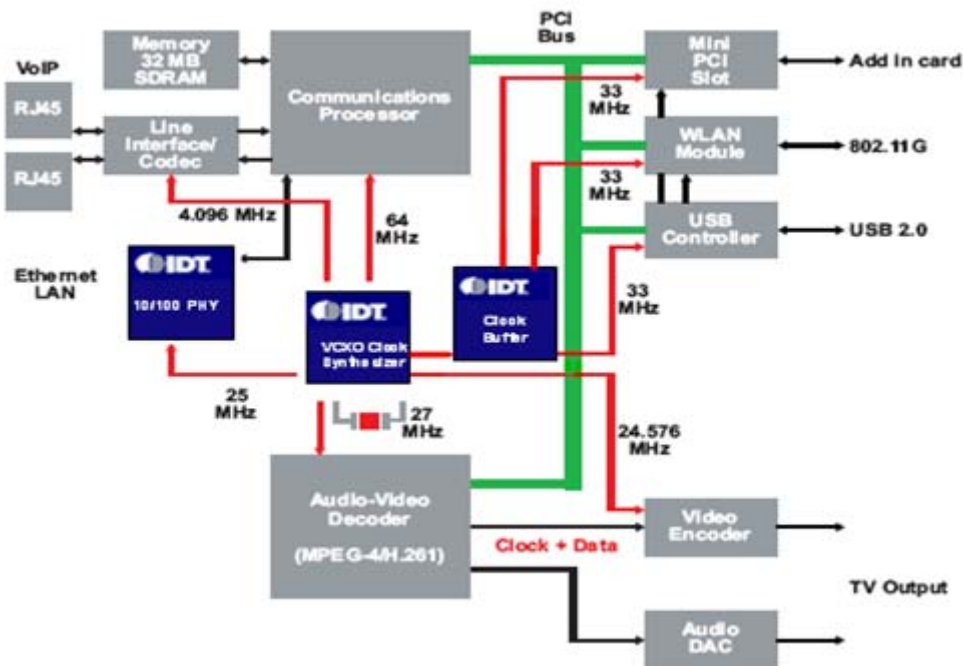
Introduction

High performance clock buffers are widely used in digital consumer and communications applications for distribution of clock signals. A critical parameter for these buffers is additive phase noise that can degrade system performance and reliability. This application note briefly explains the theory behind measuring additive phase noise for IDT clock buffers and summarizes the additive phase jitter results for several widely used IDT clock buffers. Other AC parameters of interest for buffers are input to output propagation delay and output to output skew.

In synchronous systems where timing and performance of the system is dependent on the clock, integrity of the clock signal is important. Designers must optimize board layout, use clean power supplies and follow recommended decoupling and termination schemes for the outputs in order to meet the EMI and timing budgets for their application.

IDT has a large variety of low skew clock distribution devices to meet all your application needs. Figure 1 shows a typical set top box application where an IDT clock buffer is used to distribute 33MHz PCI clocks to multiple PCI slots.

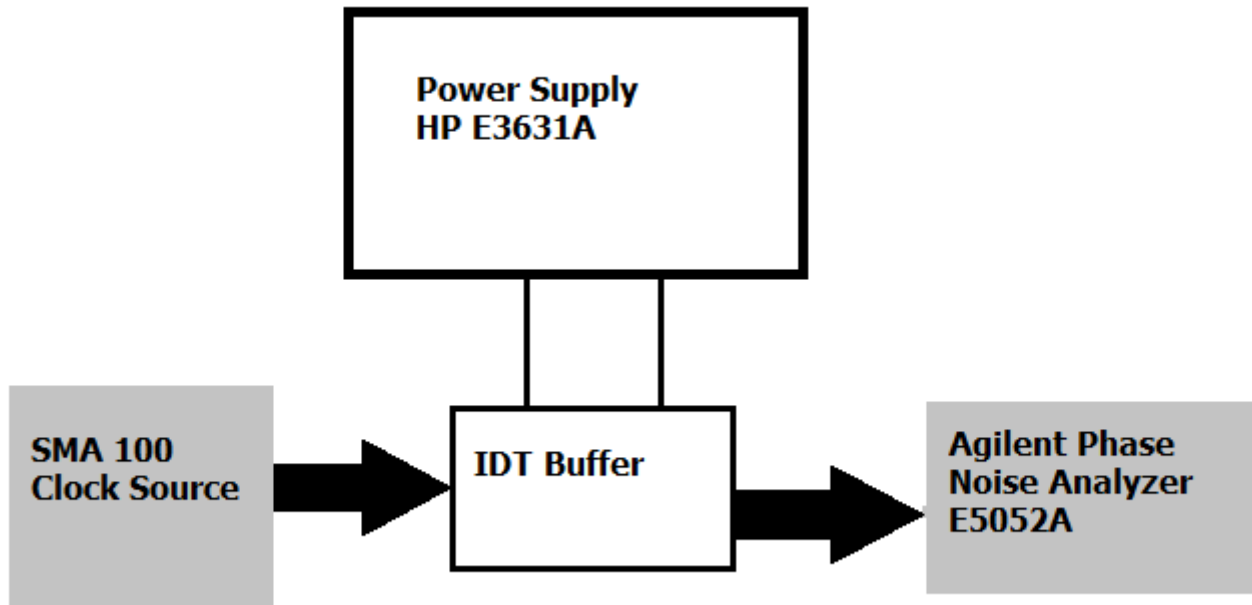
Figure 1. Set Top Box Application Diagram Using an IDT Clock Buffer



Phase Noise Measurement

The Agilent 5052A Phase Noise analyzer is used to take phase noise plots and the RMS jitter is calculated over an offset range for a center carrier frequency.

Figure 2. Test Setup for Additive Jitter Measurements



Additive Phase Noise

Any component in a signal chain has some amount of noise at its output that is generated internally (not including the contribution due to the external reference noise at the input). It is useful to measure the phase noise at the output of a device in such a way that the phase noise of any external source is canceled out. The phase noise so measured is specified as the additive phase noise of the device. It is the amount of phase noise that the device (clock buffer in our case) adds to the signal chain. IDT clock buffers have ultra low additive phase jitter thereby allowing system designers to distribute multiple copies of a clean clock to other devices on their system. The clock signal integrity is maintained thereby eliminating the need for additional jitter cleaning components. By considering the phase noise contribution due to the buffer alone, it is then possible to foretell the degree to which the buffer impacts the total system phase noise when used in conjunction with components such as oscillators and clock sources, each of which contribute to the phase noise of the total system. In many cases, the phase noise of one element in the chain dominates the system phase noise.

Additive Jitter

Additive jitter is defined as the added amount of jitter to the input signal caused by the device itself and can be calculated as:

$$\text{Total Additive Jitter} = \text{sq root} ((\text{output clock jitter})^2 - (\text{input clock rms jitter})^2)$$

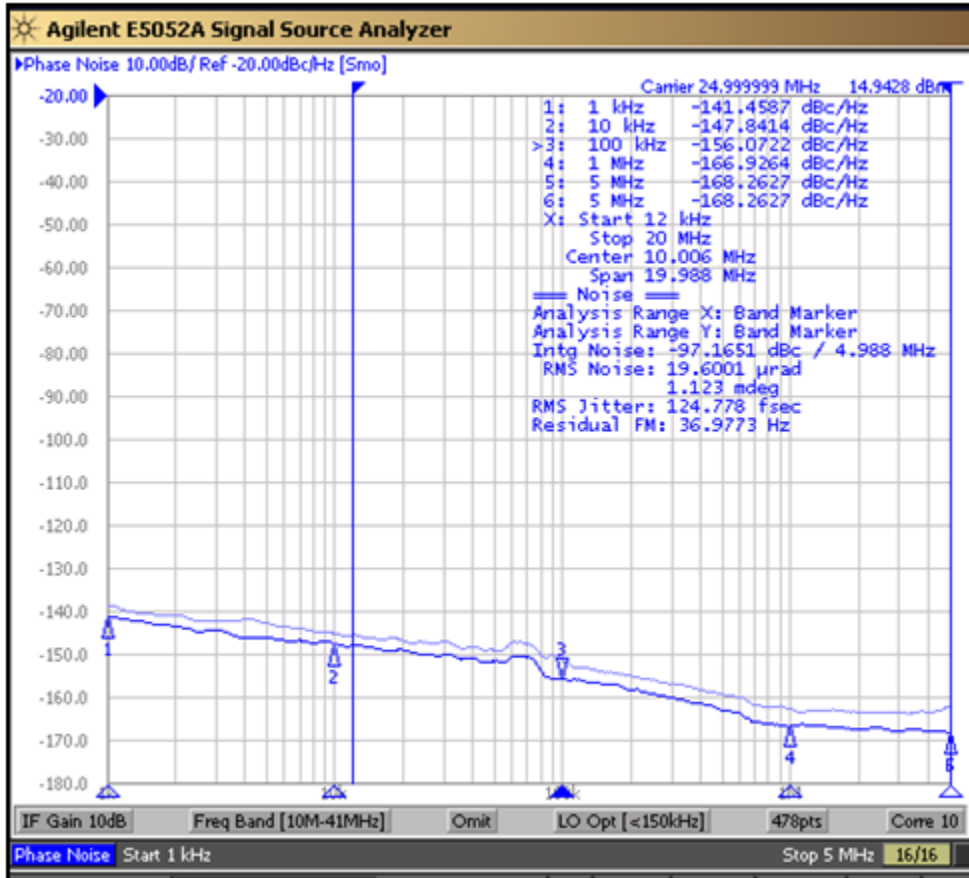
It assumes that the noise processes are random and the input noise is not correlated to the output noise. Additive jitter must be measured with a clock source where phase noise is below the noise floor of the buffer itself.

The input clock reference source used for phase jitter measurements is a SMA100A clock generator which is very low phase noise. The measured phase noise of the input clock to the IDT buffers used varies over frequencies. Below are phase noise measurements of frequency equal to 25MHz. The RMS jitter is measurement over the offset range of 12kHz to 20MHz. The average phase noise RMS Jitter measured on the SMA clock source is 80fs. We will use this value for our calculations of additive jitter in this applications note. This value represents the input clock RMS Jitter for the below formula.

Additive Phase Noise Results

Measurements for Additive Phase Noise were taken on five of the most commonly used IDT Clock Buffers at three frequencies: 25MHz, 100MHz and 125MHz. All measurements contained in this report were taken at room temperature and at the nominal voltage.

Figure 3. Phase Noise on ICS553 25MHz Clock Output and 25MHz Input Clock Source



Summary of Additive Jitter Results

The additive phase noise measurement results presented in this application note confirm ultra low additive phase jitter across IDT’s family of clock buffers. The additive phase jitter varies minimally over the buffer input frequency range and operating voltage range. All measurement data is in femto seconds (fs).

Table 1. Summary of Additive Jitter on Commonly Used IDT Clock Buffers

MHz	Range	IDT2305NZ	ICS551	ICS553	IDT74FCT3807	IDT5T30533
25	12kHz–20MHz	120.11	101.07	89.87	312.50	404.54
100	12kHz–20MHz	53.23	76.51	48.37	82.53	52.84
125	12kHz–20MHz	69.23	87.11	55.38	267.24	176.09

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.