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RENESAS

Application Note

Triplex LCD Driver Using General Purpose Ports of µPD7801x

Document No. U17107EE1V0AN00
Date Published April 2004

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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Chapter 1 Features

1.1 Introduction

There are a lot of applications existing, only a small display is necessary.
The connection of a “Static” display type is very easy, because there are only two voltage levels (V_{DD} & V_{SS}) to control as well on common as on segments lines.
But for a multiplexed display type (“Duplex” or “Triplex”) several intermediate voltage levels have to be controlled.
Hereafter the control of a “Triplex” LCD module is described using the µPD78P014. This application note is adaptable to all devices out of the µCOM 78K0 family.

1.2 Differences to a common LCD Controller/Driver

1. The different LCD-Voltage levels, needed for the common lines of an Triplex-LCD Display are generated using external resistor networks and the tri-state function of the µPD78P014 port structure. This gives a disadvantage of 4 resistors against a similar solution using a common LCD controller/ driver product like the NEC µPD7225.

2. Using a common LCD Controller/Driver the LCD voltage can be vary over a wide range and can be adopted easy to the LCD display. In the solution described hereafter the LCD-Voltage is fixed to the VDD level of the general purpose CPU.

[MEMO]

Chapter 2 Hardware Realisation

2.1 Pin/Segment Organisation for a 9 × 3 Segment Triplex LCD-Display

In the table below the connection of an 9 × 3 Triplex-Mode LCD display to port pins of the µPD78P014 are listed:

Table 2-1: Pin/Segment Organisation

PORT / PIN	SEGMENT	Description
P5.0 / Pin 26	S0	Segment Line 0
P5.1 / Pin 27	S1	Segment Line 1
P5.2 / Pin 28	S2	Segment Line 2
P5.3 / Pin 29	S3	Segment Line 3
P5.4 / Pin 30	S4	Segment Line 4
P5.5 / Pin 31	S5	Segment Line 5
P5.6 / Pin 33	S6	Segment Line 6
P5.7 / Pin 34	S7	Segment Line 7
P6.7 / Pin 42	S8	Segment Line 8
P6.4 / Pin 39	COM1 (C1)	COMMON Line 1
P6.5 / Pin 40	COM2 (C2)	COMMON Line 2
P6.6 / Pin 41	COM3 (C3)	COMMON Line 3

2.1.1 Relation LCD-Segments and Display-RAM of CPU

Table 2-2: Relation LCD-Segments and Display-RAM of CPU

SEGMENT	COM1 (C1)	COM2 (C2)	COM3 (C3)
S0	FADA.0	FADC.0	FADE.0
S1	FADA.1	FADC.1	FADE.1
S2	FADA.2	FADC.2	FADE.2
S3	FADA.3	FADC.3	FADE.3
S4	FADA.4	FADC.4	FADE.4
S5	FADA.5	FADC.5	FADE.5
S6	FADA.6	FADC.6	FADE.6
S7	FADA.7	FADC.7	FADE.7
S8	FADB.0	FADD.0	FADF.0

2.1.2 Segment example for an LCD-Glass

Table 2-3: Segment Example for an LCD-Glass

Address	BIT0	BIT1	BIT2	BIT3	BIT4	BIT5	BIT6	BIT7
FADA	S0-C1 **(2A)**	S1-C1 **(1B)**	S2-C1 **(2B)**	S3-C1 **(unused)**	S4-C1 **(3A)**	S5-C1 **(4A)**	S6-C1 **(4F)**	S7-C1 **(unused)**
FADB	S8-C1 **(3B)**							
FADC	S0-C2 **(2F)**	S1-C2 **(1ADEG)**	S2-C2 **(2G)**	S3-C2 **(2C)**	S4-C2 **(3F)**	S5-C2 **(4B)**	S6-C2 **(4G)**	S7-C2 **(3C)**
FADD	S8-C2 **(3G)**							
FADE	S0-C3 **(2E)**	S1-C3 **(1C)**	S2-C3 **(2D)**	S3-C3 **(P1)**	S4-C3 **(3E)**	S5-C3 **(4C)**	S6-C3 **(4D)**	S7-C3 **(4E)**
FADF	S8-C3 **(3D)**							

Figure 2-1: Principle Circuit Diagram

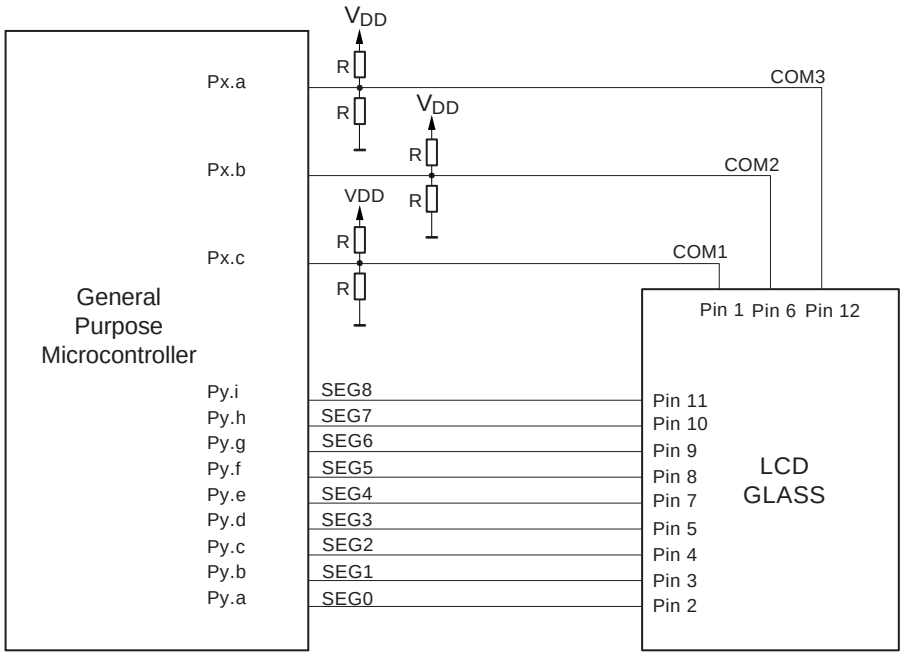
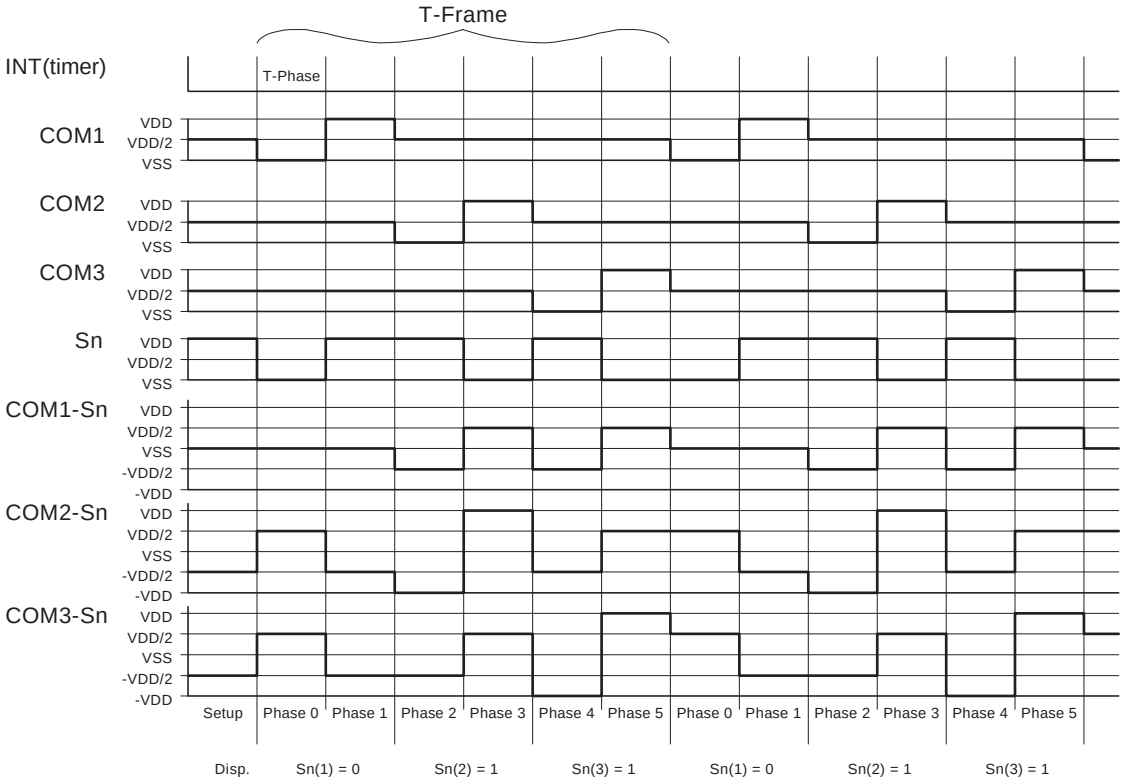


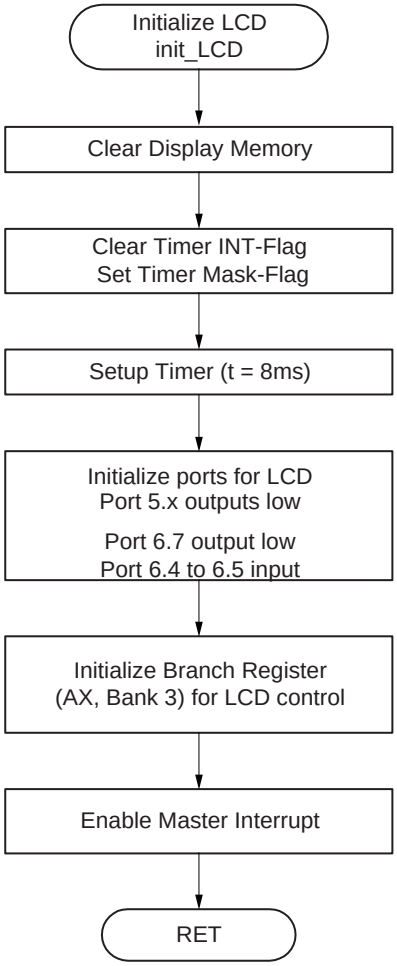
Figure 2-2: Timing Example



Chapter 3 Program Flowcharts

3.1 Initialisation

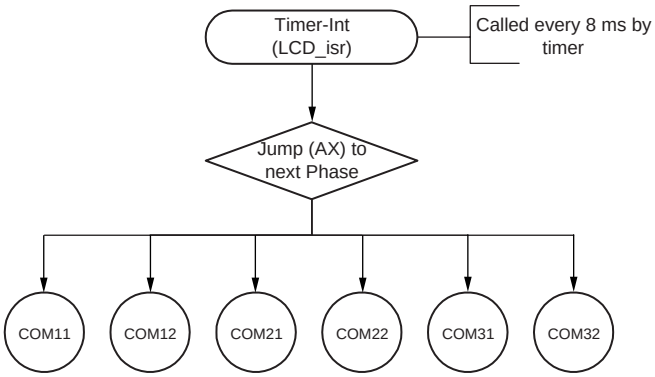
Figure 3-1: Initialisation Flow



3.2 Interrupt-Handler

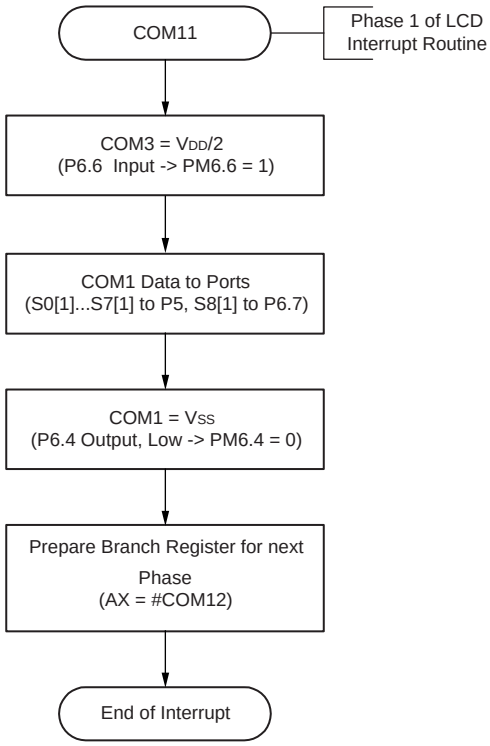
3.2.1 Dispatcher

Figure 3-2: Dispatcher Flow



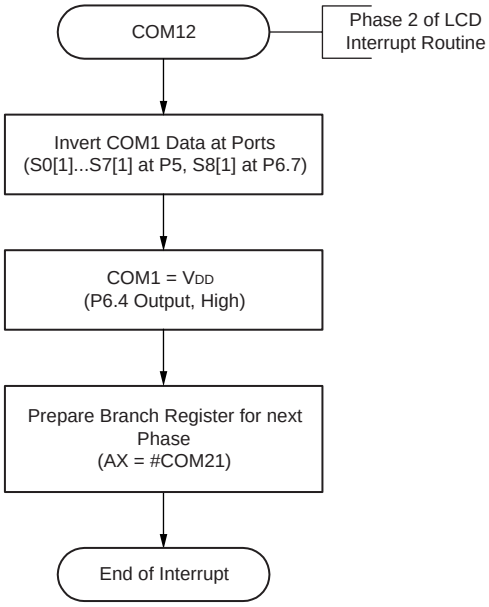
3.2.2 Phase 1 (COM11)

Figure 3-3: Phase 1 (COM11) Flow



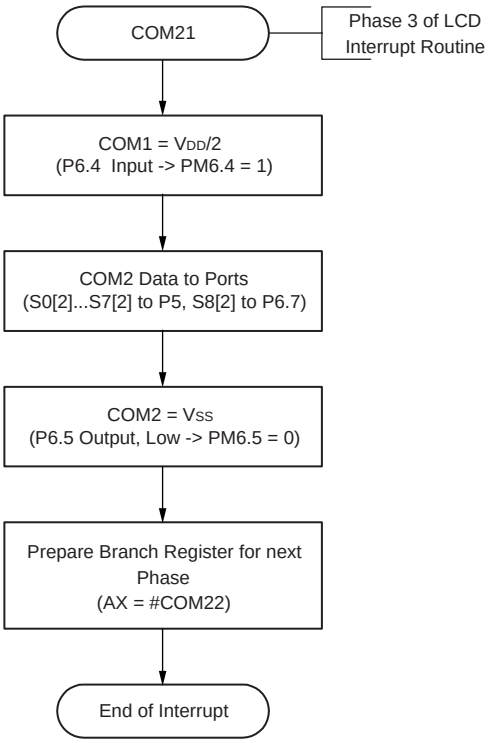
3.2.3 Phase 2 (COM12)

Figure 3-4: Phase 2 (COM12) Flow



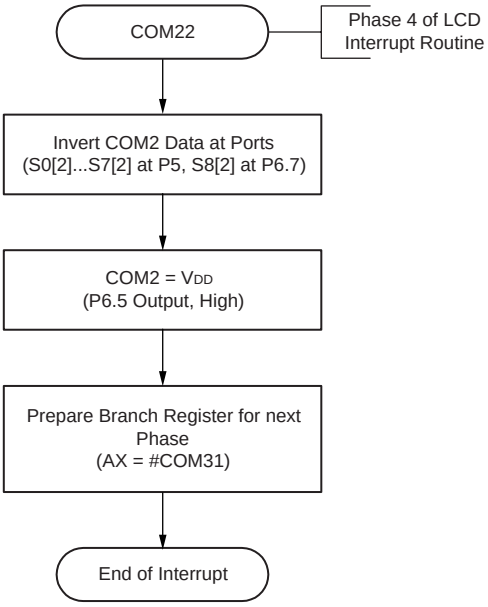
3.2.4 Phase 3 (COM21)

Figure 3-5: Phase 3 (COM21) Flow



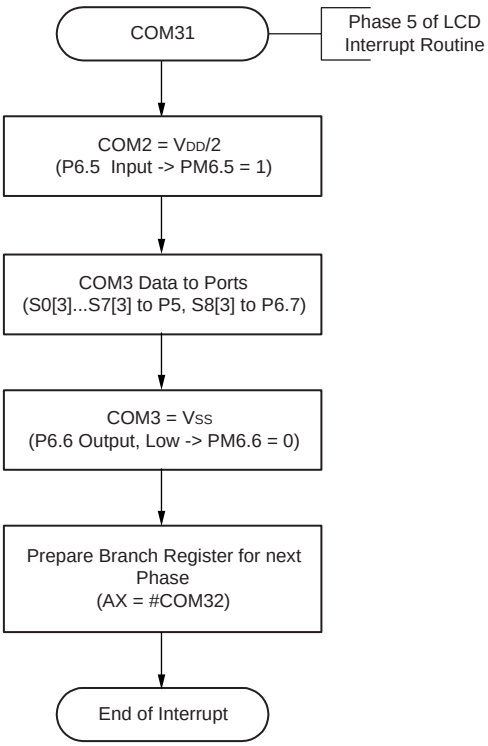
3.2.5 Phase 4 (COM22)

Figure 3-6: Phase 4 (COM22) Flow



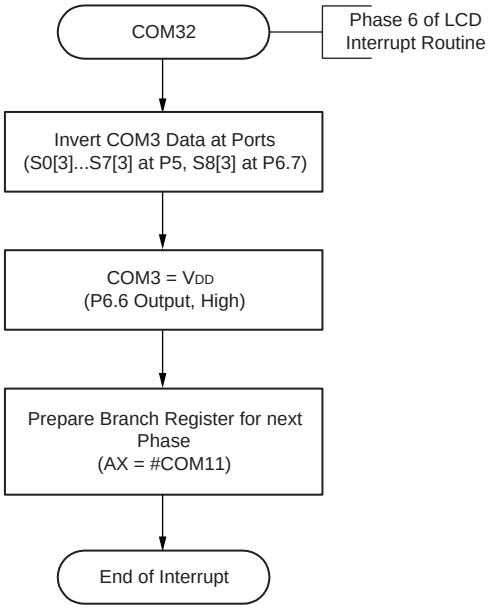
3.2.6 Phase 5 (COM31)

Figure 3-7: Phase 5 (COM31) Flow



3.2.7 Phase 6 (COM32)

Figure 3-8: Phase 6 (COM32) Flow



[MEMO]

Chapter 4 Example Program

4.1 Listing 1

```
    name    TriplexLCD;TRIPLLCD.ASM   L. Lenzen, December 1995.
               ;                L. Lenzen, January 1995.

;* Program to control the uPD78014 in a demo system which realizes an
;* triplex LCD driver/controller by standard tri-sate ports.
;* The timing of the LCD C/D service routine is critical.
;* The trigger signal is generated by TIMER3 every 15ms (@8.38MHz), which
;* is out experience of LCD C/D specialists the best compromise between CPU
;* load and LCD display contrast.
;*
;* N O T E:
;* all timings are based on a 8.38 MHz crystal (default type of IE-78000-R)
;* if a other oscillator frequency is used, the settings must be adopted.
;* As an example the alternative values for a 10 MHz oscillator frequency
;* are added as comment.
;*
;* To realize the three voltage levels, an external resistor circuitry is
;* connected to each COM line (value R depends on LCD glass current)
;*                     COMn
;*                      o
;*                      |
;*      VDD o---[R]---o---[R]---o VSS
;*                      |
;*                    to LCD
;*
;* The purpose of the program is to show that a triplex LCD glass can be
;* controlled by a standard general purpose CPU.
;* The realized LCD Controller/Driver is a so called Dot-Matrix Driver,
;* means each segment-common line combination (a dot) can be separately
;* controlled. It also means that a character generator must be realized by
;* the user software.
;*
;* In this program a 3x9 LCD glass is assumed (thus 3 * 9 = 27 dots).
;* The Common/Segment Lines are organized related to display memory as
;* follows:
;*
;*      |  SEG0 |  SEG1 |  SEG2 |  SEG3 |  SEG4 |  SEG5 |  SEG6 |  SEG7 |  SEG8 |
;*      |  P5.0 |  P5.1 |  P5.2 |  P5.3 |  P5.4 |  P5.5 |  P5.6 |  P5.7 |  P6.7 |
;* -----+-------+-------+-------+-------+-------+-------+-------+-------+-------+
;* COM1 |               FADA                            | FADB  |
;* P6.4 | Bit 0 | Bit 1 | Bit 2 | Bit 3 | Bit 4 | Bit 5 | Bit 6 | Bit 7 | Bit 0 |
;* -----+-------+-------+-------+-------+-------+-------+-------+-------+-------+
;* COM2 |               FADC                            | FADD  |
;* P6.5 | Bit 0 | Bit 1 | Bit 2 | Bit 3 | Bit 4 | Bit 5 | Bit 6 | Bit 7 | Bit 0 |
;* -----+-------+-------+-------+-------+-------+-------+-------+-------+-------+
;* COM3 |               FADE                            | FADF  |
;* P6.6 | Bit 0 | Bit 1 | Bit 2 | Bit 3 | Bit 4 | Bit 5 | Bit 6 | Bit 7 | Bit 0 |
;* -----+-------+-------+-------+-------+-------+-------+-------+-------+-------+
;*
;* The Interrupt Service Routine occupies register pair xa of Register Bank 3.
;* This register pair may not be used for other purposes than to control
;* the LCD routine.
```

Listing 1 (cont.)

```
    p78P014                 ;Processor type

    PUBLIC V_TABLE          ; absolute definition of vectors
    RSEG    INTVEC          ; Vector Area Start

V_TABLE:
    DW      start; at 0000h Reset vector
    DW  dummy
    DW  dummy
    DW  dummy
    DW  dummy
    DW  dummy
    DW  dummy
    DW  dummy
    DW  dummy
    DW  LCD_isr ; at 0012h INTTM3 vector (LCD Frame timing)

dummy:
    reti


Display EQU     0FADAh          ; memory buffer for LCD display data

    public start
    public init_LCD, LCD_clr

;-------------------------------------------------------------------------
;       Basic Initialization (must be done before program start)
;-------------------------------------------------------------------------
    rseg    RCODE
start:
    movw    sp,#0fee0h      ;set stack pointer
    sel     rb0             ;register bank 0 for main program
    mov     PCC,#00h
            ; -----0--      CPU clock at full speed

;-------------------------------------------------------------------------
;       Clear CPU RAM area (just an option, only for security)
;-------------------------------------------------------------------------
ram_clr:
    mov     a,#0            ;clear ram from FB00 to FEDF
    movw    hl,#0FE00h
    mov     b,#0DFh
clr1:
    mov     [hl+b],a
    dbnz    b,clr1
    mov     [hl+b],a
    mov     c,#3
clr2:
    dec     h
clr3:
    mov     [hl+b],a
    dbnz    b,clr3
    dbnz    c,clr2
```

Listing 1 (cont.)

```
;---------------------------------------------------------------------
;       Initialize System
;---------------------------------------------------------------------

    mov MM,#01h         ;Memory expansion mode for normal port
        ;--00----       ; no wait
        ;-----001       ; single chip mode
        ;00--0---       ; fixed to zero

    call    init_LCD    ;Initialize LCD C/D
;---------------------------------------------------------------------
;       start of MAIN Loop

    publicloop

loop:
                ;

;       end of MAIN Loop
;---------------------------------------------------------------------

;---------------------------------------------------------------------
;   Initialization of LCD Controller / Driver
; Based on Interval-Timer TM3 (so can operate with main or subsystem
; oscillator to enable also operation in standby modes)
;---------------------------------------------------------------------

init_LCD:
    ;-----------------------------------------------------------------
    ;       Clear the LCD Display Memory
    ;-----------------------------------------------------------------
    callLCD_clr ;clear display memory
                ;
    ;-----------------------------------------------------------------
    ;       Initialize the Timer TM3 for LCD Frame-Timing
    ;-----------------------------------------------------------------
    clr1    MK0L.7          ; enable interrupt
    clr1    PR0L.7          ; high priority
    clr1    IF0L.7          ; clear request bit
                ;
    ;setup timer mode register for ca. 15ms (< 20ms)
    ;for subsystem clock   32.768KHz -> TMC2 = 52h, TCL24 = 1 (15.6ms)
    ;for main system clock  8.38 MHz -> TMC2 = 52h, TCL24 = 0 (15.6ms)
    ;for main system clock 10.00 MHz -> TMC2 = 52h, TCL24 = 0 (13.1ms)
    ;for main system clock  4.19 MHz -> TMC2 = 42h, TCL24 = 0 (15.6ms)
    mov TMC2,#12h       ; Interval Timer
        ;-101.----       ; 512/fw (fw = 32.768KHz)
        ;----.-1--       ; start / enable
        ;0---.x-xx       ; don¦t care
        ;
```

Listing 1 (cont.)

```
    ;---------------------------------------------------------------
    ;       Initialize the Branch Vector Register (RB3.AX)
    ;---------------------------------------------------------------
    mov P5,#0   ; clear all segment drivers
    clr1P6.7    ;
                ;
    mov PM5,#0  ; all segment lines are output
    clr1PM6.7   ;
                ;
    set1PM6.4   ; all common lines to VDD/2
    set1PM6.5   ;
    set1PM6.6   ;
                ;
    clr1P6.4    ; prepare COM1 data
                ;
    sel RB3     ; prepare AX(3) for first LCD service process
    movwax,#COM11;
    sel RB0     ;
                ;
    ;---------------------------------------------------------------
    ;       Enable Interrupts
    ;---------------------------------------------------------------
    ei          ; now we can enable interrupts
    ret         ; exit
                ;
;-------------------------------------------------------------------------
;
;       Clear the LCD C/D Display memory (<=> LCD off)
;
;-------------------------------------------------------------------------
LCD_clr:
    mov     a,#0            ;clear LCD RAM from FADA to FADF
    movw    hl,#Display     ;base address
    mov     c,#05h          ;number of bytes + 1
lcd_clr1:
    mov     [hl+c],a;
    dbnz    c,lcd_clr1;
    mov     [hl+c],a;
    ret     ; exit
            ;


;-------------------------------------------------------------------------
;
;       Frame-Interrupt Service (called every 15ms)
;
;-------------------------------------------------------------------------

    publicLCD_isr, COM11, COM12, COM21, COM22, COM31, COM32

LCD_isr:
    sel RB3     ;select LCD Register Bank
    EI                      ;all interrupts except ADC interrupt
    br  ax      ; jump to actual process
                ;
```

Listing 1 (cont.)

```
    ;---------------------------------------------------------------
    ;   LCD Service Process for 1. frame
    ;---------------------------------------------------------------
COM11:
    set1PM6.6  ;COM3 to VDD/2
    mov a,0FADAh;S0(0) - S7(0) to P5
    mov P5,a   ;
    mov a,0FADBh;S8(0) to P6.7
    rorca,1    ;
    mov1P6.7,cy;
    clr1P6.4   ;prepare COM1 for VSS
    clr1PM6.4  ;COM1 to VSS
        ;---------------------------------------------
        ; prepare LCD Service Process for 2. frame
        ;---------------------------------------------
    movwax,#COM12;
    reti       ;
    ;---------------------------------------------------------------
    ;   LCD Service Process for 2. frame
    ;---------------------------------------------------------------
COM12:
    mov a,P5   ;invert S0(0) - S7(0)
    xor a,#0FFh;
    mov P5,a   ;
    mov1cy,P6.7;invert S8(0)
    not1cy     ;
    mov1P6.7,cy;
    set1P6.4   ;COM1 to VDD
        ;---------------------------------------------
        ; prepare LCD Service Process for 3. frame
        ;---------------------------------------------
    movwax,#COM21;
    reti       ;
    ;---------------------------------------------------------------
    ;   LCD Service Process for 3. frame
    ;---------------------------------------------------------------
COM21:
    set1PM6.4  ;COM1 to VDD/2
    mov a,0FADCh;S0(1) - S7(1) to P5
    mov P5,a   ;
    mov a,0FADDh;S8(1) to P6.7
    rorca,1    ;
    mov1P6.7,cy;
    clr1P6.5   ;prepare COM2 for VSS
    clr1PM6.5  ;COM2 to VSS
        ;---------------------------------------------
        ; prepare LCD Service Process for 4. frame
        ;---------------------------------------------
    movwax,#COM22;
    reti       ;
```

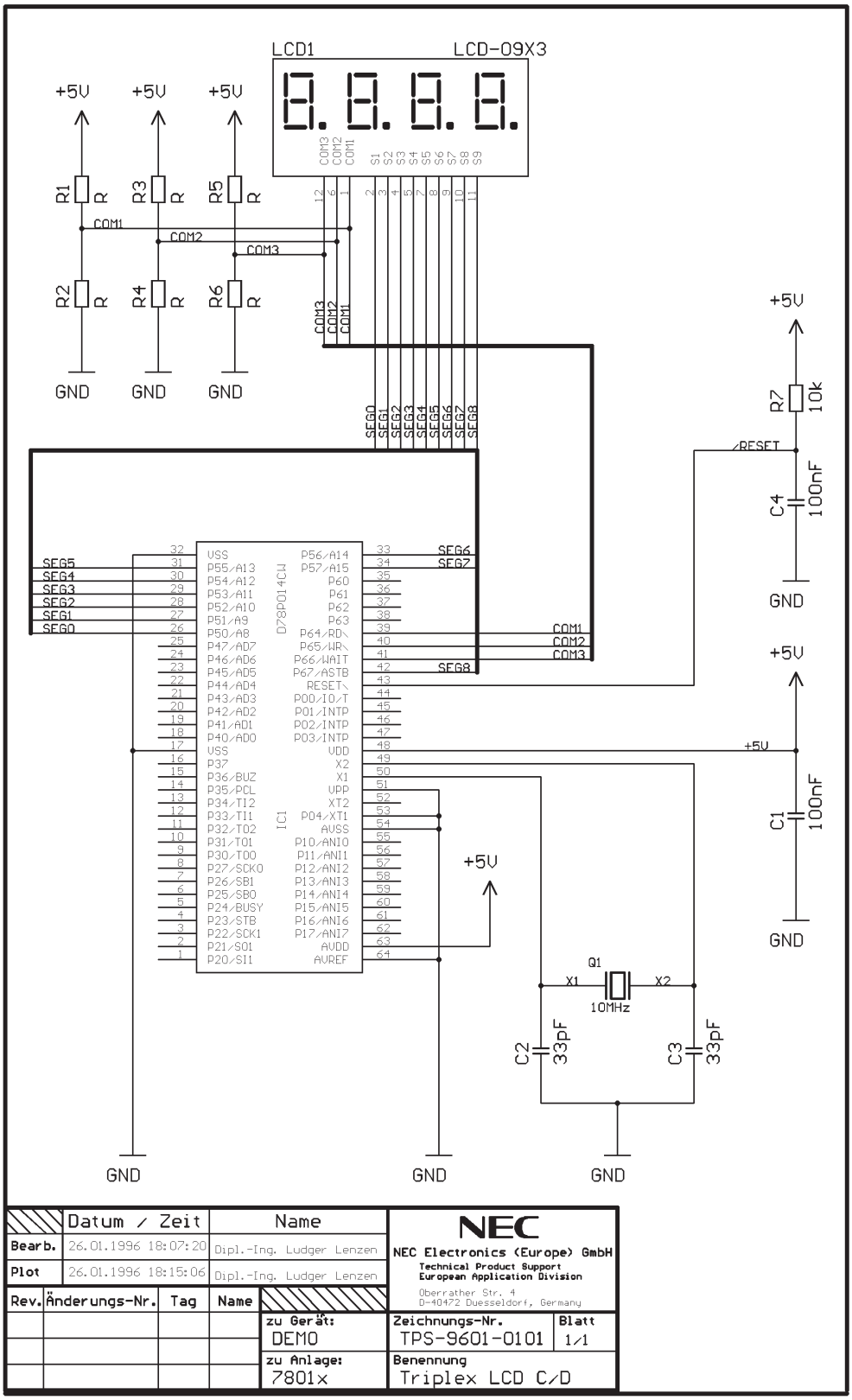
Listing 1 (cont.)

```
    ;---------------------------------------------------------------
    ;   LCD Service Process for 4. frame
    ;---------------------------------------------------------------
COM22:
    mov a,P5    ;invert S0(1) - S7(1)
    xor a,#0FFh ;
    mov P5,a    ;
    mov1cy,P6.7 ;invert S8(1)
    not1cy      ;
    mov1P6.7,cy ;
    set1P6.5    ;COM2 to VDD
        ;-----------------------------------------------
        ; prepare LCD Service Process for 5. frame
        ;-----------------------------------------------
    movwax,#COM31;
    reti        ;
    ;---------------------------------------------------------------
    ;   LCD Service Process for 5. frame
    ;---------------------------------------------------------------
COM31:
    set1PM6.5       ;COM2 to VDD/2
    mov a,0FADEh    ;S0(2) - S7(2) to P5
    mov P5,a        ;
    mov a,0FADFh    ;S8(2) to P6.7
    rorca,1         ;
    mov1P6.7,cy     ;
    clr1P6.6        ;prepare COM3 for VSS
    clr1PM6.6       ;COM3 to VSS
        ;-----------------------------------------------
        ; prepare LCD Service Process for 6. frame
        ;-----------------------------------------------
    movwax,#COM32;
    reti        ;
    ;---------------------------------------------------------------
    ;   LCD Service Process for 6. frame
    ;---------------------------------------------------------------
COM32:
    mov a,P5    ;invert S0(2) - S7(2)
    xor a,#0FFh ;
    mov P5,a    ;
    mov1cy,P6.7 ;invert S8(2)
    not1cy      ;
    mov1P6.7,cy ;
    set1P6.6    ;COM3 to VDD
        ;-----------------------------------------------
        ; prepare LCD Service Process for 1. frame
        ;-----------------------------------------------
    movwax,#COM11;
    reti        ;

    end
```

4.2 Circuit Diagram for the Example Program

Figure 4-1: Circuit Diagram



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