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April 1st, 2010
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Application Note

µPD780988 Subseries

8-bit Single-Chip Microcontrollers

10-Bit Inverter Timer (TM7) Fundamentals

µPD780982

µPD780983

µPD780984

µPD780986

µPD780988

µPD78F0988A

Document No. U16518EE1V0AN00 (1st edition)
Date Published December 2002

[MEMO]

NOTES FOR CMOS DEVICES

1. PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

2. HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

3. STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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Contents

(A) Features of the Timer7

The µPD78098x subseries incorporates a 10-bit inverter control timer 7 (TM7). This timer can control the output of three complementary phase pairs, [(U+,U-), (V+,V-), (W+,W-)], and consists of the following:

10-bit inverter control TM7

- up/down counter which generates interrupt INTTM7 on underflow

Compare Registers

- CM3, compare register 3, to set period (frequency) of waveforms (U, V, W)
- CM2, compare register 2, to set W+ active pulse width
- CM1, compare register 1, to set V+ active pulse width
- CM0, compare register 0, to set U+ active pulse width

Buffer registers

- BFCM3, buffer register 3, transfers to CM3 on TM7 interrupt, INTTM7
- BFCM2, buffer register 2, transfers to CM2 on TM7 interrupt, INTTM7
- BFCM1, buffer register 1, transfers to CM1 on TM7 interrupt, INTTM7
- BFCM0, buffer register 0, transfers to CM0 on TM7 interrupt, INTTM7

Buffer Transfer Control Timer RTM0

- 3-bit down counter which divides occurrence of interrupt INTTM7

Dead time down counters

- DTM2, 8-bit down counter for dead time between active levels of W+and W-
- DTM1, 8-bit down counter for dead time between active levels of V+ and V-
- DTM0, 8-bit down counter for dead time between active levels of U+ and U-

Dead time reload register

- DTIME, 8-bit reload register, transfers to DTM2, DTM1, DTM0 on TM7 match with CM2, CM1, CM0 respectively.

Outputs

- TO74 for W+ TO75 for W-
- TO72 for V+ TO73 for V-
- TO70 for U+ TO71 for U-

Output Stop Control Options

- none
- interrupt from watchdog timer
- rising/falling edge on Port 0.0 / TOFF7

(B) Program Description

This program demonstrates inverter operation by setting an output period of 200us and simultaneously outputting active high pulse widths of 50us on U+, 100us on V+ and 150us on W+. Outputs U-, V- and W- are simply the inverse waveforms of U+, V+ and W+. The program also sets a dead time of 10us – note that the effect of this is to shorten the active high pulse width on the positive phase, and to lengthen its inverse on the negative phase.

Timer 7 (TM7)is first stopped and cleared. An 8.38MHz count clock is selected by writing to Timer Control register 7, TMC7. The least significant 3-bits (IDEV2, IDEV1, IDEV0) of TMC7 make up the Buffer Transfer Control Timer, RTM0. By setting RTM0 to zero, INTTM7 is selected to occur once on every TM7 underflow. An active high level and no output stop control are selected by writing to Inverter Time Mode register 7, TMM7.

Compare register 3, CM3, is set to 838 which gives a count up interval of 100us (838/8.38MHz). When TM7 counts up to this value, it reverses and starts counting down until in generates interrupt INTTM7 on underflow. This gives a period of 200us (2 x 100us) for the U, V, W waveforms.

- Compare register 2 is set to 629 to set the W+ pulse width to 50us.
- Compare register 1 is set to 419 to set the V+ pulse width to 100us.
- Compare register 0 is set to 210 to set the V+ pulse width to 150us.

Note that a smaller value in CM2-CM0 gives a longer pulse width. This is because TM7 switches the positive phase waveform to its active level when it matches the compare register during its up count. It does not reset it to its inactive level until it again matches the compare register during its down count.

The program also writes values to the buffer registers BFCM3-BFCM0, as these will be transferred to compare registers CM3-CM0 on the first TM7 interrupt. The program writes a value of 84 to the dead time reload register, DTIME, to set a dead time value of 10us (84/8.38MHz). This is to ensure that the active levels of the positive and negative phases do not overlap due to the finite switching times of real world components. The value set here in DTIME will be transferred to dead time down counters DTM2-DTM0 when there is a respective match between TM7 and compare registers CM2-CM0.

Timer 7 is then started and interrupts are enabled. The TM7 interrupt routine is used to update the buffer registers, BFCM3-BFCM0, ready for transfer on the next TM7 interrupt, INTTM7. The dead time reload register, DTIME, is also updated, ready for transfer to the respective dead time down counter DTM2-DTM0 on the next TM7 match with CM2-CM0.

(C) Program Specifications

- Inverter timer, TM7, count clock: 8.38Mhz

- Compare register 3, CM3, and its buffer register BFCM3:
  838 (200us period)

- Compare register 2, CM2, and its buffer register BFCM2:
  210 (150us W+)

- Compare register 1, CM1, and its buffer register BFCM1:
  419 (100us V+)

- Compare register 0, CM0, and its buffer register BFCM0:
  629 (50us U+)

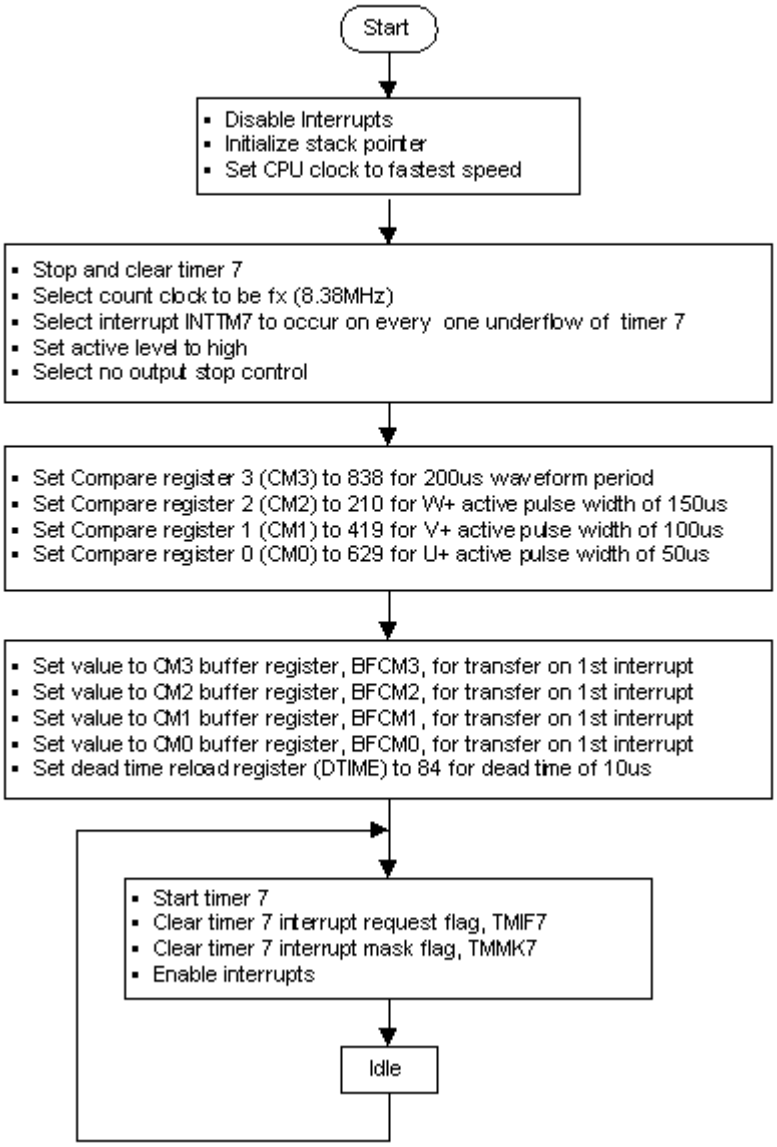
- Dead time reload register, DTIME: 84 (10us dead time)

- Pins used in program

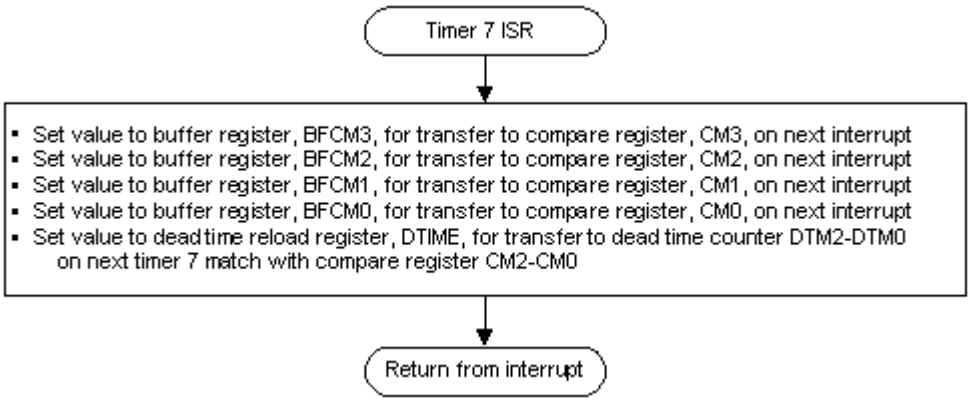
TO74 for W+	TO75 for W-
TO72 for V+	TO73 for V-
TO70 for U+	TO71 for U-

(D) Software Flow Chart

Flowchart - Main Program



Flowchart - Interrupt Service Routine



(E) Software Listing

```
/*********************************************************************
; Date:             15.07.02
;
; Parameters:   - fastest CPU clock (fx=8.3800MHz)
;                   - up/down counter TM7 count clock: fx (8.38MHz)
;                   - compare register CM3/BFCM3: 838 (200us period)
;                   - compare register CM2/BFCM2: 210 (150us W+)
;                   - compare register CM1/BFCM1: 419 (100us V+)
;                   - compare register CM0/BFCM0: 629 ( 50us U+)
;                   - dead time register DTIME:    84 (10us dead time)
;
;*********************************************************************/


/*=====================================
; Include Files
;=====================================*/
#include <in78000.h>
#include "DF0988.h"


/*=====================================
; Constants/Variables
;=====================================*/

#define TRUE  1
#define FALSE 0


/*=====================================
; Main Program
;=====================================*/

void main(void)
{
_DI();                                  /* Disable interrupts */
/* Stack pointer set by compiler */
PCC     = 0x00                          /* Set CPU clock to fastest speed */

CE7     = 0;                            /* Clear and stop timer 7 */
TMC7    = 0x00;                         /* Select 8.38MHz clock to TM7 */
/* with interrupt on every 1 underflows */
TMM7    = 0x08;                         /* Set active level high */
/* with no output stop control */

CM3     = 838;                          /* Set CM3 to 838 (100us x 2 interval) */
CM2     = 210;                          /* Set CM2 for W+ active width of 150us */
CM1     = 419;                          /* Set CM1 for V+ active width of 100us */
CM0     = 629;                          /* Set CM0 for U+ active width of 50us */

BFCM3 = 838;                            /* Set buffer 3 for 1st interrupt */
BFCM2 = 210;                            /* Set buffer 2 for 1st interrupt */
BFCM1 = 419;                            /* Set buffer 1 for 1st interrupt */
BFCM0 = 629;                            /* Set buffer 0 for 1st interrupt */
DTIME  = 84;                            /* Set dead time reload of 10us */
```

```
CE7     = 1;                            /* Start timer */
TMIF7   = 0;                            /* Clear timer interrupt request flag */
TMMK7= 0;                               /* Clear timer interrupt mask flag */
_EI();                                  /* Enable interrupts */


while(TRUE)                             /* Loop here */
{
_NOP();
}

}                                       /* End of function main */


/*=====================================
;          Timer 7 ISR
;=====================================*/


interrupt[INTTM7_vect] void TM7_ISR(void)
{

BFCM3 = 838;                            /* Set buffer 3 for next interrupt */
BFCM2 = 210;                            /* Set buffer 2 for next interrupt */
BFCM1 = 419;                            /* Set buffer 1 for next interrupt */
BFCM0 = 629;                            /* Set buffer 0 for next interrupt */
DTIME  = 84;                            /* Set dead time reload for next */
/* TM7 match with CM2-CM0 */

/* Return from interrupt */
}
/*********************************************************************/
```

[MEMO]

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