To our customers,

---

Old Company Name in Catalogs and Other Documents

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April 1\textsuperscript{st}, 2010
Renesas Electronics Corporation

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Application Note

78K0R/Kx3-L, 78K0R/Ix3, 78K0R/Kx3-C

16-bit Single-Chip Microcontrollers

Flash Memory Programming (Programmer)

78K0R/KC3-L: μPD78F1000, 78F1001, 78F1002, 78F1003
78K0R/KD3-L: μPD78F1004, 78F1005, 78F1006
78K0R/KE3-L: μPD78F1007, 78F1008, 78F1009
78K0R/KF3-L: μPD78F1010, 78F1011, 78F1012
78K0R/KG3-L: μPD78F1013, 78F1014
78K0R/IB3: μPD78F1201, 78F1203
78K0R/IC3: μPD78F1211, 78F1213, 78F1214, 78F1215
78K0R/ID3: μPD78F1223, 78F1224, 78F1225
78K0R/IE3: μPD78F1233, 78F1234, 78F1235
78K0R/KF3-C: μPD78F1846, 78F1847
78K0R/KG3-C: μPD78F1848, 78F1849
[MEMO]
1 VOLTAGE APPLICATION WAVEFORM AT INPUT PIN
Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between $V_{IL}$ (MAX) and $V_{IH}$ (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between $V_{IL}$ (MAX) and $V_{IH}$ (MIN).

2 HANDLING OF UNUSED INPUT PINS
Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to $V_{DD}$ or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

3 PRECAUTION AGAINST ESD
A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

4 STATUS BEFORE INITIALIZATION
Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

5 POWER ON/OFF SEQUENCE
In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current. The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

6 INPUT OF SIGNAL DURING POWER OFF STATE
Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.
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INTRODUCTION

Caution
Explanations in this application note assume use of the 78K0R/Kx3-L as the representative microcontroller. Users of a product other than the 78K0R/Kx3-L should read 78K0R/Kx3-L as referring to that product.

Target Readers
This application note is intended for users who understand the functions of the 78K0R/Kx3-L, 78K0R/Ix3, and 78K0R/Kx3-C and who will use these products to design application systems.

Purpose
The purpose of this application note is to help users understand how to develop dedicated flash memory programmers for rewriting the internal flash memory of the 78K0R/Kx3-L, 78K0R/Ix3, and 78K0R/Kx3-C.
The sample programs and circuit diagrams shown in this document are for reference only and are not intended for use in actual design-ins. Therefore, these sample programs must be used at the user’s own risk. Correct operation is not guaranteed if these sample programs are used.

Organization
This manual consists of the following main sections.
• Flash memory programming
• Command/data frame format
• Description of command processing
• UART communication mode
• Flash memory programming parameter characteristics

How to Read This Manual
It is assumed that the reader of this manual has general knowledge in the fields of electrical engineering, logic circuits, and microcontrollers.
• To gain a general understanding of functions:
  → Read this manual in the order of the CONTENTS.
• To learn more about hardware functions of the 78K0R/Kx3-L, 78K0R/Ix3, and 78K0R/Kx3-C:
  → See the user’s manual of the 78K0R/Kx3-L, 78K0R/Ix3, or 78K0R/Kx3-C.

Conventions
Data significance: Higher digits on the left and lower digits on the right
Active low representation: XXX (overscore over pin or signal name)
Note: Footnote for item marked with Note in the text
Caution: Information requiring particular attention
Remark: Supplementary information
Numerical representation:
  • Binary.................xxxx or xxxxB
  • Decimal...............xxxx
  • Hexadecimal .........xxxxH
Related Documents

The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

Documents related to the 78K0R/Kx3-L, 78K0R/Ix3, and 78K0R/Kx3-C

<table>
<thead>
<tr>
<th>Document Name</th>
<th>Document No.</th>
</tr>
</thead>
<tbody>
<tr>
<td>78K0R/Kx3-L User’s Manual</td>
<td>U19291E</td>
</tr>
<tr>
<td>78K0R/IB3 User’s Manual</td>
<td>U19018E</td>
</tr>
<tr>
<td>78K0R/IC3 User’s Manual</td>
<td>U19120E</td>
</tr>
<tr>
<td>78K0R/ID3 User’s Manual</td>
<td>U19185E</td>
</tr>
<tr>
<td>78K0R/IE3 User’s Manual</td>
<td>U19163E</td>
</tr>
<tr>
<td>78K0R/KG3-C User’s Manual</td>
<td>U19274E</td>
</tr>
<tr>
<td>78K0R Microcontrollers Instructions User’s Manual</td>
<td>U17792E</td>
</tr>
</tbody>
</table>

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CHAPTER 1 FLASH MEMORY PROGRAMMING

To rewrite the contents of the internal flash memory of the 78K0R/Kx3-L, a dedicated flash memory programmer (hereafter referred to as the “programmer”) is usually used. This Application Note explains how to develop a dedicated programmer.

1.1 Overview

The 78K0R/Kx3-L incorporates firmware that controls flash memory programming. The programming to the internal flash memory is performed by transmitting/receiving commands between the programmer and the 78K0R/Kx3-L via serial communication.

Figure 1-1. System Outline of Flash Memory Programming in 78K0R/Kx3-L
1.2 System Configuration

Examples of the system configuration for programming the flash memory are illustrated in Figure 1-2. These figures illustrate how to program the flash memory with the programmer, under control of a host machine. Depending on how the programmer is connected, the programmer can be used in a standalone mode without using the host machine, if a user program has been downloaded to the programmer in advance.

For example, NEC Electronics’ flash memory programmer PG-FP5 can execute programming either by using the GUI software with a host machine connected or by itself (standalone).

Figure 1-2. System Configuration Example

Single-wire UART communication mode (LSB-first transfer)

Remarks 1. The 78K0R/Kx3-L can only communicate via the single-wire UART communication mode.
2. For the pins used by flash memory programming and the recommended connections of unused pins, see the user's manual of each product.
1.3 Flash Memory Configuration

The 78K0R/Kx3-L must manage product-specific information (such as device name and memory information) via the programmer.

Table 1-1 shows the flash memory size of the 78K0R/Kx3-L and Figure 1-3 shows the configuration of the flash memory.

Table 1-1. Size of Flash Memory for Each Product

(a) Size of Flash Memory for 78K0R/Kx3-L

<table>
<thead>
<tr>
<th>Device Name</th>
<th>Flash Memory Size</th>
</tr>
</thead>
<tbody>
<tr>
<td>μPD78F1000</td>
<td>16 KB</td>
</tr>
<tr>
<td>μPD78F1001, 78F1004, 78F1007</td>
<td>32 KB</td>
</tr>
<tr>
<td>μPD78F1002, 78F1005, 78F1008</td>
<td>48 KB</td>
</tr>
<tr>
<td>μPD78F1003, 78F1006, 78F1009, 78F1010</td>
<td>64 KB</td>
</tr>
<tr>
<td>μPD78F1011, 78F1013</td>
<td>96 KB</td>
</tr>
<tr>
<td>μPD78F1012, 78F1014</td>
<td>128 KB</td>
</tr>
</tbody>
</table>

(b) Size of Flash Memory for 78K0R/Ix3

<table>
<thead>
<tr>
<th>Device Name</th>
<th>Flash Memory Size</th>
</tr>
</thead>
<tbody>
<tr>
<td>μPD78F1211</td>
<td>16 KB</td>
</tr>
<tr>
<td>μPD78F1213, 78F1223, 78F1233</td>
<td>32 KB</td>
</tr>
<tr>
<td>μPD78F1214, 78F1224, 78F1234</td>
<td>48 KB</td>
</tr>
<tr>
<td>μPD78F1215, 78F1225, 78F1235</td>
<td>64 KB</td>
</tr>
</tbody>
</table>

(c) Size of Flash Memory for 78K0R/Kx3-C

<table>
<thead>
<tr>
<th>Device Name</th>
<th>Flash Memory Size</th>
</tr>
</thead>
<tbody>
<tr>
<td>μPD78F1846, 78F1848</td>
<td>96 KB</td>
</tr>
<tr>
<td>μPD78F1847, 78F1849</td>
<td>128 KB</td>
</tr>
</tbody>
</table>

Remark Products under development are included in the above tables.
Figure 1-3. Flash Memory Configuration

Remark: Each block consists of 1 KB (this figure only illustrates some blocks in the flash memory).
1.4 Command List and Status List

The flash memory incorporated in the 78K0R/Kx3-L can be rewritten by using the commands listed in Table 1-2. The programmer transmits commands to control these functions to the 78K0R/Kx3-L, and checks the response status sent from the 78K0R/Kx3-L, to manipulate the flash memory.

1.4.1 Command list

The commands used by the programmer and their functions are listed below.

<table>
<thead>
<tr>
<th>Command Number</th>
<th>Command Name</th>
<th>Function Name</th>
<th>Function Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>20H</td>
<td>Chip Erase</td>
<td>Erase</td>
<td>Erases the entire flash memory area.</td>
</tr>
<tr>
<td>22H</td>
<td>Block Erase</td>
<td>Erase</td>
<td>Erases a specified area in the flash memory.</td>
</tr>
<tr>
<td>40H</td>
<td>Programming</td>
<td>Write</td>
<td>Writes data to a specified area in the flash memory.</td>
</tr>
<tr>
<td>13H</td>
<td>Verify</td>
<td>Verify</td>
<td>Compares the contents in a specified area in the flash memory with the data transmitted from the programmer.</td>
</tr>
<tr>
<td>32H</td>
<td>Block Blank Check</td>
<td>Blank check</td>
<td>Checks the erase status of a specified block in the flash memory.</td>
</tr>
<tr>
<td>C0H</td>
<td>Silicon Signature</td>
<td>Information acquisition</td>
<td>Acquires 78K0R/Kx3-L information (product name, flash memory configuration, etc.).</td>
</tr>
<tr>
<td>C5H</td>
<td>Version Get</td>
<td></td>
<td>Acquires version of the 78K0R/Kx3-L and firmware.</td>
</tr>
<tr>
<td>B0H</td>
<td>Checksum</td>
<td></td>
<td>Acquires checksum data of a specified area.</td>
</tr>
<tr>
<td>A0H</td>
<td>Security Set</td>
<td>Security</td>
<td>Sets security information.</td>
</tr>
<tr>
<td>00H</td>
<td>Reset</td>
<td>Others</td>
<td>Detects synchronization in communication.</td>
</tr>
<tr>
<td>9AH</td>
<td>Baud Rate Set</td>
<td></td>
<td>Sets the baud rate when UART communication mode is selected.</td>
</tr>
</tbody>
</table>
1.4.2 Status list

The following table lists the status codes the programmer receives from the 78K0R/Kx3-L.

<table>
<thead>
<tr>
<th>Status Code</th>
<th>Status</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>04H</td>
<td>Command number error</td>
<td>Error returned if a command not supported is received</td>
</tr>
<tr>
<td>05H</td>
<td>Parameter error</td>
<td>Error returned if command information (parameter) is invalid</td>
</tr>
<tr>
<td>06H</td>
<td>Normal acknowledgment (ACK)</td>
<td>Normal acknowledgment</td>
</tr>
<tr>
<td>07H</td>
<td>Checksum error</td>
<td>Error returned if data in a frame transmitted from the programmer is abnormal</td>
</tr>
<tr>
<td>0FH</td>
<td>Verify error</td>
<td>Error returned if a verify error has occurred upon verifying data transmitted from the programmer</td>
</tr>
<tr>
<td>10H</td>
<td>Protect error</td>
<td>Error returned if an attempt is made to execute processing that is prohibited by the Security Set command</td>
</tr>
<tr>
<td>15H</td>
<td>Negative acknowledgment (NACK)</td>
<td>Negative acknowledgment</td>
</tr>
<tr>
<td>1AH</td>
<td>MRG10 error</td>
<td>Erase verify error</td>
</tr>
<tr>
<td>1BH</td>
<td>MRG11 error</td>
<td>Internal verify error or blank check error during data write</td>
</tr>
<tr>
<td>1CH</td>
<td>Write error</td>
<td>Write error</td>
</tr>
</tbody>
</table>

Reception of a checksum error or NACK is treated as an immediate abnormal end in this manual. When a dedicated programmer is developed, however, the processing may be retried without problem from the wait immediately before transmission of the command that results a checksum error or NACK. In this event, limiting the retry count is recommended for preventing infinite repetition of the retry operation.

Although not listed in the above table, if a time-out error (BUSY time-out or time-out in data frame reception during UART communication) occurs, it is recommended to shutdown the power supply to the 78K0R/Kx3-L (refer to 1.6 Shutting Down Target Power Supply) and then connect the power supply again.
1.5 Power Application and Setting Flash Memory Programming Mode

To rewrite the contents of the flash memory with the programmer, the 78K0R/Kx3-L must first be set to the flash memory programming mode by supplying a specific voltage to the flash memory programming mode setting pin (FLMD0) in the 78K0R/Kx3-L, then releasing a reset.

To select a communication mode for flash memory rewriting, input pulses to the FLMD0 pin in the flash memory programming mode.

The following figure illustrates a timing chart for setting the flash memory programming mode and selecting the communication mode.

![Figure 1-4. Setting Flash Memory Programming Mode and Selecting Communication Mode](image)

The relationship between the setting of the FLMD0 pin after reset release and the operating mode is shown below.

**Table 1-4. Relationship Between FLMD0 Pin Setting After Reset Release and Operating Mode**

<table>
<thead>
<tr>
<th>FLMD0</th>
<th>Operating Mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>Low (GND)</td>
<td>Normal operating mode</td>
</tr>
<tr>
<td>High (VDD)</td>
<td>Flash memory programming mode</td>
</tr>
</tbody>
</table>

The following table shows the communication mode that can be selected with the 78K0R/Kx3-L, the number of pulses input to FLMD0 (pulse count), and the port to be used.

**Table 1-5. Relationship Between FLMD0 Pulse Count in 78K0R/Kx3-L and Communication Mode**

<table>
<thead>
<tr>
<th>Communication Mode</th>
<th>FLMD0 Pulse Count</th>
<th>Port Used for Communication</th>
</tr>
</thead>
<tbody>
<tr>
<td>Single-wire UART</td>
<td>0</td>
<td>TOOL0 (P40)</td>
</tr>
</tbody>
</table>
1.5.1 UART communication mode

The TOOL0 pin is used for UART communication. The communication conditions are as shown below.

<table>
<thead>
<tr>
<th>Item</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Baud rate</td>
<td>Communication is performed at 9,600 bps until the Baud Rate Set command for baud rate setting command processing is transmitted. The transmission rate is changed to the baud rate set by the Baud Rate Set command from the transmission of the Reset command for baud rate command processing. For details of the settable baud rate, refer to 3.2 Baud Rate Set Command.</td>
</tr>
<tr>
<td>Parity bit</td>
<td>None</td>
</tr>
<tr>
<td>Data length</td>
<td>8 bits (LSB first)</td>
</tr>
<tr>
<td>Stop bit</td>
<td>2 bits (programmer → 78K0R/Kx3-L)/1 bit (78K0R/Kx3-L → programmer)</td>
</tr>
</tbody>
</table>

The role of the master and slave is occasionally exchanged during UART communication, so communication at the optimum timing is possible.

**Caution** Set the same baud rate to the master and slave devices when performing UART communication.
1.5.2 Mode setting flowchart

Transition processing to programming mode

- RESET pin low output
- FLMD0 pin low output
- VDD pin high output (Target power supply on)

Wait for tDP

- FLMD0 pin high output

Wait for tPR

- RESET pin high output

Ready pulse check

OK
- Start of time measurement until start of reset command processing
- Initialization of UART hardware

Has specified time elapsed until start of reset command processing?

No
- Abnormal termination

Yes
- Normal termination
1.5.3 Sample program

The following shows a sample program for mode setting processing.

```c
/***************** connect to Flash device *****************/
/* */ /* connect to Flash device */ /* */ /* */
/***************** connect to Flash device *****************/

u16 fl_con_dev(void)
{
    extern void init_fl_uart(void);
    extern void init_fl_csi(void);
    extern void stop_UART0(void);

    u16 rc = NO_ERROR;

    SRMK0 = true;   // disable UART Rx INT.
    UART0 = false;  // disable UART H.W.
    stop_UART0();   // TxD/RxD = Hi-Z

    pFL_RBS = low;  // RESET = low
    pmFL_FLMD0 = PM_OUT; // FLMD0 = Low output
    pFL_FLMD0 = low;
    FL_VDD_HI();   // VDD = high

    fl_wait(tDP);   // wait

    pFL_FLMD0 = hi;  // FLMD0 = high
    fl_wait(tPR);   // wait

    pFL_RBS = hi;   // RESET = high

    rc = check_ready_pulse(); // check "READY PULSE" from target device
    if (rc){
        return rc;    // pulse width/timing error
    }

    start_flto(t01); // start "t01" wait timer

    init_fl_uart(); // Initialize UART h.w.(for Flash device control)
    UART0 = true;   // enable UART h.w.
    SRIF0 = false;  // clear UART Rx IRQ flag
    SRMK0 = false;  // enable UART Rx INT.

    while(!check_flto()) // timeout "t01" ?
    {
        ;    // no
    }

    return rc;
    // start RESET command proc.
}
```
1.6 Shutting Down Target Power Supply

After each command execution is completed, shut down the power supply to the target after setting the \texttt{RESET} pin to low level, as shown below.
Set other pins to Hi-Z when shutting down the power supply to the target.

\textbf{Caution} Shutting down the power supply and inputting a reset during command processing are prohibited.

\textbf{Figure 1-5. Timing for Terminating Flash Memory Programming Mode}

1.7 Command Execution Flow at Flash Memory Rewriting

Figure 1-6 illustrates the basic flowchart when flash memory rewriting is performed with the programmer.
Other than commands shown in Figure 1-6, the Verify command and Checksum command are also supported.
Figure 1-6. Basic Flowchart for Flash Memory Rewrite Processing

Remark The example of each command execution is shown in Figure 1-7.
Figure 1-7. General Command Execution Flow at Flash Memory Rewriting

- General command flow
- Block Blank Check command (See 3.7)
  - Yes
  - No
  - Block Erase command execution (See 3.4)
    - Programming command execution (See 3.5)
      - Verify command execution (See 3.6)
        - Security Set command execution (See 3.11)
          - End

This command is used to check whether data communication between programmer and target device was normally completed.
CHAPTER 2 COMMAND/DATA FRAME FORMAT

The programmer uses the command frame to transmit commands to the 78K0R/Kx3-L. The 78K0R/Kx3-L uses the data frame to transmit write data or verify data to the programmer. A header, footer, data length information, and checksum are appended to each frame to enhance the reliability of the transferred data.

The following shows the format of a command frame and data frame.

**Figure 2-1. Command Frame Format**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>SOH</td>
<td>01H</td>
<td>Command frame header</td>
</tr>
<tr>
<td>LEN</td>
<td>(1 byte)</td>
<td>Data length information (00H indicates 256).</td>
</tr>
<tr>
<td>COM</td>
<td>(1 byte)</td>
<td>Command number</td>
</tr>
<tr>
<td>SUM</td>
<td>(1 byte)</td>
<td>Checksum data for a frame</td>
</tr>
<tr>
<td>ETX</td>
<td>(1 byte)</td>
<td>Footer of command frame</td>
</tr>
</tbody>
</table>

**Figure 2-2. Data Frame Format**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>STX</td>
<td>02H</td>
<td>Data frame header</td>
</tr>
<tr>
<td>LEN</td>
<td>(1 byte)</td>
<td>Data length information (00H indicates 256).</td>
</tr>
<tr>
<td>COM</td>
<td>(1 byte)</td>
<td>Command number</td>
</tr>
<tr>
<td>SUM</td>
<td>(1 byte)</td>
<td>Checksum data for a frame</td>
</tr>
<tr>
<td>ETX</td>
<td>(1 byte)</td>
<td>Footer of data frame</td>
</tr>
</tbody>
</table>

**Table 2-1. Description of Symbols in Each Frame**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>SOH</td>
<td>01H</td>
<td>Command frame header</td>
</tr>
<tr>
<td>STX</td>
<td>02H</td>
<td>Data frame header</td>
</tr>
<tr>
<td>LEN</td>
<td>–</td>
<td>Data length information (00H indicates 256).</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Command frame: COM + command information length</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Data frame: Data field length</td>
</tr>
<tr>
<td>COM</td>
<td>–</td>
<td>Command number</td>
</tr>
<tr>
<td>SUM</td>
<td>–</td>
<td>Checksum data for a frame</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Obtained by sequentially subtracting all of calculation target data from the initial value (00H) in 1-byte units (borrow is ignored). The calculation targets are as follows.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Command frame: LEN + COM + all of command information</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Data frame: LEN + all of data</td>
</tr>
<tr>
<td>ETB</td>
<td>17H</td>
<td>Footer of data frame other than the last frame</td>
</tr>
<tr>
<td>ETX</td>
<td>03H</td>
<td>Command frame footer, or footer of last data frame</td>
</tr>
</tbody>
</table>

The following shows examples of calculating the checksum (SUM) for a frame.
[Command frame]
No command information is included in the following example of a Chip Erase command frame, so LEN and COM are targets of checksum calculation.

<table>
<thead>
<tr>
<th>SOH</th>
<th>LEN</th>
<th>COM</th>
<th>SUM</th>
<th>ETX</th>
</tr>
</thead>
<tbody>
<tr>
<td>01H</td>
<td>01H</td>
<td>20H</td>
<td>Checksum</td>
<td>03H</td>
</tr>
</tbody>
</table>

Checksum calculation targets

For this command frame, checksum data is obtained as follows.

00H (initial value) – 01H (LEN) – 20H (COM) = DFH (Borrow ignored. Lower 8 bits only.)

The command frame finally transmitted is as follows.

<table>
<thead>
<tr>
<th>SOH</th>
<th>LEN</th>
<th>COM</th>
<th>SUM</th>
<th>ETX</th>
</tr>
</thead>
<tbody>
<tr>
<td>01H</td>
<td>01H</td>
<td>20H</td>
<td>DFH</td>
<td>03H</td>
</tr>
</tbody>
</table>

[Data frame]
To transmit a data frame as shown below, LEN and D1 to D4 are targets of checksum calculation.

<table>
<thead>
<tr>
<th>STX</th>
<th>LEN</th>
<th>D1</th>
<th>D2</th>
<th>D3</th>
<th>D4</th>
<th>SUM</th>
<th>ETX</th>
</tr>
</thead>
<tbody>
<tr>
<td>02H</td>
<td>04H</td>
<td>FFH</td>
<td>80H</td>
<td>40H</td>
<td>22H</td>
<td>Checksum</td>
<td>03H</td>
</tr>
</tbody>
</table>

Checksum calculation targets

For this data frame, checksum data is obtained as follows.

00H (initial value) – 04H (LEN) – FFH (D1) – 80H (D2) – 40H (D3) – 22H (D4) = 1BH (Borrow ignored. Lower 8 bits only.)

The data frame finally transmitted is as follows.

<table>
<thead>
<tr>
<th>STX</th>
<th>LEN</th>
<th>D1</th>
<th>D2</th>
<th>D3</th>
<th>D4</th>
<th>SUM</th>
<th>ETX</th>
</tr>
</thead>
<tbody>
<tr>
<td>02H</td>
<td>04H</td>
<td>FFH</td>
<td>80H</td>
<td>40H</td>
<td>22H</td>
<td>1BH</td>
<td>03H</td>
</tr>
</tbody>
</table>

When a data frame is received, the checksum data is calculated in the same manner, and the obtained value is used to detect a checksum error by judging whether the value is the same as that stored in the SUM field of the receive data. When a data frame as shown below is received, for example, a checksum error is detected.

<table>
<thead>
<tr>
<th>STX</th>
<th>LEN</th>
<th>D1</th>
<th>D2</th>
<th>D3</th>
<th>D4</th>
<th>SUM</th>
<th>ETX</th>
</tr>
</thead>
<tbody>
<tr>
<td>02H</td>
<td>04H</td>
<td>FFH</td>
<td>80H</td>
<td>40H</td>
<td>22H</td>
<td>1AH</td>
<td>03H</td>
</tr>
</tbody>
</table>

↑ Normally 1BH
2.1 Command Frame Transmission Processing

For details of the flowchart of processing to transmit command frames, read 4.1 Command Frame Transmission Processing Flowchart.

2.2 Data Frame Transmission Processing

The write data frame (user program), verify data frame (user program), and security data frame (security flag) are transmitted as a data frame.

For details of the flowchart of processing to transmit data frames, read 4.2 Data Frame Transmission Processing Flowchart.

2.3 Data Frame Reception Processing

The status frame, silicon signature data frame, version data frame, and checksum data frame are received as a data frame.

For details of the flowchart of processing to receive data frames, read 4.3 Data Frame Reception Processing Flowchart.
CHAPTER 3 DESCRIPTION OF COMMAND PROCESSING

3.1 Reset Command

3.1.1 Description

This command is used to check the establishment of communication between the programmer and the 78K0R/Kx3-L after the communication mode is set.

The same baud rate must be set for the programmer and 78K0R/Kx3-L, however, the 78K0R/Kx3-L cannot detect its own baud rate generation clock frequency so the baud rate cannot be set. The 78K0R/Kx3-L is enabled to detect the baud rate generation clock frequency by itself, when “00H” is transmitted twice at 9,600 bps from the programmer, and the 78K0R/Kx3-L measures the low-level width of “00H” and calculates the average of the two sent signals. The baud rate can consequently be set, which enables synchronous detection in communication.

3.1.2 Command frame and status frame

Figure 3-1 shows the format of a command frame for the Reset command, and Figure 3-2 shows the status frame for the command.

**Figure 3-1. Reset Command Frame (from Programmer to 78K0R/Kx3-L)**

<table>
<thead>
<tr>
<th>SOH</th>
<th>LEN</th>
<th>COM</th>
<th>SUM</th>
<th>ETX</th>
</tr>
</thead>
<tbody>
<tr>
<td>01H</td>
<td>01H</td>
<td>00H (Reset)</td>
<td>Checksum</td>
<td>03H</td>
</tr>
</tbody>
</table>

**Figure 3-2. Status Frame for Reset Command (from 78K0R/Kx3-L to Programmer)**

<table>
<thead>
<tr>
<th>STX</th>
<th>LEN</th>
<th>Data</th>
<th>SUM</th>
<th>ETX</th>
</tr>
</thead>
<tbody>
<tr>
<td>02H</td>
<td>1</td>
<td>ST1</td>
<td>Checksum</td>
<td>03H</td>
</tr>
</tbody>
</table>

**Remark**

ST1: Synchronization detection result

See **4.4 Reset Command** for details on the flowchart of the processing sequence between the programmer and the 78K0R/Kx3-L, the flowchart of command processing, and the sample program.
3.2 Baud Rate Set Command

3.2.1 Description
This command is used to change the baud rate for UART communication (9,600 bps by default).
After the Baud Rate Set command has been executed, the Reset command must be executed to check synchronization at the changed baud rate.

3.2.2 Command frame and status frame
Figure 3-3 shows the format of a command frame for the Baud Rate Set command, and Figure 3-4 shows the status frame for the command.

Figure 3-3. Baud Rate Set Command Frame (from Programmer to 78K0R/Kx3-L)

<table>
<thead>
<tr>
<th>SOH</th>
<th>LEN</th>
<th>COM</th>
<th>Command Information Note</th>
<th>SUM</th>
<th>ETX</th>
</tr>
</thead>
<tbody>
<tr>
<td>01H</td>
<td>06H</td>
<td>9AH</td>
<td>D01 D02H D02L D03 D04</td>
<td>Checksum</td>
<td>03H</td>
</tr>
</tbody>
</table>

Note  For details of the command information setting, refer to Table 3-1. If data other than in Table 3-1 is set, a time-out error will occur.
If a time-out error has occurred, execute a hardware reset and re-set the flash memory programming mode.

Remark D01: Synchronization correction mode
D02H, D02L: Baud rate setting
D03: Noise filter setting
D04: Flash rewriting voltage mode setting

Table 3-1. Command Information Setting

<table>
<thead>
<tr>
<th>Synchronization Correction Mode</th>
<th>D01</th>
<th>D02H</th>
<th>D02L</th>
<th>D03</th>
<th>D04</th>
</tr>
</thead>
<tbody>
<tr>
<td>Microcontroller correction mode</td>
<td>00H</td>
<td>Fixed to 00H</td>
<td>Fixed to 0AH (115,200 bps)</td>
<td>Noise filter 00H: Off 01H: On</td>
<td>00H: When writing in full-speed mode (2.7 V ≤ VDD ≤ 5.5 V) 01H: When writing in wide-voltage mode19 (1.8 V ≤ VDD ≤ 5.5 V)</td>
</tr>
<tr>
<td>Programmer correction mode</td>
<td>01H</td>
<td>Note 2</td>
<td>Note 2</td>
<td></td>
<td>Note 2</td>
</tr>
</tbody>
</table>

Notes 1. Support of the wide-voltage mode differs depending on the products. Check if it is supported by referring to the user’s manual of each product.
2. To communicate in the programmer correction mode, set a value to D02H/D02L by executing the following procedures using the programmer.
   <1> Measure the length of the READY pulse output from the microcontroller.
   <2> Calculate errors of the READY pulse (low-level 9 bits @ 9,600 bps).
   <3> Calculate the k value by using the following equation, taking errors in consideration.
     \[ k = \left( \frac{f_{IH} \times E}{2} \right) \times \text{(Baud rate \times 2)} \]
     E: READY pulse (9,600 bps) error when the flash memory programming mode has been set
   Example: E = 1.00 when 0% error for READY pulse (low-level 9 bits @ 9,600 bps) length
            E = 1.02 when +2% error for READY pulse (low-level 9 bits @ 9,600 bps) length
            E = 0.98 when −2% error for READY pulse (low-level 9 bits @ 9,600 bps) length
     f_{IH}: High-speed internal oscillator frequency
   <4> Convert the k value to a hexadecimal number.
<5> Set the value obtained in step <4> to D02H/D02L, and then execute the Baud Rate Set command.

However, steps <1> to <3> can be omitted if the following condition is satisfied.

**Condition:** All the k values are the same as a result of calculating with consideration for the deviation of the device's operating frequency. (The k value is rounded to a whole number.)

**Example:** If specifying 1 Mbps with \( f_{IH} = 20 \, \text{MHz} \pm 2\% \), k = 10 is obtained by using the following equations (D02H/D02L = 00H/0AH).

\[
\begin{align*}
\text{20.4 MHz (20 MHz + 2\%)} \\
&\quad k = \left( f_{IH} \times E \right) \div \left( \text{Baud rate} \times 2 \right) \\
&\quad = \left( 20.4 \times 10^6 \right) \div \left( 1 \times 10^5 \times 2 \right) \\
&\quad = 10.2 \\
&\quad \approx 10 \\
\text{20 MHz (20 MHz \pm 0\%)} \\
&\quad k = \left( f_{IH} \times E \right) \div \left( \text{Baud rate} \times 2 \right) \\
&\quad = \left( 20 \times 10^6 \right) \div \left( 1 \times 10^5 \times 2 \right) \\
&\quad = 10 \\
\text{19.6 MHz (20 MHz - 2\%)} \\
&\quad k = \left( f_{IH} \times E \right) \div \left( \text{Baud rate} \times 2 \right) \\
&\quad = \left( 19.6 \times 10^6 \right) \div \left( 1 \times 10^5 \times 2 \right) \\
&\quad = 9.8 \\
&\quad \approx 10 \\
\end{align*}
\]

**Figure 3-4. Status Frame for Baud Rate Set Command (from 78K0R/Kx3-L to Programmer)**

<table>
<thead>
<tr>
<th>STX</th>
<th>LEN</th>
<th>Data</th>
<th>SUM</th>
<th>ETX</th>
</tr>
</thead>
<tbody>
<tr>
<td>02H</td>
<td>01H</td>
<td>ST1</td>
<td>checksum</td>
<td>03H</td>
</tr>
</tbody>
</table>

**Remark** ST1: Synchronization detection result

See **4.5 Baud Rate Set Command** for details on the flowchart of the processing sequence between the programmer and the 78K0R/Kx3-L, the flowchart of command processing, and the sample program.
3.3 Chip Erase Command

3.3.1 Description

This command is used to erase the entire contents of the flash memory. In addition, all of the information that is set by security setting processing can be initialized by chip erase processing, as long as erasure is not prohibited by the security setting (see 3.11 Security Set Command).

3.3.2 Command frame and status frame

Figure 3-5 shows the format of a command frame for the Chip Erase command, and Figure 3-6 shows the status frame for the command.

Figure 3-5. Chip Erase Command Frame (from Programmer to 78K0R/Kx3-L)

<table>
<thead>
<tr>
<th>SOH</th>
<th>LEN</th>
<th>COM</th>
<th>SUM</th>
<th>ETX</th>
</tr>
</thead>
<tbody>
<tr>
<td>01H</td>
<td>01H</td>
<td>20H</td>
<td>Checksum</td>
<td>03H</td>
</tr>
</tbody>
</table>

(Chip Erase)

Figure 3-6. Status Frame for Chip Erase Command (from 78K0R/Kx3-L to Programmer)

<table>
<thead>
<tr>
<th>STX</th>
<th>LEN</th>
<th>Data</th>
<th>SUM</th>
<th>ETX</th>
</tr>
</thead>
<tbody>
<tr>
<td>02H</td>
<td>01H</td>
<td>ST1</td>
<td>Checksum</td>
<td>03H</td>
</tr>
</tbody>
</table>

Remark ST1: Chip erase result

See 4.6 Chip Erase Command for details on the flowchart of the processing sequence between the programmer and the 78K0R/Kx3-L, the flowchart of command processing, and the sample program.
3.4 Block Erase Command

3.4.1 Description
This command is used to erase the content of flash memory of the block with the specified number. A block can be specified with the first address of the block where erasing starts and the last address where erasing ends. Successive multiple blocks can be specified.

Erasing cannot be performed, however, if erasing is prohibited due to the security setting (see 3.11 Security Set Command).

3.4.2 Command frame and status frame
Figure 3-7 shows the format of a command frame for the Block Erase command, and Figure 3-8 shows the status frame for the command.

Figure 3-7. Block Erase Command Frame (from Programmer to 78K0R/Kx3-L)

<table>
<thead>
<tr>
<th>SOH</th>
<th>LEN</th>
<th>COM</th>
<th>Command Information</th>
<th>SUM</th>
<th>ETX</th>
</tr>
</thead>
<tbody>
<tr>
<td>01H</td>
<td>07H</td>
<td>22H (Block Erase)</td>
<td>SAH SAMS ALEAH EAMEAL</td>
<td>03H</td>
<td></td>
</tr>
</tbody>
</table>

Remark  SAH, SAM, SAL: Block erase start address (start address of any block)
SAH: Start address, high (bits 23 to 16)
SAM: Start address, middle (bits 15 to 8)
SAL: Start address, low (bits 7 to 0)
EAH, EAM, EAL: Block erase end address (last address of any block)
EAH: End address, high (bits 23 to 16)
EAM: End address, middle (bits 15 to 8)
EAL: End address, low (bits 7 to 0)

Figure 3-8. Status Frame for Block Erase Command (from 78K0R/Kx3-L to Programmer)

<table>
<thead>
<tr>
<th>STX</th>
<th>LEN</th>
<th>Data</th>
<th>SUM</th>
<th>ETX</th>
</tr>
</thead>
<tbody>
<tr>
<td>02H</td>
<td>01H</td>
<td>ST1</td>
<td>Checksum</td>
<td>03H</td>
</tr>
</tbody>
</table>

Remark  ST1: Block erase result

See 4.7 Block Erase Command for details on the flowchart of the processing sequence between the programmer and the 78K0R/Kx3-L, the flowchart of command processing, and the sample program.
3.5 Programming Command

3.5.1 Description
This command is used to write the user program to the flash memory by transmitting write data after having transmitted the write start address and the write end address. Internal verification is then executed after the last data has been transmitted and writing has been completed.

The write start/end address can be set only in the block start/end address units.

If both of the status frames (ST1 and ST2) after the last data transmission indicate ACK, the 78K0R/Kx3-L firmware automatically executes internal verify. Therefore, the Status command for this internal verify must be transmitted.

3.5.2 Command frame and status frame
Figure 3-9 shows the format of a command frame for the Programming command, and Figure 3-10 shows the status frame for the command.

Figure 3-9. Programming Command Frame (from Programmer to 78K0R/Kx3-L)

<table>
<thead>
<tr>
<th>SOH</th>
<th>LEN</th>
<th>COM</th>
<th>Command Information</th>
<th>SUM</th>
<th>ETX</th>
</tr>
</thead>
<tbody>
<tr>
<td>01H</td>
<td>07H</td>
<td>40H</td>
<td>(Programming)</td>
<td>SAH</td>
<td>SAM</td>
</tr>
</tbody>
</table>

Remark  SAH, SAM, SAL: Write start addresses  EAH, EAM, EAL: Write end addresses

Figure 3-10. Status Frame for Programming Command (from 78K0R/Kx3-L to Programmer)

<table>
<thead>
<tr>
<th>STX</th>
<th>LEN</th>
<th>Data</th>
<th>SUM</th>
<th>ETX</th>
</tr>
</thead>
<tbody>
<tr>
<td>02H</td>
<td>01H</td>
<td>ST1 (a)</td>
<td>Checksum</td>
<td>03H</td>
</tr>
</tbody>
</table>

Remark  ST1 (a): Command reception result

3.5.3 Data frame and status frame
Figure 3-11 shows the format of a frame that includes data to be written, and Figure 3-12 shows the status frame for the data.

Figure 3-11. Data Frame to Be Written (from Programmer to 78K0R/Kx3-L)

<table>
<thead>
<tr>
<th>STX</th>
<th>LEN</th>
<th>Data</th>
<th>SUM</th>
<th>ETX/ETB</th>
</tr>
</thead>
<tbody>
<tr>
<td>02H</td>
<td>00H to FFH (00H = 256)</td>
<td>Write Data</td>
<td>Checksum</td>
<td>03H/17H</td>
</tr>
</tbody>
</table>

Remark  Write Data: User program to be written

Figure 3-12. Status Frame for Data Frame (from 78K0R/Kx3-L to Programmer)

<table>
<thead>
<tr>
<th>STX</th>
<th>LEN</th>
<th>Data</th>
<th>SUM</th>
<th>ETX</th>
</tr>
</thead>
<tbody>
<tr>
<td>02H</td>
<td>02H</td>
<td>ST1 (b)</td>
<td>ST2 (b)</td>
<td>Checksum</td>
</tr>
</tbody>
</table>

Remark  ST1 (b): Data reception check result  ST2 (b): Write result
3.5.4 Completion of transferring all data and status frame

Figure 3-13 shows the status frame after transfer of all data is completed.

Figure 3-13. Status Frame After Completion of Transferring All Data (from 78K0R/Kx3-L to Programmer)

<p>| | | | | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>STX</td>
<td>LEN</td>
<td>Data</td>
<td>SUM</td>
<td>ETX</td>
</tr>
<tr>
<td>02H</td>
<td>01H</td>
<td>ST1 (c)</td>
<td>Checksum</td>
<td>03H</td>
</tr>
</tbody>
</table>

**Remark**  ST1 (c): Internal verify result

See 4.8 Programming Command for details on the flowchart of the processing sequence between the programmer and the 78K0R/Kx3-L, the flowchart of command processing, and the sample program.
3.6 Verify Command

3.6.1 Description
This command is used to compare the data transmitted from the programmer with the data read from the 78K0R/Kx3-L (read level) in the specified address range, and check whether they match.
The verify start/end address can be set only in the block start/end address units.

3.6.2 Command frame and status frame
Figure 3-14 shows the format of a command frame for the Verify command, and Figure 3-15 shows the status frame for the command.

Figure 3-14. Verify Command Frame (from Programmer to 78K0R/Kx3-L)

<table>
<thead>
<tr>
<th>SOH</th>
<th>LEN</th>
<th>COM</th>
<th>Command Information</th>
<th>SUM</th>
<th>ETX</th>
</tr>
</thead>
<tbody>
<tr>
<td>01H</td>
<td>07H</td>
<td>13H</td>
<td>SAH, SAM, SAL</td>
<td>03H</td>
<td></td>
</tr>
</tbody>
</table>

Remark SAH, SAM, SAL: Verify start addresses
EAH, EAM, EAL: Verify end addresses

Figure 3-15. Status Frame for Verify Command (from 78K0R/Kx3-L to Programmer)

<table>
<thead>
<tr>
<th>STX</th>
<th>LEN</th>
<th>Data</th>
<th>SUM</th>
<th>ETX</th>
</tr>
</thead>
<tbody>
<tr>
<td>02H</td>
<td>01H</td>
<td>ST1 (a)</td>
<td>03H</td>
<td></td>
</tr>
</tbody>
</table>

Remark ST1 (a): Command reception result

3.6.3 Data frame and status frame
Figure 3-16 shows the format of a frame that includes data to be verified, and Figure 3-17 shows the status frame for the data.

Figure 3-16. Data Frame of Data to Be Verified (from Programmer to 78K0R/Kx3-L)

<table>
<thead>
<tr>
<th>STX</th>
<th>LEN</th>
<th>Data</th>
<th>SUM</th>
<th>ETX/ETB</th>
</tr>
</thead>
<tbody>
<tr>
<td>02H</td>
<td>00H to FFH (00H = 256)</td>
<td>Verify Data</td>
<td>03H/17H</td>
<td></td>
</tr>
</tbody>
</table>

Remark Verify Data: User program to be verified
Figure 3-17. Status Frame for Data Frame (from 78K0R/Kx3-L to Programmer)

<table>
<thead>
<tr>
<th>STX</th>
<th>LEN</th>
<th>Data</th>
<th>SUM</th>
<th>ETX</th>
</tr>
</thead>
<tbody>
<tr>
<td>02H</td>
<td>02H</td>
<td>ST1 (b)</td>
<td>ST2 (b)</td>
<td>03H</td>
</tr>
</tbody>
</table>

**Remark**  
ST1 (b): Data reception check result  
ST2 (b): Verify result<sup>Note</sup>

**Note**  
Even if a verify error occurs in the specified address range, ACK is always returned as the verify result. The status of all verify errors are reflected in the verify result for the last data. Therefore, the occurrence of verify errors can be checked only when all the verify processing for the specified address range is completed.

See 4.9 Verify Command for details on the flowchart of the processing sequence between the programmer and the 78K0R/Kx3-L, the flowchart of command processing, and the sample program.
3.7 Block Blank Check Command

3.7.1 Description
This command is used to check if a block in the flash memory, with a specified block number, is blank (erased state).

A block can be specified with the start address of the blank check start block and the last address of the blank check end block. Successive multiple blocks can be specified.

3.7.2 Command frame and status frame
Figure 3-18 shows the format of a command frame for the Block Blank Check command, and Figure 3-19 shows the status frame for the command.

**Figure 3-18. Block Blank Check Command Frame (from Programmer to 78K0R/Kx3-L)**

<table>
<thead>
<tr>
<th>SOH</th>
<th>LEN</th>
<th>COM</th>
<th>Command Information</th>
<th>SUM</th>
<th>ETX</th>
</tr>
</thead>
<tbody>
<tr>
<td>01H</td>
<td>08H</td>
<td>32H</td>
<td>Block Blank Check</td>
<td>SAH</td>
<td>SAM</td>
</tr>
</tbody>
</table>

**Remark**
SAH, SAM, SAL: Block blank check start address (start address of any block)
SAH: Start address, high (bits 23 to 16)
SAM: Start address, middle (bits 15 to 8)
SAL: Start address, low (bits 7 to 0)
EAH, EAM, EAL: Block blank check end address (last address of any block)
EAH: End address, high (bits 23 to 16)
EAM: End address, middle (bits 15 to 8)
EAL: End address, low (bits 7 to 0)
D01: 00H: When performing a block blank check for a single block
01H: When performing a block blank check for the complete area before erasing the chip

**Figure 3-19. Status Frame for Block Blank Check Command (from 78K0R/Kx3-L to Programmer)**

<table>
<thead>
<tr>
<th>STX</th>
<th>LEN</th>
<th>Data</th>
<th>SUM</th>
<th>ETX</th>
</tr>
</thead>
<tbody>
<tr>
<td>02H</td>
<td>01H</td>
<td>ST1</td>
<td>Checksum</td>
<td>03H</td>
</tr>
</tbody>
</table>

**Remark**
ST1: Block blank check result

See 4.10 Block Blank Check Command for details on the flowchart of the processing sequence between the programmer and the 78K0R/Kx3-L, the flowchart of command processing, and the sample program.
3.8 Silicon Signature Command

3.8.1 Description
This command is used to read information such as the write protocol information (silicon signature) of the device and security flag information.

If the programmer supports a programming protocol that is not supported in the 78K0R/Kx3-L, for example, execute this command to select an appropriate protocol in accordance with the values of the second and third bytes.

3.8.2 Command frame and status frame
Figure 3-20 shows the format of a command frame for the Silicon Signature command, and Figure 3-21 shows the status frame for the command.

![Figure 3-20. Silicon Signature Command Frame (from Programmer to 78K0R/Kx3-L)](image)

<table>
<thead>
<tr>
<th>SOH</th>
<th>LEN</th>
<th>COM</th>
<th>SUM</th>
<th>ETX</th>
</tr>
</thead>
<tbody>
<tr>
<td>01H</td>
<td>01H</td>
<td>C0H</td>
<td>Checksum</td>
<td>03H</td>
</tr>
</tbody>
</table>

(Silicon Signature)

![Figure 3-21. Status Frame for Silicon Signature Command (from 78K0R/Kx3-L to Programmer)](image)

<table>
<thead>
<tr>
<th>STX</th>
<th>LEN</th>
<th>Data</th>
<th>SUM</th>
<th>ETX</th>
</tr>
</thead>
<tbody>
<tr>
<td>02H</td>
<td>01H</td>
<td>ST1</td>
<td>Checksum</td>
<td>03H</td>
</tr>
</tbody>
</table>

Remark ST1: Command reception result
3.8.3 Silicon signature data frame

Figure 3-22 shows the format of a frame that includes silicon signature data.

**Figure 3-22. Silicon Signature Data Frame (from 78K0R/Kx3-L to Programmer)**

<table>
<thead>
<tr>
<th>STX</th>
<th>LEN</th>
<th>VEN</th>
<th>MET</th>
<th>MSC</th>
<th>DEC1</th>
<th>DEC2</th>
<th>DEC3</th>
<th>UAE(3)</th>
<th>DEV(10)</th>
</tr>
</thead>
<tbody>
<tr>
<td>02H</td>
<td>n</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Data (continued)

| SCF | BOT | FSWSH | FSWSL | FSWEH | FSWEL | RES(2) | Checksum | 03H |

**Remarks 1.**

- **n (LEN):** Data length
- **VEN:** Vendor code (NEC: 10H)
- **MET:** Macro extension code
- **MSC:** Macro function code
- **DEC1:** Device extension code 1
- **DEC2:** Device extension code 2
- **DEC3:** Device extension code 3
- **UAE:** User flash ROM last address (3 bytes)
- **DEV:** Device name (10 bytes)
- **SCF:** Security flag information
- **BOT:** Boot block number
- **FSWSH:** Higher 8-bit side of flash shield window (FSW) start block
- **FSWSL:** Lower 8-bit side of flash shield window (FSW) start block
- **FSWEH:** Higher 8-bit side of flash shield window (FSW) end block
- **FSWEL:** Lower 8-bit side of flash shield window (FSW) end block
- **RES:** Reserved (2 bytes)

2. For the vendor code (VEN), extension code (MET), function code (MSC), device extension code 1 (DEC1), device extension code 2 (DEC2), and device extension code 3 (DEC3), the lower 7 bits are used as data entity, and the highest bit is used as an odd parity. The following shows an example.
Table 3-2. Example of Silicon Signature Data (μPD78F1000 (78K0R/KC3-L))

<table>
<thead>
<tr>
<th>Field Name</th>
<th>Content</th>
<th>Length (Byte)</th>
<th>Example of Silicon Signature Data</th>
<th>Actual Value</th>
<th>Parity</th>
</tr>
</thead>
<tbody>
<tr>
<td>VEN</td>
<td>Vendor code (NEC)</td>
<td>1</td>
<td>10H (00010000B )</td>
<td>10H</td>
<td>Added</td>
</tr>
<tr>
<td>MET</td>
<td>Macro extension code</td>
<td>1</td>
<td>EFH (11101111B )</td>
<td>EFH</td>
<td>Added</td>
</tr>
<tr>
<td>MSC</td>
<td>Macro function code</td>
<td>1</td>
<td>04H (01000000B )</td>
<td>04H</td>
<td>Added</td>
</tr>
<tr>
<td>DEC1</td>
<td>Device extension code 1</td>
<td>1</td>
<td>DCH (11011100B )</td>
<td>DCH</td>
<td>Added</td>
</tr>
<tr>
<td>DEC2</td>
<td>Device extension code 2</td>
<td>1</td>
<td>FDH (11111101B )</td>
<td>FDH</td>
<td>Added</td>
</tr>
<tr>
<td>DEC3</td>
<td>Device extension code 3</td>
<td>1</td>
<td>FDH (11111101B )</td>
<td>FDH</td>
<td>Added</td>
</tr>
<tr>
<td>UAE</td>
<td>User flash ROM last address</td>
<td>3</td>
<td>FFH (11111111B )</td>
<td>003FFFH</td>
<td>Not added</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>3FH (00111111B )</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>00H (00000000B )</td>
<td></td>
<td></td>
</tr>
<tr>
<td>DEV</td>
<td>Device name</td>
<td>10</td>
<td>44H (01000100B ) = ‘D’</td>
<td>‘D’</td>
<td>Not added</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>37H (00110111B ) = ‘7’</td>
<td>‘7’</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>38H (00111000B ) = ‘8’</td>
<td>‘8’</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>46H (01000110B ) = ‘F’</td>
<td>‘F’</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>31H (00110001B ) = ‘1’</td>
<td>‘1’</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>30H (00110000B ) = ‘0’</td>
<td>‘0’</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>30H (00110000B ) = ‘0’</td>
<td>‘0’</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>20H (00100001B ) = ‘ ‘</td>
<td>‘ ‘</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>20H (00100000B ) = ‘ ‘</td>
<td>‘ ‘</td>
<td></td>
</tr>
<tr>
<td>SCF</td>
<td>Security flag information</td>
<td>1</td>
<td>Any</td>
<td>Same as left column</td>
<td>Not added</td>
</tr>
<tr>
<td>BOT</td>
<td>Boot block number (fixed)</td>
<td>1</td>
<td>03H (00000011B )</td>
<td>03H</td>
<td>Not added</td>
</tr>
<tr>
<td>FSWS(H)</td>
<td>Higher 8-bit side of flash shield window start block</td>
<td>1</td>
<td>Any</td>
<td>Same as left column</td>
<td>Not added</td>
</tr>
<tr>
<td>FSWS(L)</td>
<td>Lower 8-bit side of flash shield window start block</td>
<td>1</td>
<td>Any</td>
<td>Same as left column</td>
<td>Not added</td>
</tr>
<tr>
<td>FSWE(H)</td>
<td>Higher 8-bit side of flash shield window end block</td>
<td>1</td>
<td>Any</td>
<td>Same as left column</td>
<td>Not added</td>
</tr>
<tr>
<td>FSWE(L)</td>
<td>Lower 8-bit side of flash shield window end block</td>
<td>1</td>
<td>Any</td>
<td>Same as left column</td>
<td>Not added</td>
</tr>
<tr>
<td>RES</td>
<td>Reserved</td>
<td>2</td>
<td>FFFFH (1111111111111111B)</td>
<td>FFFFH</td>
<td>Not added</td>
</tr>
</tbody>
</table>

See 4.11 Silicon Signature Command for details on the flowchart of the processing sequence between the programmer and the 78K0R/Kx3-L, the flowchart of command processing, and the sample program.
3.8.4 Silicon signature list

(1) 78K0R/Kx3-L silicon signature list

Table 3-3. 78K0R/Kx3-L Silicon Signature Data List

<table>
<thead>
<tr>
<th>Item</th>
<th>Description</th>
<th>Length (Byte)</th>
<th>Data (Hex)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vendor code</td>
<td>NEC</td>
<td>1</td>
<td>10</td>
</tr>
<tr>
<td>Extension code</td>
<td>Extension code</td>
<td>1</td>
<td>7F</td>
</tr>
<tr>
<td>Function code</td>
<td>Function information</td>
<td>1</td>
<td>04</td>
</tr>
<tr>
<td>Device information</td>
<td>Device information</td>
<td>3</td>
<td>DC</td>
</tr>
<tr>
<td>Internal flash ROM last address</td>
<td>Transmitted from lower bytes of address</td>
<td>3</td>
<td>Note 1</td>
</tr>
<tr>
<td>Device name (μPD)</td>
<td>78F1000/78F1001/78F1002/78F1003 78F1004/78F1005/78F1006 78F1007/78F1008/78F1009 78F1010/78F1011/78F1012 78F1013/78F1014</td>
<td>10</td>
<td>Note 2</td>
</tr>
<tr>
<td>Security information</td>
<td>Security information</td>
<td>1</td>
<td>Any</td>
</tr>
<tr>
<td>Boot block number</td>
<td>The last block number of the boot cluster that is currently selected</td>
<td>1</td>
<td>03</td>
</tr>
<tr>
<td>FSW block number</td>
<td>FSW information</td>
<td>4</td>
<td>Any</td>
</tr>
<tr>
<td>Reserved</td>
<td>Reserved</td>
<td>2</td>
<td>FFFF</td>
</tr>
</tbody>
</table>

Note 1. The list of internal-flash-ROM last addresses is as follows.

<table>
<thead>
<tr>
<th>Item</th>
<th>Description</th>
<th>Length (Byte)</th>
<th>Data (Hex)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Internal flash ROM last address</td>
<td>16 KB (003FFFH)</td>
<td>3</td>
<td>FF3F00</td>
</tr>
<tr>
<td></td>
<td>32 KB (007FFFH)</td>
<td></td>
<td>FF7F00</td>
</tr>
<tr>
<td></td>
<td>48 KB (00BFFFH)</td>
<td></td>
<td>FFBF00</td>
</tr>
<tr>
<td></td>
<td>64 KB (00FFFFH)</td>
<td></td>
<td>FFFF00</td>
</tr>
<tr>
<td></td>
<td>96 KB (017FFFH)</td>
<td></td>
<td>FF7F01</td>
</tr>
<tr>
<td></td>
<td>128 KB (01FFFFH)</td>
<td></td>
<td>FFFF01</td>
</tr>
</tbody>
</table>

(Note 2 is on the next page.)
Note 2. The device names are listed below.

<table>
<thead>
<tr>
<th>Generic Name</th>
<th>Part Number</th>
<th>Length (Bytes)</th>
<th>Actual Value</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>78K0R/KC3-L</td>
<td>D78F1000</td>
<td>10</td>
<td>44 37 38 46 31 30 30 20 20</td>
<td>D 7 8 F 1 0 0 0 – –</td>
</tr>
<tr>
<td></td>
<td>D78F1001</td>
<td></td>
<td>44 37 38 46 31 30 30 31 20 20</td>
<td>D 7 8 F 1 0 0 1 – –</td>
</tr>
<tr>
<td></td>
<td>D78F1002</td>
<td></td>
<td>44 37 38 46 31 30 30 32 20 20</td>
<td>D 7 8 F 1 0 0 2 – –</td>
</tr>
<tr>
<td></td>
<td>D78F1003</td>
<td></td>
<td>44 37 38 46 31 30 30 33 20 20</td>
<td>D 7 8 F 1 0 0 3 – –</td>
</tr>
<tr>
<td>78K0R/KD3-L</td>
<td>D78F1004</td>
<td></td>
<td>44 37 38 46 31 30 30 34 20 20</td>
<td>D 7 8 F 1 0 0 4 – –</td>
</tr>
<tr>
<td></td>
<td>D78F1005</td>
<td></td>
<td>44 37 38 46 31 30 30 35 20 20</td>
<td>D 7 8 F 1 0 0 5 – –</td>
</tr>
<tr>
<td></td>
<td>D78F1006</td>
<td></td>
<td>44 37 38 46 31 30 30 36 20 20</td>
<td>D 7 8 F 1 0 0 6 – –</td>
</tr>
<tr>
<td>78K0R/KE3-L</td>
<td>D78F1007</td>
<td></td>
<td>44 37 38 46 31 30 30 37 20 20</td>
<td>D 7 8 F 1 0 0 7 – –</td>
</tr>
<tr>
<td></td>
<td>D78F1008</td>
<td></td>
<td>44 37 38 46 31 30 30 38 20 20</td>
<td>D 7 8 F 1 0 0 8 – –</td>
</tr>
<tr>
<td></td>
<td>D78F1009</td>
<td></td>
<td>44 37 38 46 31 30 30 39 20 20</td>
<td>D 7 8 F 1 0 0 9 – –</td>
</tr>
<tr>
<td>78K0R/KF3-L</td>
<td>D78F1010</td>
<td></td>
<td>44 37 38 46 31 30 30 31 20 20</td>
<td>D 7 8 F 1 0 1 0 – –</td>
</tr>
<tr>
<td></td>
<td>D78F1011</td>
<td></td>
<td>44 37 38 46 31 30 31 31 20 20</td>
<td>D 7 8 F 1 0 1 1 – –</td>
</tr>
<tr>
<td></td>
<td>D78F1012</td>
<td></td>
<td>44 37 38 46 31 30 31 32 20 20</td>
<td>D 7 8 F 1 0 1 2 – –</td>
</tr>
<tr>
<td>78K0R/KG3-L</td>
<td>D78F1013</td>
<td></td>
<td>44 37 38 46 31 30 31 33 20 20</td>
<td>D 7 8 F 1 0 1 3 – –</td>
</tr>
<tr>
<td></td>
<td>D78F1014</td>
<td></td>
<td>44 37 38 46 31 30 31 34 20 20</td>
<td>D 7 8 F 1 0 1 4 – –</td>
</tr>
</tbody>
</table>
(2) 78K0R/Ix3 silicon signature list

Table 3-4. 78K0R/Ix3 Silicon Signature Data List

<table>
<thead>
<tr>
<th>Item</th>
<th>Description</th>
<th>Length (Byte)</th>
<th>Data (Hex)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vendor code</td>
<td>NEC</td>
<td>1</td>
<td>10</td>
</tr>
<tr>
<td>Extension code</td>
<td>Extension code</td>
<td>1</td>
<td>7F</td>
</tr>
<tr>
<td>Function code</td>
<td>Function information</td>
<td>1</td>
<td>04</td>
</tr>
<tr>
<td>Device information</td>
<td>Device information</td>
<td>3</td>
<td>DC FD FD</td>
</tr>
<tr>
<td>Internal flash ROM last address</td>
<td>Transmitted from lower bytes of address</td>
<td>3</td>
<td>Note 1</td>
</tr>
<tr>
<td>Device name (μPD)</td>
<td>78F1201/78F1203</td>
<td>10</td>
<td>Note 2</td>
</tr>
<tr>
<td></td>
<td>78F1211/78F1213/78F1214/78F1215</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>78F1223/78F1224/78F1225</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>78F1233/78F1234/78F1235</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Security information</td>
<td>Security information</td>
<td>1</td>
<td>Any</td>
</tr>
<tr>
<td>Boot block number</td>
<td>The last block number of the boot cluster that is currently selected</td>
<td>1</td>
<td>03</td>
</tr>
<tr>
<td>FSW block number</td>
<td>FSW information</td>
<td>4</td>
<td>Any</td>
</tr>
<tr>
<td>Reserved</td>
<td>Reserved</td>
<td>2</td>
<td>FFFF</td>
</tr>
</tbody>
</table>

**Note 1.** The list of internal-flash-ROM last addresses is as follows.

<table>
<thead>
<tr>
<th>Item</th>
<th>Description</th>
<th>Length (Byte)</th>
<th>Data (Hex)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Internal flash ROM last address</td>
<td>16 KB (003FFFH)</td>
<td>3</td>
<td>FF3F00</td>
</tr>
<tr>
<td></td>
<td>32 KB (007FFFH)</td>
<td></td>
<td>FF7F00</td>
</tr>
<tr>
<td></td>
<td>48 KB (00BFFFH)</td>
<td></td>
<td>FBF00</td>
</tr>
<tr>
<td></td>
<td>64 KB (00FFFFH)</td>
<td></td>
<td>FFFF00</td>
</tr>
</tbody>
</table>

(Note 2 is on the next page.)
Note 2. The device names are listed below.

### Device Name List

<table>
<thead>
<tr>
<th>Generic Name</th>
<th>Part Number</th>
<th>Length (Bytes)</th>
<th>Actual Value</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>10</td>
<td></td>
</tr>
<tr>
<td>78K0R/IB3</td>
<td>D78F1221</td>
<td>44 37 38 46 31 32 31 20 20</td>
<td>D 7 8 F 1 2 2 2 1 – –</td>
</tr>
<tr>
<td></td>
<td>D78F1222</td>
<td>44 37 38 46 31 32 32 20 20</td>
<td>– –</td>
</tr>
<tr>
<td>78K0R/IC3</td>
<td>D78F1211</td>
<td>44 37 38 46 31 32 31 20 20</td>
<td>D 7 8 F 1 2 2 2 1 – –</td>
</tr>
<tr>
<td></td>
<td>D78F1213</td>
<td>44 37 38 46 31 32 31 33 20 20</td>
<td>D 7 8 F 1 2 1 3 – –</td>
</tr>
<tr>
<td></td>
<td>D78F1214</td>
<td>44 37 38 46 31 32 31 34 20 20</td>
<td>D 7 8 F 1 2 1 4 – –</td>
</tr>
<tr>
<td></td>
<td>D78F1215</td>
<td>44 37 38 46 31 32 31 5 20 20</td>
<td>D 7 8 F 1 2 1 5 – –</td>
</tr>
<tr>
<td>78K0R/ID3</td>
<td>D78F1223</td>
<td>44 37 38 46 31 32 32 33 20 20</td>
<td>D 7 8 F 1 2 2 2 3 – –</td>
</tr>
<tr>
<td></td>
<td>D78F1224</td>
<td>44 37 38 46 31 32 32 34 20 20</td>
<td>D 7 8 F 1 2 2 4 – –</td>
</tr>
<tr>
<td></td>
<td>D78F1225</td>
<td>44 37 38 46 31 32 32 35 20 20</td>
<td>D 7 8 F 1 2 2 5 – –</td>
</tr>
<tr>
<td>78K0R/IE3</td>
<td>D78F1233</td>
<td>44 37 38 46 31 32 33 33 20 20</td>
<td>D 7 8 F 1 2 2 3 3 – –</td>
</tr>
<tr>
<td></td>
<td>D78F1234</td>
<td>44 37 38 46 31 32 33 34 20 20</td>
<td>D 7 8 F 1 2 2 3 4 – –</td>
</tr>
<tr>
<td></td>
<td>D78F1235</td>
<td>44 37 38 46 31 32 33 35 20 20</td>
<td>D 7 8 F 1 2 2 3 5 – –</td>
</tr>
</tbody>
</table>
### (3) 78K0R/Kx3-C silicon signature list

#### Table 3-5. 78K0R/Kx3-C Silicon Signature Data List

<table>
<thead>
<tr>
<th>Item</th>
<th>Description</th>
<th>Length (Byte)</th>
<th>Data (Hex)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vendor code</td>
<td>NEC</td>
<td>1</td>
<td>10</td>
</tr>
<tr>
<td>Extension code</td>
<td>Extension code</td>
<td>1</td>
<td>7F</td>
</tr>
<tr>
<td>Function code</td>
<td>Function information</td>
<td>1</td>
<td>04</td>
</tr>
<tr>
<td>Device information</td>
<td>Device information</td>
<td>3</td>
<td>DC</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>FD</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>FD</td>
</tr>
<tr>
<td>Internal flash ROM</td>
<td>Transmitted from lower bytes of</td>
<td>3</td>
<td>Note 1</td>
</tr>
<tr>
<td>last address</td>
<td>address</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Device name (μPD)</td>
<td>78F1846/78F1847</td>
<td>10</td>
<td>Note 2</td>
</tr>
<tr>
<td></td>
<td>78F1848/78F1849</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Security information</td>
<td>Security information</td>
<td>1</td>
<td>Any</td>
</tr>
<tr>
<td>Boot block number</td>
<td>The last block number of the boot</td>
<td>1</td>
<td>03</td>
</tr>
<tr>
<td></td>
<td>cluster that is currently selected</td>
<td></td>
<td></td>
</tr>
<tr>
<td>FSW block number</td>
<td>FSW information</td>
<td>4</td>
<td>Any</td>
</tr>
<tr>
<td>Reserved</td>
<td>Reserved</td>
<td>2</td>
<td>FFFF</td>
</tr>
</tbody>
</table>

**Notes**

1. The list of internal-flash-ROM last addresses is as follows.

<table>
<thead>
<tr>
<th>Item</th>
<th>Description</th>
<th>Length (Byte)</th>
<th>Data (Hex)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Internal flash ROM</td>
<td>96 KB (017FFFH)</td>
<td>3</td>
<td>FF7F01</td>
</tr>
<tr>
<td>last address</td>
<td>128 KB (01FFFFFFH)</td>
<td></td>
<td>FFFF01</td>
</tr>
</tbody>
</table>

2. The device names are listed below.

#### Device name list

<table>
<thead>
<tr>
<th>Generic Name</th>
<th>Part Number</th>
<th>Length (Bytes)</th>
<th>Actual Value</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>Upper Row: Signature Data</td>
</tr>
<tr>
<td>78K0R/KF3-C</td>
<td>D78F1846</td>
<td>10</td>
<td></td>
</tr>
<tr>
<td></td>
<td>D78F1847</td>
<td>10</td>
<td>D 7 8 F 1 8 4 7 – –</td>
</tr>
<tr>
<td>78K0R/KG3-C</td>
<td>D78F1848</td>
<td>10</td>
<td>D 7 8 F 1 8 4 8 – –</td>
</tr>
<tr>
<td></td>
<td>D78F1849</td>
<td>10</td>
<td>D 7 8 F 1 8 4 9 – –</td>
</tr>
</tbody>
</table>
3.9 Version Get Command

3.9.1 Description
This command is used to acquire information on the 78K0R/Kx3-L device version and firmware version. The device version value is fixed to 00H. Use this command when the programming parameters must be changed in accordance with the 78K0R/Kx3-L firmware version.

Caution The firmware version may be updated during firmware update that does not affect the change of flash programming parameters (at this time, update of the firmware version is not reported).

Example Firmware version and reprogramming parameters

<table>
<thead>
<tr>
<th>Firmware version</th>
<th>Programming parameters</th>
</tr>
</thead>
<tbody>
<tr>
<td>V1.00</td>
<td>Parameter A</td>
</tr>
<tr>
<td>V2.00</td>
<td>Parameter B</td>
</tr>
<tr>
<td>V3.00</td>
<td></td>
</tr>
</tbody>
</table>

Upgrade that requires changing of flash programming parameters
Upgrade of items that does not affect the change of flash programming parameters

3.9.2 Command frame and status frame
Figure 3-23 shows the format of a command frame for the Version Get command, and Figure 3-24 shows the status frame for the command.

Figure 3-23. Version Get Command Frame (from Programmer to 78K0R/Kx3-L)

<table>
<thead>
<tr>
<th>SOH</th>
<th>LEN</th>
<th>COM</th>
<th>SUM</th>
<th>ETX</th>
</tr>
</thead>
<tbody>
<tr>
<td>01H</td>
<td>01H</td>
<td>C5H</td>
<td>Checksum</td>
<td>03H</td>
</tr>
</tbody>
</table>

Figure 3-24. Status Frame for Version Get Command (from 78K0R/Kx3-L to Programmer)

<table>
<thead>
<tr>
<th>STX</th>
<th>LEN</th>
<th>Data</th>
<th>SUM</th>
<th>ETX</th>
</tr>
</thead>
<tbody>
<tr>
<td>02H</td>
<td>01H</td>
<td>ST1</td>
<td>Checksum</td>
<td>03H</td>
</tr>
</tbody>
</table>

Remark ST1: Command reception result
3.9.3 Version data frame

Figure 3-25 shows the data frame of version data.

Figure 3-25. Version Data Frame (from 78K0R/Kx3-L to Programmer)

<table>
<thead>
<tr>
<th>STX</th>
<th>LEN</th>
<th>Data</th>
<th>SUM</th>
<th>ETX</th>
</tr>
</thead>
<tbody>
<tr>
<td>02H</td>
<td>06H</td>
<td>DV1</td>
<td>DV2</td>
<td>DV3</td>
</tr>
</tbody>
</table>

Remark
- DV1: Integer of device version (fixed to 00H)
- DV2: First decimal place of device version (fixed to 00H)
- DV3: Second decimal place of device version (fixed to 00H)
- FV1: Integer of firmware version
- FV2: First decimal place of firmware version
- FV3: Second decimal place of firmware version

See 4.12 Version Get Command for details on the flowchart of the processing sequence between the programmer and the 78K0R/Kx3-L, the flowchart of command processing, and the sample program.
3.10 Checksum Command

3.10.1 Description
This command is used to acquire the checksum data in the specified area.

For the checksum calculation start/end address, specify a fixed address in block units (1 KB) starting from the top of the flash memory.

Checksum data is obtained by sequentially subtracting data in the specified address range from the initial value (0000H) in 1-byte units.

3.10.2 Command frame and status frame
Figure 3-26 shows the format of a command frame for the Checksum command, and Figure 3-27 shows the status frame for the command.

Figure 3-26. Checksum Command Frame (from Programmer to 78K0R/Kx3-L)

<table>
<thead>
<tr>
<th>SOH</th>
<th>LEN</th>
<th>COM</th>
<th>Command Information</th>
<th>SUM</th>
<th>ETX</th>
</tr>
</thead>
<tbody>
<tr>
<td>01H</td>
<td>07H</td>
<td>0BH</td>
<td>SAH  SAM  SAL  EAH  EAM  EAL</td>
<td>Checksum</td>
<td>03H</td>
</tr>
</tbody>
</table>

Remark
SAH, SAM, SAL: Checksum calculation start addresses
EAH, EAM, EAL: Checksum calculation end addresses

Figure 3-27. Status Frame for Checksum Command (from 78K0R/Kx3-L to Programmer)

<table>
<thead>
<tr>
<th>STX</th>
<th>LEN</th>
<th>Data</th>
<th>SUM</th>
<th>ETX</th>
</tr>
</thead>
<tbody>
<tr>
<td>02H</td>
<td>01H</td>
<td>ST1</td>
<td>Checksum</td>
<td>03H</td>
</tr>
</tbody>
</table>

Remark
ST1: Command reception result

3.10.3 Checksum data frame
Figure 3-28 shows the format of a frame that includes checksum data.

Figure 3-28. Checksum Data Frame (from 78K0R/Kx3-L to Programmer)

<table>
<thead>
<tr>
<th>STX</th>
<th>LEN</th>
<th>Data</th>
<th>SUM</th>
<th>ETX</th>
</tr>
</thead>
<tbody>
<tr>
<td>02H</td>
<td>02H</td>
<td>CK1</td>
<td>CK2</td>
<td>Checksum</td>
</tr>
</tbody>
</table>

Remark
CK1: Higher 8 bits of checksum data
CK2: Lower 8 bits of checksum data

See 4.13 Checksum Command for details on the flowchart of the processing sequence between the programmer and the 78K0R/Kx3-L, the flowchart of command processing, and the sample program.
3.11 Security Set Command

3.11.1 Description

This command is used to perform security settings (enabling/disabling of write, block erase, chip erase, and boot block rewriting, and setting of flash shield window start/end block number). By performing these settings with this command, rewriting of the flash memory by an unauthorized party can be restricted and the rewrite area for self programming can be specified.

Caution  Even after the security setting, additional setting of changing from enable to disable can be performed; however, changing from disable to enable is not possible. If an attempt is made to perform such a setting, a protect error (10H) will occur. If such setting is required, all of the security flags must first be initialized by executing the Chip Erase command (the Block Erase command cannot be used to initialize the security flags).

If chip erase or boot block rewrite has been disabled, however, chip erase itself will be impossible, so the settings cannot be erased from the programmer. Re-confirmation of security setting execution is therefore recommended before disabling chip erase, due to this programmer specification.

3.11.2 Command frame and status frame

Figure 3-29 shows the format of a command frame for the Security Set command, and Figure 3-30 shows the status frame for the command.

**Figure 3-29. Security Set Command Frame (from Programmer to 78K0R/Kx3-L)**

<table>
<thead>
<tr>
<th>SOH</th>
<th>LEN</th>
<th>COM</th>
<th>Command Information</th>
<th>SUM</th>
<th>ETX</th>
</tr>
</thead>
<tbody>
<tr>
<td>01H</td>
<td>03H</td>
<td>A0H (Security Set)</td>
<td>00H (fixed)</td>
<td>00H (fixed)</td>
<td>Checksum</td>
</tr>
</tbody>
</table>

**Figure 3-30. Status Frame for Security Set Command (from 78K0R/Kx3-L to Programmer)**

<table>
<thead>
<tr>
<th>STX</th>
<th>LEN</th>
<th>Data</th>
<th>SUM</th>
<th>ETX</th>
</tr>
</thead>
<tbody>
<tr>
<td>02H</td>
<td>01H</td>
<td>ST1 (a)</td>
<td>Checksum</td>
<td>03H</td>
</tr>
</tbody>
</table>

**Remark**  ST1 (a): Command reception result
3.11.3 Data frame and status frame

Figure 3-31 shows the format of a security data frame, and Figure 3-32 shows the status frame for the data.

**Figure 3-31. Security Data Frame (from Programmer to 78K0R/Kx3-L)**

<table>
<thead>
<tr>
<th>STX</th>
<th>LEN</th>
<th>Data</th>
<th>SUM</th>
<th>ETX</th>
</tr>
</thead>
<tbody>
<tr>
<td>02H</td>
<td>06H</td>
<td>FLG</td>
<td>BOT</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>FSWSH</td>
<td>FSWSL</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>FSWEH</td>
<td>FSWEL</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>FFH (fixed)</td>
<td>FFH (fixed)</td>
<td>Checksum</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>03H</td>
</tr>
</tbody>
</table>

**Remarks**
1. FLG: Security flag
2. BOT: Boot cluster last block number (fixed to 03H)
3. FSWSH: Higher 8 bits of flash shield window start block number
4. FSWSL: Lower 8 bits of flash shield window start block number
5. FSWEH: Higher 8 bits of flash shield window end block number
6. FSWEL: Lower 8 bits of flash shield window end block number
7. If the flash shield window is not to be set, set FSWS to 0000H and the end block to the target device end block number.

**Figure 3-32. Status Frame for Security Data Writing (from 78K0R/Kx3-L to Programmer)**

<table>
<thead>
<tr>
<th>STX</th>
<th>LEN</th>
<th>Data</th>
<th>SUM</th>
<th>ETX</th>
</tr>
</thead>
<tbody>
<tr>
<td>02H</td>
<td>01H</td>
<td>ST1 (b)</td>
<td>Checksum</td>
<td>03H</td>
</tr>
</tbody>
</table>

**Remark** ST1 (b): Security data write result

3.11.4 Internal verify check and status frame

Figure 3-33 shows the status frame for internal verify check.

**Figure 3-33. Status Frame for Internal Verify Check (from 78K0R/Kx3-L to Programmer)**

<table>
<thead>
<tr>
<th>STX</th>
<th>LEN</th>
<th>Data</th>
<th>SUM</th>
<th>ETX</th>
</tr>
</thead>
<tbody>
<tr>
<td>02H</td>
<td>01H</td>
<td>ST1 (c)</td>
<td>Checksum</td>
<td>03H</td>
</tr>
</tbody>
</table>

**Remark** ST1 (c): Internal verify result

The following table shows the contents in the security flag field.

**Table 3-6. Contents of Security Flag Field**

<table>
<thead>
<tr>
<th>Item</th>
<th>Contents</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bit 7</td>
<td>Fixed to “1”</td>
</tr>
<tr>
<td>Bit 6</td>
<td></td>
</tr>
<tr>
<td>Bit 5</td>
<td></td>
</tr>
<tr>
<td>Bit 4</td>
<td>Boot block rewrite disable flag (1: Enables boot block rewrite, 0: Disable boot block rewrite)</td>
</tr>
<tr>
<td>Bit 3</td>
<td>Fixed to “1”</td>
</tr>
<tr>
<td>Bit 2</td>
<td>Programming disable flag (1: Enables programming, 0: Disable programming)</td>
</tr>
<tr>
<td>Bit 1</td>
<td>Block erase disable flag (1: Enables block erase, 0: Disable block erase)</td>
</tr>
<tr>
<td>Bit 0</td>
<td>Chip erase disable flag (1: Enables chip erase, 0: Disable chip erase)</td>
</tr>
</tbody>
</table>
The following table shows the relationship between the security flag field settings and the enable/disable status of each operation.

Table 3-7. Security Flag Field and Enable/Disable Status of Each Operation

<table>
<thead>
<tr>
<th>Operating Mode</th>
<th>Flash Memory Programming Mode</th>
<th>Self-Programming Mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>Security Setting Item</td>
<td>Command Operation After Security Setting</td>
<td>• All commands can be executed regardless of the security setting values</td>
</tr>
<tr>
<td></td>
<td>√: Execution possible, ×: Execution impossible</td>
<td>• Only retention of security setting values is possible</td>
</tr>
<tr>
<td></td>
<td>△: Writing and block erase in boot area are impossible</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Programming</td>
<td>Chip Erase</td>
</tr>
<tr>
<td>Disable programming</td>
<td>×</td>
<td>√</td>
</tr>
<tr>
<td>Disable chip erase</td>
<td>√</td>
<td>×</td>
</tr>
<tr>
<td>Disable block erase</td>
<td>√</td>
<td>√</td>
</tr>
<tr>
<td>Boot block rewrite disable flag</td>
<td>△</td>
<td>×</td>
</tr>
</tbody>
</table>

Same condition as that in flash memory programming mode (on-board/off-board programming)

See 4.14 Security Set Command for details on the flowchart of the processing sequence between the programmer and the 78K0R/Kx3-L, the flowchart of command processing, and the sample program.
CHAPTER 4 UART COMMUNICATION MODE

4.1 Command Frame Transmission Processing Flowchart

[Flowchart diagram shown with steps:
- Command frame transmission processing
- Command frame header (SOH = 01H) transmission
- Wait between data transmissions
- Data length (LEN) transmission
- Wait between data transmissions
- Command number (COM) transmission
- (LEN - 1) bytes transmitted?
  - Yes: Transmits 1-byte command information
  - No: Wait between data transmissions
- Transmits 1-byte command information
- Wait between data transmissions
- Checksum data (SUM) transmission
- Wait between data transmissions
- Command frame footer (ETX = 03H) transmission
- End of command frame transmission]
4.2 Data Frame Transmission Processing Flowchart

- Data frame transmission processing
- Data frame header (STX = 02H) transmission
- Wait between data transmissions
- Data length (LEN) transmission
- LEN bytes transmitted?
  - Yes: Data frame transmission processing
  - No: Wait between data transmissions
- Transmits 1-byte data
- Wait between data transmissions
- Checksum data (SUM) transmission
- Wait between data transmissions
- Last data frame?
  - Yes: Transmission of last data frame footer (ETX = 03H)
  - No: Transmission of footer other than those of last data frame (ETB = 17H)
- End of data frame transmission
4.3 Data Frame Reception Processing Flowchart

Data frame reception processing

Yes
Data frame header (STX = 02H) received?
No
Timed out?
No
Yes
Data frame header (STX = 02H) received?
No
Timed out?
Yes
Reception time-out error

Yes
Data length (LEN) received?
No
Timed out?
No
Yes
Reception time-out error

Yes
1-byte data received?
No
Timed out?
No
Yes
Reception time-out error

No
LEN byte received?
Yes

Yes
Checksum data (SUM) received?
No
Timed out?
No
Yes
Reception time-out error

Yes
Data frame footer received?
No
Timed out?
No
Yes
Last data frame footer (ETX = 03H) or footer other than those of last data frame (ETB = 17H) or No

Yes
Checksum error?
No
Yes
End of data frame reception

Yes
Checksum error?
4.4 Reset Command

4.4.1 Processing sequence chart

Reset command processing sequence

Note: Do not exceed the retry count for the reset command transmission (up to 16 times).
4.4.2 Description of processing sequence

- <1> Waits from the previous frame reception until the next command processing starts (wait time \( t_{com} \)).
- <2> The low level is output (data 00H is transmitted at 9,600 bps).
- <3> Wait state (wait time \( t_{12} \)).
- <4> The low level is output (data 00H is transmitted at 9,600 bps).
- <5> Wait state (wait time \( t_{2c} \)).
- <6> The Reset command is transmitted by command frame transmission processing.
- <7> A time-out check is performed from command transmission until status frame reception.
  - If a time-out occurs, a time-out error [C] is returned (time-out time \( t_{WT0} \)).
- <8> The status code is checked.

  When ST1 = ACK: Normal completion [A]
  When ST1 \( \neq \) ACK: The retry count \( (t_{RS}) \) is checked.
  - The sequence is re-executed from <5> if the retry count is not over.
  - If the retry count is over, the processing ends abnormally [B].

4.4.3 Status at processing completion

<table>
<thead>
<tr>
<th>Status at Processing Completion</th>
<th>Status Code</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Normal completion [A]</td>
<td>Normal acknowledgment (ACK)</td>
<td>06H The command was executed normally and synchronization between the programmer and the 78K0R/Kx3-L has been established.</td>
</tr>
<tr>
<td>Abnormal termination [B]</td>
<td>Checksum error</td>
<td>07H The checksum of the transmitted command frame does not match.</td>
</tr>
<tr>
<td></td>
<td>Negative acknowledgment (NACK)</td>
<td>15H Command frame data is abnormal (such as invalid data length (LEN) or no ETX).</td>
</tr>
<tr>
<td>Time-out error [C]</td>
<td>–</td>
<td>The status frame was not received within the specified time.</td>
</tr>
</tbody>
</table>
4.4.4 Flowchart

- Reset command processing
- Wait from previous frame reception until next command transmission
- Transmits 00 at 9,600 bps
- Wait
- Transmits 00 at 9,600 bps
- Wait
- Command frame transmission processing (Reset)
- Status frame received?
  - No
  - Timed out?
    - No
    - Status = ACK?
      - No
      - Retry count over?
        - No
        - Abnormal termination [B]
        - Yes
        - Normal completion [A]
      - Yes
        - Normal completion [A]
    - Yes
      - Time-out error [C]
- Yes
  - Yes
    - Normal completion [A]
4.4.5 Sample program
The following shows a sample program for Reset command processing.

```c
/* ***************************** ......................................................*/ 
/* */ 
/* Reset command */ 
/* */ 
/* ***************************** ......................................................*/ 
/* [r] u16 ... error code */ 
/* ***************************** ......................................................*/ 
u16 fl_ua_reset(void)
{
    u16 rc;
    u32 retry;

    set_uart0_br(BR_9600); // change to 9600bps
    fl_wait(tCOM); // wait
    set_ua_dir_tx(); // Change Mono-wire UART transmit mode
   putc_ua(0x00); // send 0x00 @ 9600bps
    fl_wait(t12); // wait
    putc_ua(0x00); // send 0x00 @ 9600bps
    set_ua_dir_rx(); // Change Mono-wire UART receive mode

    for (retry = 0; retry < tRS; retry++){
        fl_wait(t2C); // wait
        put_cmd_ua(FL_COM_RESET, 1, fl_cmd_prm); // send RESET command
        rc = get_sfrm_ua(fl ua_sfrm, tWT0_MAX);
        if (rc == FLC_DFTO_ERR) // t.o. ?
            break; // yes // case [C]
        if (rc == FLC_ACK){ // ACK ?
            break; // yes // case [A]
        }else{
            NOP();
        }
        //continue; // case [B] (if exit from loop)
    }
    // switch(rc) {
    // // case FLC_NO_ERR: return rc; break; // case [A]
    // case FLC_DFTO_ERR: return rc; break; // case [C]
    // default: return rc; break; // case [B]
    // }
    return rc;
}
```
4.5 Baud Rate Set Command

4.5.1 Processing sequence chart

Baud Rate Set command processing sequence

**Note** Do not exceed the retry count for the reset command transmission (up to 16 times).
4.5.2 Description of processing sequence

<1> Waits from the previous frame reception until the next command transmission (wait time $t_{\text{com}}$).
<2> The Baud Rate Set command is transmitted by command frame transmission processing.
<3> Waits from command transmission until Reset command transmission (wait time $t_{\text{WT10}}$).
<4> The baud rate of UART communication is switched to the value set by the Baud Rate Set command.
<5> The Reset command is transmitted by command frame transmission processing.
<6> A time-out check is performed from command transmission until status frame reception.
   If a time-out occurs, a time-out error [C] is returned (time-out time $t_{\text{WT0}}$).
<7> Since the status code should be ACK, the processing ends normally [A].

4.5.3 Status at processing completion

<table>
<thead>
<tr>
<th>Status at Processing Completion</th>
<th>Status Code</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Normal completion [A]</td>
<td>Normal acknowledgment (ACK)</td>
<td>06H</td>
</tr>
<tr>
<td>Abnormal termination [B]</td>
<td>Checksum error</td>
<td>07H</td>
</tr>
<tr>
<td></td>
<td>Negative acknowledgment (NACK)</td>
<td>15H</td>
</tr>
<tr>
<td>Time-out error [C]$^{\text{new}}$</td>
<td>–</td>
<td>Data frame reception was timed out. With the 78K0R/Kx3-L, this command also results in errors in the following cases. • Command information (D01, D02H, D02L, D03) is invalid • The command frame includes the checksum error • The data length of the command frame (LEN) is invalid • The footer of the command frame (ETX) is missing • The Reset command was not detected after setting the baud rate and receiving command frame data for 16 times.</td>
</tr>
</tbody>
</table>

Note If a time-out error has occurred, execute a hardware reset and re-set to the flash memory programming mode.
4.5.4 Flowchart

- Baud Rate Set command processing
  - Wait from previous frame reception until next command transmission
    - Command frame transmission processing (Baud Rate Set)
      - Wait from command frame transmission until Reset command transmission
        - Command frame transmission processing (Reset)
          - Status frame received? (No: Normal completion [A], Yes: Timed out?)
            - Timed out? (No: Normal completion [A], Yes: Time-out error [C])
4.5.5 Sample program

The following shows a sample program for Baud Rate Set command processing.

```c
/* ***********************************************/
/* */
/* Set baudrate command */
/* */
/* ***********************************************/
/* [i]  u8 brid  ... baudrate ID */
/* [i]  u8 fpv   ... Flash programming voltage */
/* [r]  u16 ... error code */
/* ***********************************************/

u16 fl_ua_setbaud(u8 brid, u8 fpv)
{
    u16 rc;
    u8 br;
    u32 retry;

    fl_cmd_prm[0] = 0x00; // "D01"  : adjust by target device (115200bps)
    fl_cmd_prm[1] = 0x00; // "D02H" : adjust by target device (115200bps)
    fl_cmd_prm[2] = 0x0a; // "D02L" : (fixed value)
    fl_cmd_prm[3] = 0x01; // "D03"  : noise filter on
    fl_cmd_prm[4] = fpv; // "D04"  : Flash programming voltage

    fl_wait(tCOM);  // wait before sending command
    put_cmd_ua(FL_COM_SET_BAUDRATE, 1+5, fl_cmd_prm); // send "Baudrate Set" command
    retry = tRS;
    while(1){
        fl_wait(tWT10);

        put_cmd_ua(FL_COM_RESET, 1, fl_cmd_prm); // send RESET command
        rc = get_sfrm_ua(fl_ua_sfrm, tWT0_MAX);  // get status frame
        if (rc){
            if (retry--)
                continue;
            else
                return rc;
        }
        break;  // got ACK !!!!
    }

    // switch(rc) {
    //     case FLC_NO_ERR: return rc; break; // case [A]
    //     case FLC_DFTO_ERR: return rc; break; // case [C]
    //     default:        return rc; break; // case [B]
    // }

    return rc;
}
```

Application Note  U19486EJ1V0AN
4.6 Chip Erase Command

4.6.1 Processing sequence chart

Chip Erase command processing sequence
4.6.2 Description of processing sequence

<1> Waits from the previous frame reception until the next command transmission (wait time tCOM).
<2> The Chip Erase command is transmitted by command frame transmission processing.
<3> A time-out check is performed from command transmission until status frame reception. If a time-out occurs, a time-out error [C] is returned (time-out time tWT1).
<4> The status code is checked.

When ST1 = ACK: Normal completion [A]
When ST1 ≠ ACK: Abnormal termination [B]

4.6.3 Status at processing completion

<table>
<thead>
<tr>
<th>Status at Processing Completion</th>
<th>Status Code</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Normal completion [A]</td>
<td>Normal acknowledgment (ACK)</td>
<td>06H</td>
</tr>
<tr>
<td>Abnormal termination [B]</td>
<td>Checksum error</td>
<td>07H</td>
</tr>
<tr>
<td></td>
<td>Protect error</td>
<td>10H</td>
</tr>
<tr>
<td></td>
<td>Negative acknowledgment (NACK)</td>
<td>15H</td>
</tr>
<tr>
<td></td>
<td>MRG10 error</td>
<td>1AH</td>
</tr>
<tr>
<td></td>
<td>MRG11 error</td>
<td>1BH</td>
</tr>
<tr>
<td></td>
<td>Write error</td>
<td>1CH</td>
</tr>
<tr>
<td>Time-out error [C]</td>
<td>–</td>
<td>The status frame was not received within the specified time.</td>
</tr>
</tbody>
</table>
4.6.4 Flowchart

1. Chip Erase command processing

2. Waits from previous frame reception until next command transmission

3. Command frame transmission processing (Chip Erase)

4. Status frame received?
   - Yes: Status = ACK?
     - Yes: Normal completion [A]
     - No: Abnormal termination [B]
   - No: Timed out?
     - Yes: Time-out error [C]
     - No: tWT1

5. tCOM
4.6.5 Sample program

The following shows a sample program for Chip Erase command processing.

```c
/******************************************************************
/*               */
/* Erase all(chip) command                                      */
/*               */
/******************************************************************
/* [r] u16        ... error code                                 */
/******************************************************************
u16    fl_ua_erase_all(void)
{
    u16 rc;

    fl_wait(tCOM); // wait before sending command
    put_cmd_ua(FL_COM_ERASE_CHIP, 1, fl_cmd_prm); // send ERASE CHIP command
    rc = get_sfrm_ua(fl_ua_sfrm, tWT1_MAX); // get status frame
    // switch(rc) {
    //     case FLC_NO_ERR: return rc; break; // case [A]
    //     case FLC_DFTO_ERR: return rc; break; // case [C]
    //     default: return rc; break; // case [B]
    // }
    return rc;
}
```
4.7 Block Erase Command

4.7.1 Processing sequence chart

Block Erase command processing sequence

1. Wait from previous frame reception until next command transmission
2. Block Erase command frame transmission
3. Time-out check for status frame reception
4. Status frame reception

Status frame received within specified time

Normal completion [A]

Other than ACK

Abnormal termination [B]

Time-out error [C]

ACK

Reception status [ACK/other than ACK]

Programmer 78K0R/Kx3-L
4.7.2 Description of processing sequence

<1> Waits from the previous frame reception until the next command transmission (wait time $t_{COM}$).

<2> The Block Erase command is transmitted by command frame transmission processing.

<3> A time-out check is performed from command transmission until status frame reception.
   If a time-out occurs, a time-out error [C] is returned (time-out time $t_{WT2}$).

<4> The status code is checked.

When ST1 = ACK: Normal completion [A]
When ST1 $\neq$ ACK: Abnormal termination [B]

4.7.3 Status at processing completion

<table>
<thead>
<tr>
<th>Status at Processing Completion</th>
<th>Status Code</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Normal completion [A]</td>
<td>06H</td>
<td>The command was executed normally and block erase was performed normally.</td>
</tr>
<tr>
<td>Parameter error</td>
<td>05H</td>
<td>The specified end address is out of the flash memory range, or the specified start/end address is not the first/end address of the block.</td>
</tr>
<tr>
<td>Checksum error</td>
<td>07H</td>
<td>The checksum of the transmitted command frame does not match.</td>
</tr>
<tr>
<td>Protect error</td>
<td>10H</td>
<td>Write, block erase, or chip erase is prohibited in the security setting. A boot block is included in the specified range and boot block rewrite is prohibited.</td>
</tr>
<tr>
<td>Negative acknowledgment (NACK)</td>
<td>15H</td>
<td>Command frame data is abnormal (such as invalid data length (LEN) or no ETX).</td>
</tr>
<tr>
<td>MRG10 error</td>
<td>1AH</td>
<td>An erase error has occurred.</td>
</tr>
<tr>
<td>Time-out error [C]</td>
<td>–</td>
<td>The status frame was not received within the specified time.</td>
</tr>
</tbody>
</table>
4.7.4 Flowchart

Block Erase command processing

Wait from previous frame reception until next command transmission

Command frame transmission processing (Block Erase)

Status frame received?

Yes

Status = ACK?

Yes

Normal completion [A]

No

Abnormal termination [B]

No

Timed out?

Yes

Time-out error [C]

No

No

Timed out? tWT2

No
4.7.5 Sample program

The following shows a sample program for Block Erase command processing.

```c
/* ******************************************************/
/* */
/* Erase block command */
/* */
/* ******************************************************/
/* [i] u8 block          ... block number */
/* [r] u16    ... error code */
/* ******************************************************/

u16 f1_ua_erase_blk(u16 sblk, u16 eblk) {
    u16 rc;
    u32 wt2_max;
    u32 top, bottom;

    top = get_top_addr(sblk);       // get start address of start block
    bottom = get_bottom_addr(eblk);  // get end address of end block

    set_range_prm(fl_cmd_prm, top, bottom); // set SAH/SAM/SAL, EAH/EAM/EAL

    wt2_max = make_wt2_max(sblk, eblk);

    fl_wait(tCOM);                  // wait before sending command

    put_cmd_ua(FL_COM_ERASE_BLOCK, 1+6, fl_cmd_prm); // send ERASE CHIP command

    rc = get_sfrm_ua(f1_ua_sfrm, wt2_max); // get status frame

    switch(rc) {
        //
        //    case FLC_NO_ERR: return rc; break; // case [A]
        //    case FLC_DFTO_ERR: return rc; break; // case [C]
        //    default: return rc; break; // case [B]
        // }

    return rc;
}
```
4.8 Programming Command

4.8.1 Processing sequence chart

Programming command processing sequence:
4.8.2 Description of processing sequence

<1> Waits from the previous frame reception until the next command transmission (wait time \( t_{COM} \)).

<2> The Programming command is transmitted by command frame transmission processing.

<3> A time-out check is performed from command transmission until status frame reception.
   If a time-out occurs, a time-out error [C] is returned (time-out time \( t_{WT3} \)).

<4> The status code is checked.

   When \( ST1 = ACK \): Proceeds to <5>.
   When \( ST1 \neq ACK \): Abnormal termination [B]

<5> Waits from the previous frame reception until the next data frame transmission (wait time \( t_{FD3} \)).

<6> User data is transmitted by data frame transmission processing.

<7> A time-out check is performed from user data transmission until data frame reception.
   If a time-out occurs, a time-out error [C] is returned (time-out time \( t_{WT4} \)).

<8> The status code (\( ST1/ST2 \)) is checked (also refer to the processing sequence chart and flowchart).

   When \( ST1 \neq ACK \): Abnormal termination [B]
   When \( ST1 = ACK \): The following processing is performed according to the \( ST2 \) value.
   - When \( ST2 = ACK \): Proceeds to <9> when transmission of all data frames is completed.
     If there still remain data frames to be transmitted, the processing re-executes the sequence from <5>.
   - When \( ST2 \neq ACK \): Abnormal termination [D]

<9> A time-out check is performed until status frame reception.
   If a time-out occurs, a time-out error [C] is returned (time-out time \( t_{WT5} \times \) number of blocks).

<10> The status code is checked.

   When \( ST1 = ACK \): Normal completion [A]
   When \( ST1 \neq ACK \): Abnormal termination [E]
### Status at processing completion

<table>
<thead>
<tr>
<th>Status at Processing Completion</th>
<th>Status Code</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Normal completion [A]</td>
<td>Normal acknowledgment (ACK)</td>
<td>06H</td>
</tr>
<tr>
<td>Abnormal termination [B]</td>
<td>Parameter error</td>
<td>05H</td>
</tr>
<tr>
<td></td>
<td>Checksum error</td>
<td>07H</td>
</tr>
<tr>
<td></td>
<td>Protect error</td>
<td>10H</td>
</tr>
<tr>
<td></td>
<td>Negative acknowledgment (NACK)</td>
<td>15H</td>
</tr>
<tr>
<td>Abnormal termination [D], [E]</td>
<td>MRG10 error</td>
<td>1AH</td>
</tr>
<tr>
<td></td>
<td>MRG11 error</td>
<td>1BH</td>
</tr>
<tr>
<td></td>
<td>Write error</td>
<td>1CH</td>
</tr>
</tbody>
</table>
4.8.4 Flowchart

Programming command processing

Wait from previous frame reception until next command transmission
tWait

Command frame transmission processing (Programming)

Status frame received?
Yes

Status = ACK?
No

Timed out?
yes

Time-out error [C]

Status = ACK?
No

Abnormal termination [B]

Status frame received?
Yes

Data frame transmission processing (User program)

Status frame received?
Yes

ST1 = ACK?
No

Timed out?
yes

Time-out error [C]

ST2 = ACK?
Yes

Abnormal termination [B]

All data frames transmitted?
No

Normal completion [A]

Status = ACK?
Yes

Abnormal termination [E]

Status frame received?
Yes

Status = ACK?
Yes

Abnormal termination [C]

Timed out?
yes

Time-out error [C]

Status frame received?
Yes

Status = ACK?
Yes

Abnormal termination [C]

Timed out?
yes

Time-out error [C]

× number of blocks
4.8.5 Sample program

The following shows a sample program for Programming command processing.

```c
#define fl_st2_ua (fl_ua_sfrm[OFS_STA_PLD+1])

u16 fl_ua_write(u32 top, u32 bottom)
{
    u16 rc;
    u32 send_head, send_size;
    bool is_end;
    u16 block_num;

    block_num = get_block_num(top, bottom); // get block num

    set_range_prm(fl_cmd_prm, top, bottom); // set SAH/SAM/SAL, EAH/EAM/EAL

    fl_wait(tCOM); // wait before sending command
    put_cmd_ua(FL_COM_WRITE, 7, fl_cmd_prm); // send "Programming" command
    rc = get_sfrm_ua(fl_ua_sfrm, tWT3_MAX); // get status frame
    switch(rc) {
        case FLC_NO_ERR: break; // continue
        // case FLC_DFTO_ERR: return rc; break; // case [C]
        default: FLC_DFTO_ERR: return rc; break; // case [B]
    }

    send_head = top;
    while(1){
        // make send data frame
        if ((bottom - send_head) > 256){ // rest size > 256 ?
            is_end = false; // yes, not is_end frame
```
send_size = 256; // transmit size = 256 byte

} else{
    is_end = true;
    send_size = bottom - send_head + 1; // transmit size = (bottom - send_head)+1 byte
}

memcpy(fl_txdata_frm, rom_buf+send_head, send_size); // set data frame

send_head += send_size;

fl_wait(tFD3); // wait before sending data

put_dfrm_ua(send_size, fl_txdata_frm, is_end); // send user data

rc = get_sfrm_ua(f1 ua_sfrm, tWT4_MAX); // get status frame

switch(rc) {
  case FLC_NO_ERR: break; // continue
  case FLC_DFTO_ERR: return rc; break; // case [C]
  default: return rc; break; // case [B]
}

if (f1_st2_ua != FLST_ACK){ // ST2 = ACK ?
  rc = decode_status(f1_st2_ua); // No
  return rc; // case [D]
}

if (is_end)
  break;

/*********************************************************/
/* Check internally verify */
/*********************************************************/

// get status frame again
if (top == 0){ /* include Block0 */
  rc = get_sfrm_ua(f1 ua_sfrm, tWT5_B0_MAX + tWT5_MAX*(block_num-1));
}
else{
  rc = get_sfrm_ua(f1 ua_sfrm, tWT5_MAX*block_num);
}

switch(rc) {
  case FLC_NO_ERR: return rc; break; // case [A]
  case FLC_DFTO_ERR: return rc; break; // case [C]
  default: return rc; break; // case [E]
}

return rc;
4.9 Verify Command

4.9.1 Processing sequence chart

Verify command processing sequence
4.9.2 Description of processing sequence

<1> Waits from the previous frame reception until the next command transmission (wait time \( t_{com} \)).

<2> The Verify command is transmitted by command frame transmission processing.

<3> A time-out check is performed from command transmission until status frame reception.
   If a time-out occurs, a time-out error [C] is returned (time-out time \( t_{WT6} \)).

<4> The status code is checked.
   - When ST1 = ACK: Proceeds to <5>.
   - When ST1 ≠ ACK: Abnormal termination [B]

<5> Waits from the previous frame reception until the next data frame transmission (wait time \( t_{FD3} \)).

<6> User data for verifying is transmitted by data frame transmission processing.

<7> A time-out check is performed from user data transmission until status frame reception.
   If a time-out occurs, a time-out error [C] is returned (time-out time \( t_{WT7} \)).

<8> The status code (ST1/ST2) is checked (also refer to the processing sequence chart and flowchart).
   - When ST1 ≠ ACK: Abnormal termination [B]
   - When ST1 = ACK: The following processing is performed according to the ST2 value.
     - When ST2 = ACK: If transmission of all data frames is completed, the processing ends normally [A].
       If there still remain data frames to be transmitted, the processing re-executes the sequence from <5>.
     - When ST2 ≠ ACK: Abnormal termination [D]

4.9.3 Status at processing completion

<table>
<thead>
<tr>
<th>Status at Processing Completion</th>
<th>Status Code</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Normal completion [A]</td>
<td>Normal acknowledgment (ACK)</td>
<td>06H</td>
</tr>
<tr>
<td>Abnormal termination [B]</td>
<td>Parameter error</td>
<td>05H</td>
</tr>
<tr>
<td></td>
<td>Checksum error</td>
<td>07H</td>
</tr>
<tr>
<td></td>
<td>Negative acknowledgment (NACK)</td>
<td>15H</td>
</tr>
<tr>
<td>Time-out error [C]</td>
<td>–</td>
<td>The status frame was not received within the specified time.</td>
</tr>
<tr>
<td>Abnormal termination [D]</td>
<td>Verify error</td>
<td>0FH (ST2)</td>
</tr>
</tbody>
</table>
4.9.4 Flowchart

Verify command processing

Wait from previous frame reception until next command transmission

Command frame transmission processing (Verify)

Status frame received?

Yes

ST1 = ACK?

No

Timed out?

No

Yes

Time-out error [C]

No

ST1 = ACK?

Yes

Abnormal termination [B]

Wait from previous frame reception until next data frame transmission

Data frame transmission processing (User program)

Status frame received?

Yes

Timed out?

No

Yes

Time-out error [C]

No

ST1 = ACK?

Yes

Abnormal termination [B]

ST2 = ACK?

No

Abnormal termination [D]

Yes

All data frames transmitted?

No

Normal completion [A]

Yes
4.9.5 Sample program

The following shows a sample program for Verify command processing.

```c
u16 fl_ua_verify(u32 top, u32 bottom, u8 *buf)
{
    u16 rc;
    u32 send_head, send_size;
    bool is_end;

    set_range_prm(fl_cmd_prm, top, bottom); // set SAH/SAM/SAL, EAH/EAM/EAL

    fl_wait(tCOM); // wait before sending command
    put_cmd_ua(FL_COM_VERIFY, 7, fl_cmd_prm); // send VERIFY command
    rc = get_sfrm_ua(fl_ua_sfrm, tWT6_MAX); // get status frame
    switch(rc) {
        case FLC_NO_ERR:    break; // continue
        // case FLC_DFTO_ERR: return rc;  break; // case [C]
        default:  return rc;  break; // case [B]
    }

    send_head = top;
    while(1){
        // make send data frame
        if ((bottom - send_head) > 256){ // rest size > 256 ?
            is_end = false; // yes, not is_end frame
            send_size = 256; // transmit size = 256 byte
        } else{
            is_end = true;
            send_size = bottom - send_head + 1; // transmit size = (bottom - send_head)+1 byte
        }
        
        // send user data
        while(send_size > 0){
            if (is_end) {
                put_data_ua(buf, send_size / 256);
            } else{
                put_data_ua(buf, send_size % 256);
            }
            send_size -= 256;
        }
    }
}
```
memcpy(fl_txdata_frm, buf+send_head, send_size); // set data frame payload
send_head += send_size;

fl_wait(tFD3);
put_dfrm ua(send_size, fl_txdata_frm, is_end); // send user data

rc = get_sfrm ua(fl_ua_sfrm, tWT7_MAX);  // get status frame
switch(rc) {
  case FLC_NO_ERR:    break; // continue
  // case FLC_DFTO_ERR: return rc;  break; // case [C]
  default:  return rc;  break; // case [B]
}
if (fl_st2_ua != FLST_ACK){  // ST2 = ACK ?
  rc = decode_status(fl_st2_ua); // No
  return rc;    // case [D]
}
if (is_end)      // send all user data ?
  break;      // yes
// continue;

return FLC_NO_ERR; // case [A]
4.10 Block Blank Check Command

4.10.1 Processing sequence chart

Block Blank Check command processing sequence

1. Wait from previous frame reception until next command transmission
2. Block Blank Check command frame transmission
3. Time-out check for status frame reception
   - Status frame received within specified time
   - Time-out error [C]
4. Status frame reception
   - Normal completion [A]
   - Abnormal termination [B]
   - Other than ACK

Programmer

78K0R/Kx3-L

*Diagram shows the flow of commands and responses between the programmer and the 78K0R/Kx3-L device.*
4.10.2 Description of processing sequence

<1> Waits from the previous frame reception until the next command transmission (wait time \( t_{\text{com}} \)).

<2> The Block Blank Check command is transmitted by command frame transmission processing.

<3> A time-out check is performed from command transmission until status frame reception.
   If a time-out occurs, a time-out error [C] is returned (time-out time \( t_{\text{WT8}} \times \) number of blocks).

<4> The status code is checked.

   When ST1 = ACK: Normal completion [A]
   When ST1 ≠ ACK: Abnormal termination [B]

4.10.3 Status at processing completion

<table>
<thead>
<tr>
<th>Status at Processing Completion</th>
<th>Status Code</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Normal completion [A]</td>
<td>Normal acknowledgment (ACK)</td>
<td>06H The command was executed normally and block blank check was executed normally.</td>
</tr>
<tr>
<td>Abnormal termination [B]</td>
<td>Parameter error</td>
<td>05H The end address is out of the flash memory range, the start/end address is not the first/end address of the block, or the value of parameter D01 is other than 00H or 01H.</td>
</tr>
<tr>
<td></td>
<td>Checksum error</td>
<td>07H The checksum of the transmitted command frame does not match.</td>
</tr>
<tr>
<td></td>
<td>Negative acknowledgment (NACK)</td>
<td>15H Command frame data is abnormal (such as invalid data length (LEN) or no ETX).</td>
</tr>
<tr>
<td></td>
<td>MRG11 error</td>
<td>1BH The flash memory of the specified block is not blank.</td>
</tr>
<tr>
<td>Time-out error [C]</td>
<td>–</td>
<td>1BH The status frame was not received within the specified time.</td>
</tr>
</tbody>
</table>
4.10.4 Flowchart

```
Block Blank Check command processing

Wait from previous frame reception until next command transmission

Command frame transmission processing (Block Blank Check)

Status frame received?

Yes

Timed out?

No

Status = ACK?

No

Yes

Normal completion [A]

Timed out?

Yes

Time-out error [C]

No

Status frame received?

Yes

Status = ACK?

No

Yes

Abnormal termination [B]

Timed out?

Yes

Time-out error [C]

No

Normal completion [A]
```

\[ t_{\text{COM}} \times \text{number of blocks} \]
4.10.5 Sample program
The following shows a sample program for Block Blank Check command processing.

```c
u16 fl_ua_blk_blank_chk(u32 top, u32 bottom, u8 whole)
{
    u16 rc;
    u16 block_num;

    set_range_prm(fl_cmd_prm, top, bottom); // set SAH/SAM/SAL, EAH/EAM/EAL
    block_num = get_block_num(top, bottom); // get block num
    fl_cmd_prm[6] = whole; // check only user area or not

    fl_wait(tCOM); // wait before sending command

    put_cmd_ua(FL_COM_BLOCK_BLANK_CHK, 7+1, fl_cmd_prm);

    rc = get_sfrm_ua(fl_ua_sfrm, tWT8_MAX * block_num); // get status frame
    // switch(rc) {
    //     case FLC_NO_ERR: return rc; break; // case [A]
    //     case FLC_DFTO_ERR: return rc; break; // case [C]
    //     default: return rc; break; // case [B]
    // }
    return rc;
}
```
4.11 Silicon Signature Command

4.11.1 Processing sequence chart

Silicon Signature command processing sequence
4.11.2 Description of processing sequence

<1> Waits from the previous frame reception until the next command transmission (wait time $t_{\text{com}}$).

<2> The Silicon Signature command is transmitted by command frame transmission processing.

<3> A time-out check is performed from command transmission until status frame reception.
   If a time-out occurs, a time-out error [C] is returned (time-out time $t_{\text{WT1}}$).

<4> The status code is checked.
   
   When $ST1 = \text{ACK}$: Proceeds to <5>.
   When $ST1 \neq \text{ACK}$: Abnormal termination [B]

<5> A time-out check is performed until data frame (silicon signature data) reception.
   If a time-out occurs, a time-out error [C] is returned (time-out time $t_{\text{FD2}}$).

<6> The received data frame (silicon signature data) is checked.
   
   If data frame is normal: Normal completion [A]
   If data frame is abnormal: Data frame error [D]

4.11.3 Status at processing completion

<table>
<thead>
<tr>
<th>Status at Processing Completion</th>
<th>Status Code</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Normal completion [A]</td>
<td>Normal acknowledgment (ACK)</td>
<td>06H</td>
</tr>
<tr>
<td>Abnormal termination [B]</td>
<td>Checksum error</td>
<td>07H</td>
</tr>
<tr>
<td></td>
<td>Negative acknowledgment (NACK)</td>
<td>15H</td>
</tr>
<tr>
<td>Time-out error [C]</td>
<td>–</td>
<td>The status frame or data frame was not received within the specified time.</td>
</tr>
<tr>
<td>Data frame error [D]</td>
<td>–</td>
<td>The checksum of the data frame received as silicon signature data does not match.</td>
</tr>
</tbody>
</table>
4.11.4 Flowchart

- Silicon Signature command processing
- Wait from previous frame reception until next command transmission
- Command frame transmission processing (Silicon Signature)
  - Status frame received?
    - Yes
      - Status = ACK?
        - Yes
          - Normal completion [A]
        - No
          - Abnormal termination [B]
    - No
      - Timed out?
        - Yes
          - Time-out error [C]
        - No
          - Data frame (silicon signature) received?
            - Yes
              - Normal data frame?
                - Yes
                  - Normal completion [A]
                - No
                  - Data frame error [D]
            - No
              - Timed out?
                - Yes
                  - Time-out error [C]
                - No
4.11.5 Sample program

The following shows a sample program for Silicon Signature command processing.

```c
u16  fl_ua_getsig(u8 *sig)
{
    u16   rc;

    fl_wait(tCOM); // wait before sending command
    put_cmd_ua(FL_COM_GET_SIGNATURE, 1, fl_cmd_prm); // send GET SIGNATURE command

    rc = get_sfrm_ua(fl_ua_sfrm, tWT11_MAX); // get status frame
    switch(rc) {
        case FLC_NO_ERR:   break; // continue
        // case FLC_DFTO_ERR: return rc; break; // case [C]
        default:   return rc; break; // case [B]
    }

    rc = get_dfrm_ua(fl_rxdata_frm, tFD2_MAX); // get status frame
    if (rc){ // if error
        return rc; // case [D]
    }
    memcpy(sig, fl_rxdata_frm+OFS_STA_PLD, fl_rxdata_frm[OFS_LEN]); // copy Signature data
    return rc; // case [A]
}
```
4.12 Version Get Command

4.12.1 Processing sequence chart

Version Get command processing sequence

Programmer 78K0R/Kx3-L

1. Wait from previous frame reception until next command transmission
2. Version Get command frame transmission
3. Time-out check for status frame reception
4. Status frame reception
5. Time-out check for data frame reception
6. Data frame (version data) reception

Time-out occurs
- Status frame received within specified time
  - Reception status [ACK/other than ACK]
  - Time-out error [C]
  - Abnormal termination [B]

Other than ACK
- Time-out occurs
  - Data frame received within specified time
    - Normal data frame? [Yes/No]
      - Yes
        - Normal completion [A]
      - No
        - Data frame error [D]

Within specified time
- Normal completion [A]
4.12.2 Description of processing sequence

<1> Waits from the previous frame reception until the next command transmission (wait time $t_{com}$).

<2> The Version Get command is transmitted by command frame transmission processing.

<3> A time-out check is performed from command transmission until status frame reception.

   If a time-out occurs, a time-out error [C] is returned (time-out time $t_{WT1}$).

<4> The status code is checked.

   When ST1 = ACK: Proceeds to <5>.
   When ST1 ≠ ACK: Abnormal termination [B]

<5> A time-out check is performed until data frame (version data) reception.

   If a time-out occurs, a time-out error [C] is returned (time-out time $t_{FD2}$).

<6> The received data frame (version data) is checked.

   If data frame is normal: Normal completion [A]
   If data frame is abnormal: Data frame error [D]

4.12.3 Status at processing completion

<table>
<thead>
<tr>
<th>Status at Processing Completion</th>
<th>Status Code</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Normal completion [A]</td>
<td>Normal acknowledgment (ACK)</td>
<td>06H</td>
</tr>
<tr>
<td>Abnormal termination [B]</td>
<td>Checksum error</td>
<td>07H</td>
</tr>
<tr>
<td></td>
<td>Negative acknowledgment (NACK)</td>
<td>15H</td>
</tr>
<tr>
<td>Time-out error [C]</td>
<td>–</td>
<td>The status frame or data frame was not received within the specified time.</td>
</tr>
<tr>
<td>Data frame error [D]</td>
<td>–</td>
<td>The checksum of the data frame received as version data does not match.</td>
</tr>
</tbody>
</table>
4.12.4 Flowchart

- Wait from previous frame reception until next command transmission
- Command frame transmission processing (Version Get)
  - Status frame received?
    - Yes
      - Status = ACK?
        - Yes
          - Normal completion [A]
        - No
          - Abnormal termination [B]
          - Data frame (version data) received?
            - Yes
              - Normal data frame?
                - Yes
                  - Normal completion [A]
                - No
                  - Data frame error [D]
            - No
              - Timed out?
                - Yes
                  - Time-out error [C]
                - No
                  - Abnormal termination [B]
4.12.5 Sample program

The following shows a sample program for Version Get command processing.

```c
/******************************************************************
/*               */
/* Get device/firmware version command                        */
/*               */
/******************************************************************
/* [i] u8 *buf ... pointer to version date save area           */
/* [r] u16 ... error code                                      */
/******************************************************************
u16  fl_ua_getver(u8 *buf)
{
    u16  rc;

    fl_wait(tCOM);  // wait before sending command

    put_cmd_ua(FL_COM_GET_VERSION, 1, fl_cmd_prm); // send GET VERSION command

    rc = get_sfrm_ua(fl_ua_sfrm, tWT12_MAX);  // get status frame
    switch(rc) {
        case  FLC_NO_ERR:   break; // continue
        // case  FLC_DFTO_ERR: return rc; break; // case [C]
        default:   return rc; break; // case [B]
    }

    rc = get_dfrm_ua(fl_rxdata_frm, tFD2_MAX);  // get data frame
    if (rc){
        return rc;  // case [D]
    }

    memcpy(buf, fl_rxdata_frm+OFS_STA_PLD, DFV_LEN); // copy version data
    return rc;  // case [A]
}
```
4.13 Checksum Command

4.13.1 Processing sequence chart

Checksum command processing sequence
4.13.2 Description of processing sequence

<1> Waits from the previous frame reception until the next command transmission (wait time $t_{com}$).

<2> The Checksum command is transmitted by command frame transmission processing.

<3> A time-out check is performed from command transmission until status frame reception. If a time-out occurs, a time-out error [C] is returned (time-out time $t_{WT1}$).

<4> The status code is checked.

- When ST1 = ACK: Proceeds to <5>.
- When ST1 ≠ ACK: Abnormal termination [B]

<5> A time-out check is performed until data frame (checksum data) reception. If a time-out occurs, a time-out error [C] is returned (time-out time $t_{FD1}$).

<6> The received data frame (checksum data) is checked.

- If data frame is normal: Normal completion [A]
- If data frame is abnormal: Data frame error [D]

4.13.3 Status at processing completion

<table>
<thead>
<tr>
<th>Status at Processing Completion</th>
<th>Status Code</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Normal completion [A]</td>
<td>Normal acknowledgment (ACK)</td>
<td>06H</td>
</tr>
<tr>
<td>Abnormal termination [B]</td>
<td>Parameter error</td>
<td>05H</td>
</tr>
<tr>
<td></td>
<td>Checksum error</td>
<td>07H</td>
</tr>
<tr>
<td></td>
<td>Negative acknowledgment (NACK)</td>
<td>15H</td>
</tr>
<tr>
<td>Time-out error [C]</td>
<td>–</td>
<td>–</td>
</tr>
<tr>
<td>Data frame error [D]</td>
<td>–</td>
<td>–</td>
</tr>
</tbody>
</table>
4.13.4 Flowchart

1. Checksum command processing
2. Wait from previous frame reception until next command transmission
3. Command frame transmission processing (Checksum)
4. Status frame received?
   - Yes
     - Status = ACK?
       - Yes
         - Abnormal termination [B]
       - No
         - Data frame (checksum data) received?
           - Yes
             - Normal data frame?
               - Yes
                 - Normal completion [A]
               - No
                 - Data frame error [D]
           - No
             - Timed out?
               - Yes
                 - Time-out error [C]
               - No
4. Timed out?
   - Yes
     - Time-out error [C]
   - No

Abnormal termination [B]
Data frame error [D]
Time-out error [C]
4.13.5 Sample program

The following shows a sample program for Checksum command processing.

```c
u16 fl_ua_getsum(u16 *sum, u32 top, u32 bottom)
{
    u16 rc;

    // set params
    set_range_prm(fl_cmd_prm, top, bottom); // set SAH/SAM/SAL, EAH/EAM/EAL

    // wait before sending command
    fl_wait(tCOM);

    // send command
    put_cmd_ua(FL_COM_GET_CHECK_SUM, 7, fl_cmd_prm); // send GET VERSION command

    rc = get_sfrm_ua(fl_ua_sfrm, tWT16_MAX); // get status frame
    switch(rc) {
        case FLC_NO_ERR:   break; // continue
        case FLC_DFTO_ERR: return rc; break; // case [C]
        default:   return rc; break; // case [B]
    }

    // get data frame (Checksum data)
    rc = get_dfrm_ua(fl_rxdata_frm, tFD1_MAX); // get status frame
    if (rc) {
        return rc; // case [D]
    }

    *sum = (fl_rxdata_frm[OFS_STA_PLD] << 8) + fl_rxdata_frm[OFS_STA_PLD+1]; // set SUM data
    return rc; // case [A]
}
```
4.14 Security Set Command

4.14.1 Processing sequence chart

Security Set command processing sequence

Programmer

78K0R/Kx3-L

<1> Wait from previous frame reception until next command transmission

<2> Security Set command frame transmission

<3> Time-out check for status frame reception

<4> Status frame reception

<5> Wait from previous frame reception until data frame transmission

<6> Data frame (security data) transmission

<7> Time-out check for status frame reception

<8> Status frame reception

Reception status [ACK/other than ACK]

Abnormal termination [B]

Other than ACK

Time-out error [C]

Time-out occurs

Status frame received within specified time

Reception status [ACK/other than ACK]

ACK

Abnormal termination [D]

Other than ACK

Time-out occurs

Status frame received within specified time

Reception status [ACK/other than ACK]

ACK

Abnormal termination [E]

Other than ACK

Time-out error [C]

Normal completion [A]
4.14.2 Description of processing sequence

<1> Waits from the previous frame reception until the next command transmission (wait time \( t_{\text{COM}} \)).

<2> The Security Set command is transmitted by command frame transmission processing.

<3> A time-out check is performed from command transmission until status frame reception.
   If a time-out occurs, a time-out error [C] is returned (time-out time \( t_{\text{WT13}} \)).

<4> The status code is checked.
   - When \( ST1 = \text{ACK} \): Proceeds to <5>.
   - When \( ST1 \neq \text{ACK} \): Abnormal termination [B]

<5> Waits from the previous frame reception until the next data frame transmission (wait time \( t_{\text{FD3}} \)).

<6> The data frame (security setting data) is transmitted by data frame transmission processing.

<7> A time-out check is performed until status frame reception.
   If a time-out occurs, a time-out error [C] is returned (time-out time \( t_{\text{WT14}} \)).

<8> The status code is checked.
   - When \( ST1 = \text{ACK} \): Proceeds to <9>.
   - When \( ST1 \neq \text{ACK} \): Abnormal termination [D]

<9> A time-out check is performed until status frame reception.
   If a time-out occurs, a time-out error [C] is returned (time-out time \( t_{\text{WT15}} \)).

<10> The status code is checked.
   - When \( ST1 = \text{ACK} \): Normal completion [A]
   - When \( ST1 \neq \text{ACK} \): Abnormal termination [E]

4.14.3 Status at processing completion

<table>
<thead>
<tr>
<th>Status at Processing Completion</th>
<th>Status Code</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Normal completion [A]</td>
<td>Normal acknowledgment (ACK)</td>
<td>06H</td>
</tr>
<tr>
<td>Abnormal termination [B]</td>
<td>Parameter error</td>
<td>05H</td>
</tr>
<tr>
<td>Checksum error</td>
<td>07H</td>
<td>The checksum of the transmitted command frame or data frame does not match.</td>
</tr>
<tr>
<td>Protect error</td>
<td>10H</td>
<td>An already prohibited flag is to be enabled.</td>
</tr>
<tr>
<td>Negative acknowledgment (NACK)</td>
<td>15H</td>
<td>Command frame data is abnormal (such as invalid data length (LEN) or no ETX).</td>
</tr>
<tr>
<td>Time-out error [C]</td>
<td>–</td>
<td>The status frame or data frame was not received within the specified time.</td>
</tr>
<tr>
<td>Abnormal termination [D], [E]</td>
<td>MRG10 error</td>
<td>1AH</td>
</tr>
<tr>
<td></td>
<td>MRG11 error</td>
<td>1BH</td>
</tr>
<tr>
<td></td>
<td>Write error</td>
<td>1CH</td>
</tr>
</tbody>
</table>
4.14.4 Flowchart

Flowchart:

1. Wait from previous frame reception until next command transmission
2. Command frame transmission processing (Security Set)
3. Status frame received?
   - Yes
     - Timed out?
       - No
       - Yes
         - Time-out error [C]
     - Yes
       - Status = ACK?
         - No
           - Abnormal termination [E]
         - Yes
1. Data frame transmission processing (Security data)
2. Status frame received?
   - Yes
     - Timed out?
       - No
       - Yes
         - Time-out error [C]
     - Yes
       - Status = ACK?
         - No
           - Abnormal termination [E]
         - Yes
1. Status frame received?
   - Yes
     - Timed out?
       - No
       - Yes
         - Time-out error [C]
     - Yes
       - Status = ACK?
         - No
           - Abnormal termination [E]
         - Yes
1. Status frame received?
   - Yes
     - Timed out?
       - No
       - Yes
         - Time-out error [C]
     - Yes
       - Status = ACK?
         - No
           - Abnormal termination [E]
         - Yes
1. Status frame received?
   - Yes
     - Timed out?
       - No
       - Yes
         - Time-out error [C]
     - No
       - Status = ACK?
         - No
           - Abnormal termination [E]
         - Yes
1. Status frame received?
   - Yes
     - Timed out?
       - No
       - Yes
         - Time-out error [C]
     - No
       - Status = ACK?
         - No
           - Abnormal termination [E]
         - Yes
1. Abnormal termination [E]
4.14.5 Sample program
The following shows a sample program for Security Set command processing.

```c
u16 fl_ua_setscf(u8 scf, u8 bot, u8 fsws, u8 fswe)
{
    u16 rc;

    /**************************************************************************/
    /* set params */
    /**************************************************************************/
    fl_cmd_prm[0] = 0x00; // "BLK" (must be 0x00)
    fl_cmd_prm[1] = 0x00; // "PAG" (must be 0x00)

    fl_txdata_frm[0] = scf|= 0b11101000; // "FLG" (bit 7,6,5,3 must be '1')
    fl_txdata_frm[1] = bot; // "BOT"
    fl_txdata_frm[2] = 0x00; // "FSWS High"
    fl_txdata_frm[3] = fsws; // "FSWS Low"
    fl_txdata_frm[4] = 0x00; // "FSWE High"
    fl_txdata_frm[5] = fswe; // "FSWE Low"
    fl_txdata_frm[6] = 0xff; // (must be 0xff)
    fl_txdata_frm[7] = 0xff; // (must be 0xff)

    /**************************************************************************/
    /* send command */
    /**************************************************************************/
    fl_wait(tCOM); // wait before sending command
    put_cmd_ua(FL_COM_SET_SECURITY, 3, fl_cmd_prm);

    rc = get_sfrm_ua(fl_ua_sfrm, tWT13_MAX); // get status frame
    switch(rc) {
        case FLC_NO_ERR: break; // continue
        // case FLC_DFTO_ERR: return rc; break; // case [C]
        default: return rc; break; // case [B]
    }

    /**************************************************************************/
    /* send data frame (security setting data) */
    /**************************************************************************/
    fl_wait(tFD4);
    put_dfrm_ua(6, fl_txdata_frm, true); // send security setting data
    rc = get_sfrm_ua(fl_ua_sfrm, tWT14_MAX); // get status frame
    rc = get_sfrm_ua(fl_ua_sfrm, tWT14_MAX+100); // get status frame (+100us
```
is overhead)

```c
switch(rc) {
    case FLC_NO_ERR:   break; // continue
    // case FLC_DFTO_ERR: return rc; break; // case [C]
    default:   return rc; break; // case [B]
}
```

```
/* Check internally verify */
rc = get_sfrm_ua(fl_ua_sfrm, tWT15_MAX); // get status frame
```

```c
if (rc) {
    // case FLC_NO_ERR:   return rc; break; // case [A]
    // case FLC_DFTO_ERR: return rc; break; // case [C]
    // default:   return rc; break; // case [B]

    return rc;
} 
```
CHAPTER 5  FLASH MEMORY PROGRAMMING PARAMETER CHARACTERISTICS

This chapter describes the characteristics of parameter transmitted between the programmer and the devices (78K0R/Kx3-L, 78K0R/Ix3, and 78K0R/Kx3-C) in the flash memory programming mode.

Refer to the user’s manual of the 78K0R/Kx3-L, 78K0R/Ix3, or 78K0R/Kx3-C for electrical specifications when designing a programmer.

5.1 Flash Memory Parameter Characteristics of 78K0R/Kx3-L

5.5.1 Flash memory parameter characteristics in full-speed mode

(1) Flash memory programming mode setting time

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>MIN.</th>
<th>TYP.</th>
<th>MAX.</th>
</tr>
</thead>
<tbody>
<tr>
<td>VDD↑ to FLMD0↑</td>
<td>tDP</td>
<td>0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>FLMD0↑ to RESET↑</td>
<td>tPR</td>
<td>2 ms</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Ready start time from RESET↑</td>
<td>tR0</td>
<td>4.4 ms</td>
<td>100 ms</td>
<td></td>
</tr>
<tr>
<td>Low level data0 (Ready) width</td>
<td>tL0</td>
<td>892 μs</td>
<td>937.5 μs</td>
<td>987 μs</td>
</tr>
<tr>
<td>Wait for low level data1</td>
<td>tL1</td>
<td>110.6 μs</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Wait for low level data2</td>
<td>tL2</td>
<td>4.5 μs</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Wait for Read command</td>
<td>tL3C</td>
<td>608.1 μs</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Low level data1/data2 width</td>
<td>tL1, tL2</td>
<td>937.5 μs</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Note The low-level width is the same as the 00H data width at 9,600 bps. (It includes the start bit and is therefore “0” data of 9 bits.)

\[ t_{L0} \] is the low-level width of the data transmitted from the 78K0R/Kx3-L firmware. \[ t_{L1} \] and \[ t_{L2} \] are the low-level widths of the data transmitted from the flash memory programmer.
(2) Programming characteristics

<table>
<thead>
<tr>
<th>Wait</th>
<th>Condition</th>
<th>Symbol</th>
<th>MIN.</th>
<th>MAX.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Between data frame transmissions</td>
<td>Data frame reception</td>
<td>( t_{DR} )</td>
<td>9.3 ( \mu s )</td>
<td>1.9 ( \mu s )</td>
</tr>
<tr>
<td></td>
<td>Data frame transmission</td>
<td>( t_{DT} )</td>
<td>0 ( \mu s )</td>
<td>0 ( \mu s )</td>
</tr>
<tr>
<td>From status frame transmission until data frame transmission</td>
<td>—</td>
<td>( t_{DR1} )</td>
<td>2.3 ( \mu s )</td>
<td>0 ( \mu s )</td>
</tr>
<tr>
<td>From status frame transmission until data frame reception (1)</td>
<td>Programming command</td>
<td>( t_{RD2} )</td>
<td>2.3 ( \mu s )</td>
<td>0 ( \mu s )</td>
</tr>
<tr>
<td>From status frame transmission until data frame reception (2)</td>
<td>Verify command</td>
<td>( t_{RD3} )</td>
<td>83.8 ( \mu s )</td>
<td>0 ( \mu s )</td>
</tr>
<tr>
<td>From status frame transmission until data frame reception (3)</td>
<td>Security setting command</td>
<td>( t_{RD4} )</td>
<td>236.2 ( \mu s )</td>
<td>0 ( \mu s )</td>
</tr>
<tr>
<td>From status frame transmission until command frame reception</td>
<td>Note 3</td>
<td>( t_{COM} )</td>
<td>13.2 ( \mu s )</td>
<td>2.6 ( \mu s )</td>
</tr>
</tbody>
</table>

**Notes 1.** Use the value in the upper row after the flash memory programming mode is set and until the transmission of the Baud Rate Set command of the programmer finishes. Use the value in the lower row from the time of the transmission of the Reset command after the Baud Rate Set command is transmitted.

2. Enable successive reception for the programmer. Also, set the time-out time for the programmer to at least 3 seconds.

3. Use the value in the upper row after the flash memory programming mode is set and until the transmission of the Reset command finishes after the Baud Rate Set command of the programmer is transmitted. Use the value in the lower row from the time of the transmission of the Reset command after the Baud Rate Set command is transmitted.

**Remark** The waits are defined as follows.

\(<t_{DR}, t_{RD2}, t_{RD3}, t_{RD4}, t_{COM}>\)

The 78K0R/Kx3-L can execute the next communication after the MIN. time has elapsed after completion of the current communication.

The programmer needs to transmit the following data within the period from the MIN. time to the MAX. time after completion of the current communication.

The MAX. time is not specified, but use approximately 3 seconds.

\(<t_{DT}, t_{RD1}>\)

The 78K0R/Kx3-L can execute the next communication after the MIN. time has elapsed after completion of the current communication.

The programmer needs to be ready for reception of the following data within the MIN. time after completion of the current communication.

The MAX. time is not specified, but set the timeout to approximately 3 seconds.
### (3) Command characteristics

<table>
<thead>
<tr>
<th>Command</th>
<th>Symbol</th>
<th>Condition</th>
<th>MIN.</th>
<th>MAX.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Reset</td>
<td>( t_{WT0} )</td>
<td>-</td>
<td>0(^{\text{Note 1}})</td>
<td></td>
</tr>
<tr>
<td>Chip Erase</td>
<td>( t_{WT1} )</td>
<td>-</td>
<td>(34.8 + 1.8 \times \text{total number of blocks}) \text{ms}</td>
<td>(877.8 + 56.3 \times \text{total number of blocks}) \text{ms}</td>
</tr>
<tr>
<td>Block Erase</td>
<td>( t_{WT2}^{\text{Note 2}} )</td>
<td>-</td>
<td>10.6 \text{ms}</td>
<td>(0.8 + 251.9 \times \text{execution count of simultaneous selection and erasure} + 55.0 \times \text{number of blocks to be erased}) \text{ms}</td>
</tr>
<tr>
<td>Programming</td>
<td>( t_{WT3} )</td>
<td>-</td>
<td>0(^{\text{Note 1}})</td>
<td></td>
</tr>
<tr>
<td></td>
<td>( t_{WT4}^{\text{Note 3}} )</td>
<td>-</td>
<td>1.6 \text{ms}</td>
<td>41.9 \text{ms}</td>
</tr>
<tr>
<td></td>
<td>( t_{WT5}^{\text{Note 4}} )</td>
<td>Block 0</td>
<td>30.7 \text{ms}</td>
<td>633.5 \text{ms}</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Other than block 0</td>
<td>4.3 \text{ms}</td>
<td>6.7 \text{ms}</td>
</tr>
<tr>
<td>Verify</td>
<td>( t_{WT6} )</td>
<td>-</td>
<td>0(^{\text{Note 1}})</td>
<td></td>
</tr>
<tr>
<td></td>
<td>( t_{WT7}^{\text{Note 3}} )</td>
<td>-</td>
<td>0(^{\text{Note 1}})</td>
<td></td>
</tr>
<tr>
<td>Block Blank Check</td>
<td>( t_{WT8}^{\text{Note 4}} )</td>
<td>-</td>
<td>2.0 \text{ms}</td>
<td>3.7 \text{ms}</td>
</tr>
<tr>
<td>Baud Rate Set</td>
<td>( t_{WT9} )</td>
<td>-</td>
<td>205.3 \text{μs}</td>
<td>3.7 \text{ms}</td>
</tr>
<tr>
<td>Silicon Signature</td>
<td>( t_{WT10} )</td>
<td>-</td>
<td>0(^{\text{Note 1}})</td>
<td></td>
</tr>
<tr>
<td>Version Get</td>
<td>( t_{WT11} )</td>
<td>-</td>
<td>0(^{\text{Note 1}})</td>
<td></td>
</tr>
<tr>
<td>Security Set</td>
<td>( t_{WT12} )</td>
<td>-</td>
<td>0(^{\text{Note 1}})</td>
<td></td>
</tr>
<tr>
<td></td>
<td>( t_{WT13} )</td>
<td>-</td>
<td>0(^{\text{Note 1}})</td>
<td></td>
</tr>
<tr>
<td></td>
<td>( t_{WT14} )</td>
<td>-</td>
<td>7.5 \text{μs}</td>
<td>14.1 \text{μs}</td>
</tr>
<tr>
<td></td>
<td>( t_{WT15} )</td>
<td>-</td>
<td>2.6 \text{μs}</td>
<td>626.8 \text{ms}</td>
</tr>
<tr>
<td>Checksum</td>
<td>( t_{WT16} )</td>
<td>-</td>
<td>0(^{\text{Note 1}})</td>
<td></td>
</tr>
</tbody>
</table>

**Notes**
1. Reception must be enabled for the programmer before command frame transmission.
2. See [5.4 Simultaneous Selection and Erasure Performed by Block Erase Command](#) for the calculation method of the execution count of simultaneous selection and erasure.
3. Time for 256-byte data transmission
4. Time for one block transmission

**Remark** The waits are defined as follows.

<\( t_{WT0} \) to \( t_{WT8} \), \( t_{WT11} \) to \( t_{WT16} \>)

The 78K0R/Kx3-L completes command processing between the MIN. and MAX. times and transmits a status frame.

For commands with a specified MAX. time, the programmer must wait for the start bit of the reception frame until the MAX. time has elapsed and then perform time-out processing.

For commands without a specified MAX. time, set the timeout to approximately 3 seconds.

<\( t_{WT10} \)>

The 78K0R/Kx3-L can execute the next communication after the MIN. time has elapsed after completion of the current communication.

The programmer needs to transmit the following data within the period from the MIN. time to the MAX. time after completion of the current communication.

The MAX. time is not specified, but use approximately 3 seconds.
### 5.1.2 Flash memory parameter characteristics in wide-voltage mode

#### (1) Flash memory programming mode setting time

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>MIN.</th>
<th>TYP.</th>
<th>MAX.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vcc↑ to FLMD0↑</td>
<td>tDP</td>
<td>0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>FLMD0↑ to RESET↑</td>
<td>tPR</td>
<td>2 ms</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Ready start time from RESET↑</td>
<td>tR0</td>
<td>4.4 ms</td>
<td>100 ms</td>
<td></td>
</tr>
<tr>
<td>Low level data0 (Ready) width</td>
<td>tl0</td>
<td>892 μs</td>
<td>937.5 μs</td>
<td>987 μs</td>
</tr>
<tr>
<td>Wait for low level data1</td>
<td>t01</td>
<td>110.6 μs</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Wait for low level data2</td>
<td>t02</td>
<td>4.5 μs</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Wait for Read command</td>
<td>tC</td>
<td>608.1 μs</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Low level data1/data2 width</td>
<td>tl1, tl2</td>
<td></td>
<td></td>
<td>937.5 μs</td>
</tr>
</tbody>
</table>

**Note**  The low-level width is the same as the 00H data width at 9,600 bps. (It includes the start bit and is therefore "0" data of 9 bits.)

tl0 is the low-level width of the data transmitted from the 78K0R/Kx3-L firmware. tl1 and tl2 are the low-level widths of the data transmitted from the flash programmer.
(2) Programming characteristics

<table>
<thead>
<tr>
<th>Wait</th>
<th>Condition</th>
<th>Symbol</th>
<th>MIN.</th>
<th>MAX.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Between data frame transmissions</td>
<td>Data frame reception</td>
<td>t_{DR}</td>
<td>9.3 μs</td>
<td></td>
</tr>
</tbody>
</table>
| Data frame transmission                    |                               | t_{DT} | 0
| From status frame transmission until data frame transmission |                               | t_{FD1} | 0$^{Note}$ |
| From status frame transmission until data frame reception (1) | Programming command          | t_{FD2} | 11.4 μs |        |
| From status frame transmission until data frame reception (2) | Verify command               | t_{FD3} | 416.4 μs |        |
| From status frame transmission until data frame reception (3) | Security setting command      | t_{FD4} | 985.8 μs |        |
| From status frame transmission until command frame reception | -                             | t_{COM} | 13.2 μs |        |

**Note**  Enable successive reception for the programmer.

**Remark** The waits are defined as follows.

<\text{t}_{DR}, \text{t}_{FD2}, \text{t}_{FD3}, \text{t}_{FD4}, \text{t}_{COM}>

The 78K0R/Kx3-L can execute the next communication after the MIN. time has elapsed after completion of the current communication.

The programmer needs to transmit the following data within the period from the MIN. time to the MAX. time after completion of the current communication.

The MAX. time is not specified, but use approximately 3 seconds.

<\text{t}_{DT}, \text{t}_{FD1}>

The 78K0R/Kx3-L can execute the next communication after the MIN. time has elapsed after completion of the current communication.

The programmer needs to be ready for reception of the following data within the MIN. time after completion of the current communication.

The MAX. time is not specified, but set the timeout to approximately 3 seconds.
(3) Command characteristics

<table>
<thead>
<tr>
<th>Command</th>
<th>Symbol</th>
<th>Condition</th>
<th>MIN.</th>
<th>MAX.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Reset</td>
<td>tWT0</td>
<td>–</td>
<td>0 Note 1</td>
<td></td>
</tr>
<tr>
<td>Chip Erase</td>
<td>tWT1</td>
<td>–</td>
<td>(76.0 + 9.3 \times \text{total number of blocks}) ms</td>
<td>(1420.1 + 281.1 \times \text{total number of blocks}) ms</td>
</tr>
<tr>
<td>Block Erase</td>
<td>tWT2</td>
<td>–</td>
<td>20.3 ms</td>
<td>(3.3 + 271.6 \times \text{execution count of simultaneous selection and erasure} + 275.0 \times \text{number of blocks to be erased}) ms</td>
</tr>
<tr>
<td>Programming</td>
<td>tWT3</td>
<td>–</td>
<td>0 Note 1</td>
<td></td>
</tr>
<tr>
<td></td>
<td>tWT4</td>
<td>–</td>
<td>6.6 ms</td>
<td>149.9 ms</td>
</tr>
<tr>
<td></td>
<td>tWT5</td>
<td>Block 0</td>
<td>89.8 ms</td>
<td>1187.5 ms</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Other than block 0</td>
<td>23.1 ms</td>
<td>34.9 ms</td>
</tr>
<tr>
<td>Verify</td>
<td>tWT6</td>
<td>–</td>
<td>0 Note 1</td>
<td></td>
</tr>
<tr>
<td></td>
<td>tWT7</td>
<td>–</td>
<td>0 Note 1</td>
<td></td>
</tr>
<tr>
<td>Block Blank Check</td>
<td>tWT8</td>
<td>–</td>
<td>9.9 ms</td>
<td>18.0 ms</td>
</tr>
<tr>
<td>Baud Rate Set</td>
<td>tWT10</td>
<td>–</td>
<td>379.2 \mu S</td>
<td></td>
</tr>
<tr>
<td>Silicon Signature</td>
<td>tWT11</td>
<td>–</td>
<td>0 Note 1</td>
<td></td>
</tr>
<tr>
<td>Version Get</td>
<td>tWT12</td>
<td>–</td>
<td>0 Note 1</td>
<td></td>
</tr>
<tr>
<td>Security Set</td>
<td>tWT13</td>
<td>–</td>
<td>0 Note 1</td>
<td></td>
</tr>
<tr>
<td></td>
<td>tWT14</td>
<td>–</td>
<td>37.6 \mu S</td>
<td>70.2 \mu S</td>
</tr>
<tr>
<td></td>
<td>tWT15</td>
<td>–</td>
<td>13.4 \mu S</td>
<td>1152.3 ms</td>
</tr>
<tr>
<td>Checksum</td>
<td>tWT16</td>
<td>–</td>
<td>0 Note 1</td>
<td></td>
</tr>
</tbody>
</table>

Notes
1. Reception must be enabled for the programmer before command frame transmission.
2. See 5.4 Simultaneous Selection and Erasure Performed by Block Erase Command for the calculation method of the execution count of simultaneous selection and erasure.
3. Time for 256-byte data transmission
4. Time for one block transmission

Remark
The waits are defined as follows.

<\text{tWT0} to \text{tWT8}, \text{tWT11} to \text{tWT16}>

The 78K0R/Kx3-L completes command processing between the MIN. and MAX. times and transmits a status frame.
For commands with a specified MAX. time, the programmer must wait for the start bit of the reception frame until the MAX. time has elapsed and then perform time-out processing.
For commands without a specified MAX. time, set the timeout to approximately 3 seconds.

<\text{tWT10}>

The 78K0R/Kx3-L can execute the next communication after the MIN. time has elapsed after completion of the current communication.
The programmer needs to transmit the following data within the period from the MIN. time to the MAX. time after completion of the current communication.
The MAX. time is not specified, but use approximately 3 seconds.
5.2 Flash Memory Parameter Characteristics of 78K0R/Ix3

(1) Flash memory programming mode setting time

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>MIN.</th>
<th>TYP.</th>
<th>MAX.</th>
</tr>
</thead>
<tbody>
<tr>
<td>VDD↑ to FLMD0↑</td>
<td>tDP</td>
<td>0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>FLMD0↑ to RESET↑</td>
<td>tPR</td>
<td>2 ms</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Ready start time from RESET↑</td>
<td>tR0</td>
<td>4.4 ms</td>
<td>100 ms</td>
<td></td>
</tr>
<tr>
<td>Low level data0 (Ready) width&lt;sup&gt;Note&lt;/sup&gt;</td>
<td>tL0</td>
<td>892 µs</td>
<td>937.5 µs</td>
<td>987 µs</td>
</tr>
<tr>
<td>Wait for low level data1</td>
<td>tL1</td>
<td>110.6 µs</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Wait for low level data2</td>
<td>tL2</td>
<td>4.5 µs</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Wait for Read command</td>
<td>tLc</td>
<td>608.1 µs</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Low level data1/data2 width&lt;sup&gt;Note&lt;/sup&gt;</td>
<td>tL1, tL2</td>
<td>937.5 µs</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<sup>Note</sup> The low-level width is the same as the 00H data width at 9,600 bps. (It includes the start bit and is therefore “0” data of 9 bits.)

- tL0 is the low-level width of the data transmitted from the 78K0R/Ix3 firmware.
- tL1 and tL2 are the low-level widths of the data transmitted from the flash programmer.
## (2) Programming characteristics

<table>
<thead>
<tr>
<th>Wait</th>
<th>Condition</th>
<th>Symbol</th>
<th>MIN.</th>
<th>MAX.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Between data frame transmissions</td>
<td>Data frame reception</td>
<td>tDR</td>
<td>9.3 μs</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Data frame transmission</td>
<td>tDT</td>
<td>0 μs</td>
<td></td>
</tr>
<tr>
<td>From status frame transmission until data frame transmission</td>
<td>—</td>
<td>tFD1</td>
<td>0 μs</td>
<td>0 μs</td>
</tr>
<tr>
<td>From status frame transmission until data frame reception (1)</td>
<td>Programming command</td>
<td>tFD2</td>
<td>2.3 μs</td>
<td></td>
</tr>
<tr>
<td>From status frame transmission until data frame reception (2)</td>
<td>Verify command</td>
<td>tFD3</td>
<td>83.8 μs</td>
<td></td>
</tr>
<tr>
<td>From status frame transmission until data frame reception (3)</td>
<td>Security setting command</td>
<td>tFD4</td>
<td>236.2 μs</td>
<td></td>
</tr>
<tr>
<td>From status frame transmission until command frame reception</td>
<td>Note 3</td>
<td>tCOM</td>
<td>13.2 μs</td>
<td></td>
</tr>
</tbody>
</table>

Notes 1. Use the value in the upper row after the flash memory programming mode is set and until the transmission of the Baud Rate Set command of the programmer finishes. Use the value in the lower row from the time of the transmission of the Reset command after the Baud Rate Set command is transmitted.

2. Enable successive reception for the programmer. Also, set the time-out time for the programmer to at least 3 seconds.

3. Use the value in the upper row after the flash memory programming mode is set and until the transmission of the Reset command finishes after the Baud Rate Set command of the programmer is transmitted. Use the value in the lower row from the time of the transmission of the Reset command after the Baud Rate Set command is transmitted.

Remark The waits are defined as follows.

\(<t_{DR}, t_{FD2}, t_{FD3}, t_{FD4}, t_{COM}>\)

The 78K0R/Ix3 can execute the next communication after the MIN. time has elapsed after completion of the current communication.

The programmer needs to transmit the following data within the period from the MIN. time to the MAX. time after completion of the current communication.

The MAX. time is not specified, but use approximately 3 seconds.

\(<t_{DT}, t_{FD1}>\)

The 78K0R/Ix3 can execute the next communication after the MIN. time has elapsed after completion of the current communication.

The programmer needs to be ready for reception of the following data within the MIN. time after completion of the current communication.

The MAX. time is not specified, but set the timeout to approximately 3 seconds.
## (3) Command characteristics

<table>
<thead>
<tr>
<th>Command</th>
<th>Symbol</th>
<th>Condition</th>
<th>MIN.</th>
<th>MAX.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Reset</td>
<td>tWT0</td>
<td></td>
<td>0&lt;sup&gt;Note 1&lt;/sup&gt;</td>
<td></td>
</tr>
<tr>
<td>Chip Erase</td>
<td>tWT1</td>
<td></td>
<td>(34.8 + 1.8 × total number of blocks) ms</td>
<td>(877.8 + 56.3 × total number of blocks) ms</td>
</tr>
<tr>
<td>Block Erase</td>
<td>tWT2</td>
<td></td>
<td>10.6 ms</td>
<td>(0.8 + 251.9 × execution count of simultaneous selection and erasure + 55.0 × number of blocks to be erased) ms</td>
</tr>
<tr>
<td>Programming</td>
<td>tWT3</td>
<td></td>
<td>0&lt;sup&gt;Note 1&lt;/sup&gt;</td>
<td></td>
</tr>
<tr>
<td></td>
<td>tWT4</td>
<td></td>
<td>1.6 ms</td>
<td>41.9 ms</td>
</tr>
<tr>
<td></td>
<td>tWT5</td>
<td>Block 0</td>
<td>30.7 ms</td>
<td>633.5 ms</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Other than block 0</td>
<td>4.3 ms</td>
<td>6.7 ms</td>
</tr>
<tr>
<td>Verify</td>
<td>tWT6</td>
<td></td>
<td>0&lt;sup&gt;Note 1&lt;/sup&gt;</td>
<td></td>
</tr>
<tr>
<td></td>
<td>tWT7</td>
<td></td>
<td>0&lt;sup&gt;Note 1&lt;/sup&gt;</td>
<td></td>
</tr>
<tr>
<td>Block Blank Check</td>
<td>tWT8</td>
<td></td>
<td>2.0 ms</td>
<td>3.7 ms</td>
</tr>
<tr>
<td>Baud Rate Set</td>
<td>tWT9</td>
<td></td>
<td>205.3 μs</td>
<td></td>
</tr>
<tr>
<td>Silicon Signature</td>
<td>tWT10</td>
<td></td>
<td>0&lt;sup&gt;Note 1&lt;/sup&gt;</td>
<td></td>
</tr>
<tr>
<td>Version Get</td>
<td>tWT11</td>
<td></td>
<td>0&lt;sup&gt;Note 1&lt;/sup&gt;</td>
<td></td>
</tr>
<tr>
<td>Security Set</td>
<td>tWT12</td>
<td></td>
<td>0&lt;sup&gt;Note 1&lt;/sup&gt;</td>
<td></td>
</tr>
<tr>
<td></td>
<td>tWT13</td>
<td></td>
<td>0&lt;sup&gt;Note 1&lt;/sup&gt;</td>
<td></td>
</tr>
<tr>
<td></td>
<td>tWT14</td>
<td></td>
<td>7.5 μs</td>
<td>14.1 μs</td>
</tr>
<tr>
<td></td>
<td>tWT15</td>
<td></td>
<td>2.6 μs</td>
<td>626.8 ms</td>
</tr>
<tr>
<td>Checksum</td>
<td>tWT16</td>
<td></td>
<td>0&lt;sup&gt;Note 1&lt;/sup&gt;</td>
<td></td>
</tr>
</tbody>
</table>

**Notes**

1. Reception must be enabled for the programmer before command frame transmission.
2. See 5.4 Simultaneous Selection and Erasure Performed by Block Erase Command for the calculation method of the execution count of simultaneous selection and erasure.
3. Time for 256-byte data transmission
4. Time for one block transmission

**Remark**

The waits are defined as follows.

\(<tWT0 \text{ to } tWT8, tWT11 \text{ to } tWT16>\>

The 78K0R/Ix3 completes command processing between the MIN. and MAX. times and transmits a status frame.

For commands with a specified MAX. time, the programmer must wait for the start bit of the reception frame until the MAX. time has elapsed and then perform time-out processing.

For commands without a specified MAX. time, set the timeout to approximately 3 seconds.

\(<tWT10>\>

The 78K0R/Ix3 can execute the next communication after the MIN. time has elapsed after completion of the current communication.

The programmer needs to transmit the following data within the period from the MIN. time to the MAX. time after completion of the current communication.

The MAX. time is not specified, but use approximately 3 seconds.
5.3 Flash Memory Parameter Characteristics of 78K0R/Kx3-C

(1) Flash memory programming mode setting time

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>MIN.</th>
<th>TYP.</th>
<th>MAX.</th>
</tr>
</thead>
<tbody>
<tr>
<td>$\mathrm{V}_{\mathrm{DD}} \uparrow$ to $\mathrm{FLMD0} \uparrow$</td>
<td>$t_{\mathrm{DP}}$</td>
<td>0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$\mathrm{FLMD0} \uparrow$ to $\mathrm{RESET} \uparrow$</td>
<td>$t_{\mathrm{PR}}$</td>
<td>2 ms</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Ready start time from $\mathrm{RESET} \uparrow$</td>
<td>$t_{\mathrm{R}}$</td>
<td>2 ms</td>
<td>4.4 ms</td>
<td>100 ms</td>
</tr>
<tr>
<td>Low level data0 (Ready) width Note</td>
<td>$t_{\mathrm{L0}}$</td>
<td>892 $\mu$s</td>
<td>937.5 $\mu$s</td>
<td>987 $\mu$s</td>
</tr>
<tr>
<td>Wait for low level data1</td>
<td>$t_{\mathrm{L1}}$</td>
<td>110.6 $\mu$s</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Wait for low level data2</td>
<td>$t_{\mathrm{L2}}$</td>
<td>4.5 $\mu$s</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Wait for Read command</td>
<td>$t_{\mathrm{C}}$</td>
<td>608.1 $\mu$s</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Low level data1/data2 width Note</td>
<td>$t_{\mathrm{L1}, \mathrm{L2}}$</td>
<td></td>
<td>937.5 $\mu$s</td>
<td></td>
</tr>
</tbody>
</table>

Note: The low-level width is the same as the 00H data width at 9,600 bps. (It includes the start bit and is therefore "0" data of 9 bits.)

$t_{\mathrm{L0}}$ is the low-level width of the data transmitted from the 78K0R/Kx3-C firmware. $t_{\mathrm{L1}}$ and $t_{\mathrm{L2}}$ are the low-level widths of the data transmitted from the flash programmer.
## (2) Programming characteristics

<table>
<thead>
<tr>
<th>Wait</th>
<th>Condition</th>
<th>Symbol</th>
<th>MIN.</th>
<th>MAX.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Between data frame transmissions</td>
<td>Data frame reception</td>
<td>$t_{DR}$</td>
<td>9.3 $\mu$s</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Data frame transmission</td>
<td>$t_{DT}$</td>
<td>1.9 $\mu$s</td>
<td>0 $\mu$s</td>
</tr>
<tr>
<td>From status frame transmission until data frame transmission</td>
<td>–</td>
<td>$t_{FD1}$</td>
<td>0 $\mu$s</td>
<td></td>
</tr>
<tr>
<td>From status frame transmission until data frame reception (1)</td>
<td>Programming command</td>
<td>$t_{FD2}$</td>
<td>2.3 $\mu$s</td>
<td></td>
</tr>
<tr>
<td>From status frame transmission until data frame reception (2)</td>
<td>Verify command</td>
<td>$t_{FD3}$</td>
<td>83.8 $\mu$s</td>
<td></td>
</tr>
<tr>
<td>From status frame transmission until data frame reception (3)</td>
<td>Security setting command</td>
<td>$t_{FD4}$</td>
<td>236.2 $\mu$s</td>
<td></td>
</tr>
<tr>
<td>From status frame transmission until command frame reception</td>
<td>Note 3</td>
<td>$t_{COM}$</td>
<td>13.2 $\mu$s</td>
<td></td>
</tr>
</tbody>
</table>

### Notes 1.
Use the value in the upper row after the flash memory programming mode is set and until the transmission of the Baud Rate Set command of the programmer finishes. Use the value in the lower row from the time of the transmission of the Reset command after the Baud Rate Set command is transmitted.

2. Enable successive reception for the programmer. Also, set the time-out time for the programmer to at least 3 seconds.

3. Use the value in the upper row after the flash memory programming mode is set and until the transmission of the Reset command finishes after the Baud Rate Set command of the programmer is transmitted. Use the value in the lower row from the time of the transmission of the Reset command after the Baud Rate Set command is transmitted.

### Remark
The waits are defined as follows.

$<$\(t_{DR}, t_{FD2}, t_{FD3}, t_{FD4}, t_{COM}\)>$

The 78K0R/Kx3-C can execute the next communication after the MIN. time has elapsed after completion of the current communication.

The programmer needs to transmit the following data within the period from the MIN. time to the MAX. time after completion of the current communication.

The MAX. time is not specified, but use approximately 3 seconds.

$<$\(t_{DT}, t_{FD1}\)>$

The 78K0R/Kx3-C can execute the next communication after the MIN. time has elapsed after completion of the current communication.

The programmer needs to be ready for reception of the following data within the MIN. time after completion of the current communication.

The MAX. time is not specified, but set the timeout to approximately 3 seconds.
### (3) Command characteristics

<table>
<thead>
<tr>
<th>Command</th>
<th>Symbol</th>
<th>Condition</th>
<th>MIN.</th>
<th>MAX.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Reset</td>
<td>tWT0</td>
<td>—</td>
<td>0&lt;sup&gt;Note 1&lt;/sup&gt;</td>
<td></td>
</tr>
<tr>
<td>Chip Erase</td>
<td>tWT1</td>
<td>—</td>
<td>(34.8 + 1.8 × total number of blocks) ms</td>
<td>(877.8 + 56.3 × total number of blocks) ms</td>
</tr>
<tr>
<td>Block Erase</td>
<td>tWT2&lt;sup&gt;Note 2&lt;/sup&gt;</td>
<td>—</td>
<td>10.6 ms</td>
<td>(0.8 + 251.9 × execution count of simultaneous selection and erasure + 55.0 × number of blocks to be erased) ms</td>
</tr>
<tr>
<td>Programming</td>
<td>tWT3</td>
<td>—</td>
<td>0&lt;sup&gt;Note 1&lt;/sup&gt;</td>
<td></td>
</tr>
<tr>
<td></td>
<td>tWT4&lt;sup&gt;Note 2&lt;/sup&gt;</td>
<td>—</td>
<td>1.6 ms</td>
<td>41.9 ms</td>
</tr>
<tr>
<td></td>
<td>tWT5&lt;sup&gt;Note 2&lt;/sup&gt;</td>
<td>Block 0</td>
<td>30.7 ms</td>
<td>633.5 ms</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Other than block 0</td>
<td>4.3 ms</td>
<td>6.7 ms</td>
</tr>
<tr>
<td>Verify</td>
<td>tWT6</td>
<td>—</td>
<td>0&lt;sup&gt;Note 1&lt;/sup&gt;</td>
<td></td>
</tr>
<tr>
<td>Block Blank Check</td>
<td>tWT8&lt;sup&gt;Note 4&lt;/sup&gt;</td>
<td>—</td>
<td>2.0 ms</td>
<td>3.7 ms</td>
</tr>
<tr>
<td>Baud Rate Set</td>
<td>tWT9</td>
<td>—</td>
<td>205.3 μs</td>
<td></td>
</tr>
<tr>
<td>Silicon Signature</td>
<td>tWT11</td>
<td>—</td>
<td>0&lt;sup&gt;Note 1&lt;/sup&gt;</td>
<td></td>
</tr>
<tr>
<td>Version Get</td>
<td>tWT12</td>
<td>—</td>
<td>0&lt;sup&gt;Note 1&lt;/sup&gt;</td>
<td></td>
</tr>
<tr>
<td>Security Set</td>
<td>tWT13</td>
<td>—</td>
<td>0&lt;sup&gt;Note 1&lt;/sup&gt;</td>
<td></td>
</tr>
<tr>
<td></td>
<td>tWT14</td>
<td>—</td>
<td>7.5 μs</td>
<td>14.1 μs</td>
</tr>
<tr>
<td></td>
<td>tWT15</td>
<td>—</td>
<td>2.6 μs</td>
<td>626.8 ms</td>
</tr>
<tr>
<td>Checksum</td>
<td>tWT16</td>
<td>—</td>
<td>0&lt;sup&gt;Note 1&lt;/sup&gt;</td>
<td></td>
</tr>
</tbody>
</table>

**Notes**

1. Reception must be enabled for the programmer before command frame transmission.
2. See 5.4 *Simultaneous selection and erasure performed by Block Erase command* for the calculation method of the execution count of simultaneous selection and erasure.
3. Time for 256-byte data transmission
4. Time for one block transmission

**Remark** The waits are defined as follows.

<<tWT0 to tWT8, tWT11 to tWT16>>

The 78K0R/Kx3-C completes command processing between the MIN. and MAX. times and transmits a status frame.

For commands with a specified MAX. time, the programmer must wait for the start bit of the reception frame until the MAX. time has elapsed and then perform time-out processing.

For commands without a specified MAX. time, set the timeout to approximately 3 seconds.

<<<tWT10>>>

The 78K0R/Kx3-C can execute the next communication after the MIN. time has elapsed after completion of the current communication.

The programmer needs to transmit the following data within the period from the MIN. time to the MAX. time after completion of the current communication.

The MAX. time is not specified, but use approximately 3 seconds.
5.4 Simultaneous Selection and Erasure Performed by Block Erase Command

The Block Erase command of the 78K0R/Kx3-L, 78K0R/Ix3, and 78K0R/Kx3-C is executed by repeating "simultaneous selection and erasure", which erases multiple blocks simultaneously.

The wait time inserted during Block Erase command execution is therefore equal to the total execution time of "simultaneous selection and erasure".

To calculate the "total execution time of simultaneous selection and erasure", the execution count (M) of the simultaneous selection and erasure must first be calculated.

"M" is calculated by obtaining the number of blocks to be erased simultaneously (number of blocks to be selected and erased simultaneously).

The following describes the method for calculating the number of blocks to be selected and erased simultaneously and the execution count (M).

5.4.1 Calculation of number of blocks to be selected and erased simultaneously

The number of blocks to be selected and erased simultaneously should be 1, 2, 4, 8, 16, 32, 64, or 128, depending on which satisfies all of the following conditions.

[Condition 1]
(Number of blocks to be erased) ≥ (Number of blocks to be selected and erased simultaneously)

[Condition 2]
(Start block number) ÷ (Number of blocks to be selected and erased simultaneously) = Remainder is 0

[Condition 3]
The maximum value among the values that satisfy both Conditions 1 and 2
5.4.2 Calculation of the execution count (M) of simultaneous selection and erasure

Calculation of the execution count (M) is illustrated in the following flowchart.

Note Based on the maximum value of SSER_BKNUM (128), obtain the value that satisfies Conditions 1 and 2 by executing SSER_BKNUM ÷ 2; Condition 3 is then satisfied.
Example 1  Erasing blocks 1 to 127 (N (number of blocks to be erased) = 127)

<1> The first start block number is 1 and the number of blocks to be erased is 127; the values that satisfy Condition 1 are therefore 1, 2, 4, 8, 16, 32, and 64. Moreover, the value that satisfies Condition 2 is 1 and the value that satisfies Condition 3 is 1, so the number of blocks to be selected and erased simultaneously is 1; only block 1 is then erased.

<2> After block 1 is erased, the next start block number is 2 and the number of blocks to be erased is 126; the values that satisfy Condition 1 are therefore 1, 2, 4, 8, 16, 32, and 64. Moreover, the values that satisfy Condition 2 are 1 and 2, the value that satisfies Condition 3 is 2, so the number of blocks to be selected and erased simultaneously is 2; blocks 2 and 3 are then erased.

<3> After blocks 2 and 3 are erased, the next start block number is 4 and the number of blocks to be erased is 124; the values that satisfy Condition 1 are therefore 1, 2, 4, 8, 16, 32, and 64. Moreover, the values that satisfy Condition 2 are 1, 2, and 4, the value that satisfies Condition 3 is 4, so the number of blocks to be selected and erased simultaneously is 4; blocks 4 to 7 are then erased.

<4> After blocks 4 to 7 are erased, the next start block number is 8 and the number of blocks to be erased is 120; the values that satisfy Condition 1 are therefore 1, 2, 4, 8, 16, 32, and 64. Moreover, the values that satisfy Condition 2 are 1, 2, 4, and 8, the value that satisfies Condition 3 is 8, so the number of blocks to be selected and erased simultaneously is 8; blocks 8 to 15 are then erased.

<5> After blocks 8 to 15 are erased, the next start block number is 16 and the number of blocks to be erased is 112; the values that satisfy Condition 1 are therefore 1, 2, 4, 8, 16, 32, and 64. Moreover, the values that satisfy Condition 2 are 1, 2, 4, 8, and 16, the value that satisfies Condition 3 is 16, so the number of blocks to be selected and erased simultaneously is 16; blocks 16 to 31 are then erased.

<6> After blocks 16 to 31 are erased, the next start block number is 32 and the number of blocks to be erased is 96; the values that satisfy Condition 1 are therefore 1, 2, 4, 8, 16, 32, and 64. Moreover, the values that satisfy Condition 2 are 1, 2, 4, 8, 16, and 32, the value that satisfies Condition 3 is 32, so the number of blocks to be selected and erased simultaneously is 32; blocks 32 to 63 are then erased.

<7> After blocks 32 to 63 are erased, the next start block number is 64 and the number of blocks to be erased is 64; the values that satisfy Condition 1 are therefore 1, 2, 4, 8, 16, 32, and 64. Moreover, the values that satisfy Condition 2 are 1, 2, 4, 8, 16, 32, and 64, the value that satisfies Condition 3 is 64, so the number of blocks to be selected and erased simultaneously is 64; blocks 64 to 127 are then erased.

Therefore, simultaneous selection and erasure is executed seven times (1, 2 and 3, 4 to 7, 8 to 15, 16 to 31, 32 to 63, and 64 to 127) to erase blocks 1 to 127, so M = 7 is obtained.
Block configuration when executing simultaneous selection and erasure (when erasing blocks 1 to 127)

<User area>

<Range of blocks that can be selected and erased simultaneously>
Example 2  Erasing blocks 5 to 10 (N (number of blocks to be erased) = 6)

<1> The first start block number is 5 and the number of blocks to be erased is 6; the values that satisfy Condition 1 are therefore 1, 2, and 4.
Moreover, the value that satisfies Condition 2 is 1 and the value that satisfies Condition 3 is 1, so the number of blocks to be selected and erased simultaneously is 1; only block 5 is the erased.

<2> After block 5 is erased, the next start block number is 6 and the number of blocks to be erased is 5; the values that satisfy Condition 1 are therefore 1, 2, and 4.
Moreover, the values that satisfy Condition 2 are 1 and 2, the value that satisfies Condition 3 is 2, so the number of blocks to be selected and erased simultaneously is 2; blocks 6 and 7 are then erased.

<3> After blocks 6 and 7 are erased, the next start block number is 8 and the number of blocks to be erased is 3; the values that satisfy Condition 1 are therefore 1 and 2.
Moreover, the values that satisfy Condition 2 are 1 and 2, the value that satisfies Condition 3 is 2, so the number of blocks to be selected and erased simultaneously is 2; blocks 8 and 9 are then erased.

<4> After blocks 8 and 9 are erased, the next start block number is 10 and the number of blocks to be erased is 1; the value that satisfies Condition 1 is therefore 1. This also satisfies Conditions 2 and 3, so the number of blocks to be selected and erased simultaneously is 1; block 10 is then erased.

Therefore, simultaneous selection and erasure is executed four times (5, 6 and 7, 8 and 9, and 10) to erase blocks 5 to 10, so M = 4 is obtained.
Block configuration when executing simultaneous selection and erasure (when erasing blocks 5 to 10)

<User area>

<Range of blocks that can be selected and erased simultaneously>
Example 3  Erasing blocks 25 to 73 (N (number of blocks to be erased) = 49)

<1>  The first start block number is 25 and the number of blocks to be erased is 49; the values that satisfy Condition 1 are therefore 1, 2, 4, 8, 16, and 32. Moreover, the value that satisfies Condition 2 is 1 and the value that satisfies Condition 3 is 1, so the number of blocks to be selected and erased simultaneously is 1; only block 25 is then erased.

<2>  After block 25 is erased, the next start block number is 26 and the number of blocks to be erased is 48; the values that satisfy Condition 1 are therefore 1, 2, 4, 8, 16, and 32. Moreover, the values that satisfy Condition 2 are 1 and 2, the value that satisfies Condition 3 is 2, so the number of blocks to be selected and erased simultaneously is 2; blocks 26 and 27 are then erased.

<3>  After blocks 26 and 27 are erased, the next start block number is 28 and the number of blocks to be erased is 46; the values that satisfy Condition 1 are therefore 1, 2, 4, 8, 16, and 32. Moreover, the values that satisfy Condition 2 are 1, 2, and 4, the value that satisfies Condition 3 is 4, so the number of blocks to be selected and erased simultaneously is 4; blocks 28 to 31 are then erased.

<4>  After blocks 28 to 31 are erased, the next start block number is 32 and the number of blocks to be erased is 42; the values that satisfy Condition 1 are therefore 1, 2, 4, 8, 16, and 32. Moreover, the values that satisfy Condition 2 are 1, 2, 4, 8, and 32, the value that satisfies Condition 3 is 32, so the number of blocks to be selected and erased simultaneously is 32; blocks 32 to 63 are then erased.

<5>  After blocks 32 to 63 are erased, the next start block number is 64, and the number of blocks to be erased is 10; the values that satisfy Condition 1 are therefore 1, 2, 4, and 8. Moreover, the values that satisfy Condition 2 are 1, 2, 4, and 8, the value that satisfies Condition 3 is 8, so the number of blocks to be selected and erased simultaneously is 8; blocks 64 to 71 are then erased.

<6>  After blocks 64 to 71 are erased, the next start block number is 72, and the number of blocks to be erased is 2; the values that satisfy Condition 1 are therefore 1 and 2. Moreover, the values that satisfy Condition 2 are 1 and 2, the value that satisfies Condition 3 is 2, so the number of blocks to be selected and erased simultaneously is 2; blocks 72 and 73 are then erased.

Therefore, simultaneous selection and erasure is executed six times (25, 26 and 27, 28 to 31, 32 to 63, 64 to 71, and 72 and 73) to erase blocks 25 to 73, so $M = 6$ is obtained.
Block configuration when executing simultaneous selection and erasure (when erasing blocks 25 to 73)
5.5 UART Communication Mode

In the figure below, TOOL0 is illustrated as two separate lines for the sake of description, but it is actually a single line. The VDD level of TOOL0 can be achieved by using a pull-up resistor (the pin is Hi-Z).

(a) Data frame

(b) Programming mode setting

(c) Reset command

(d) Chip Erase command/Block Erase command/Block Blank Check command/Oscillating Frequency Set command
(e) Baud Rate Set command

(f) Silicon Signature command/Version Get command

(g) Checksum command

(h) Programming command
**(i) Verify command**

```
TOOL0 (output)  
| Command frame | Status frame | Data frame (1) | Status frame (1) |
TOOL0 (input)   
```

```
Data frame (n - 1) | Status frame (n - 1) | Data frame (n) | Status frame (n) |
```

**(j) Security Set command**

```
TOOL0 (output)  
| Command frame | Status frame | Data frame | Status frame | Status frame |
TOOL0 (input)   
```

```
Command frame | Status frame | Data frame | Status frame | Status frame |
```

**(k) Wait before command frame transmission**

```
TOOL0 (output)  
| Status frame | Command frame |
TOOL0 (input)   
```

```
Status frame | Command frame |
```

APPENDIX A  CIRCUIT DIAGRAMS (REFERENCE)

Figure A-1 shows a circuit diagram of the programmer and the 78K0R/Kx3-L, for reference.
APPENDIX A CIRCUIT DIAGRAMS (REFERENCE)

Figure A-1. Reference Circuit Diagram of Programmer and 78K0R/Kx3-L (Main Board)

78K0R_Kx3-L Flash Programmer Sample Application Main Board for Monowire UART I/F
(Wide-voltage mode)

(VDD = 5.0V)

Remark For details about connecting unused pins shown in this circuit diagram, see the user’s manual of each product.
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