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April 1st, 2010
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## Application Note

### 78K0R/Kx3

16-bit Single-Chip Microcontrollers

Flash Memory Programming (Programmer)

<table>
<thead>
<tr>
<th>μPD78F1142</th>
<th>μPD78F1152</th>
<th>μPD78F1162</th>
</tr>
</thead>
<tbody>
<tr>
<td>μPD78F1143</td>
<td>μPD78F1153</td>
<td>μPD78F1163</td>
</tr>
<tr>
<td>μPD78F1144</td>
<td>μPD78F1154</td>
<td>μPD78F1164</td>
</tr>
<tr>
<td>μPD78F1145</td>
<td>μPD78F1155</td>
<td>μPD78F1165</td>
</tr>
<tr>
<td>μPD78F1146</td>
<td>μPD78F1156</td>
<td>μPD78F1166</td>
</tr>
<tr>
<td></td>
<td></td>
<td>μPD78F1167</td>
</tr>
<tr>
<td></td>
<td></td>
<td>μPD78F1168</td>
</tr>
</tbody>
</table>
NOTES FOR CMOS DEVICES

1. VOLTAGE APPLICATION WAVEFORM AT INPUT PIN
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the
   CMOS device stays in the area between $V_{IL}$ (MAX) and $V_{IH}$ (MIN) due to noise, etc., the device may
   malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed,
   and also in the transition period when the input level passes through the area between $V_{IL}$ (MAX) and
   $V_{IH}$ (MIN).

2. HANDLING OF UNUSED INPUT PINS
   Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is
   possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS
   devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed
   high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to $V_{DD}$ or $GND$
   via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must
   be judged separately for each device and according to related specifications governing the device.

3. PRECAUTION AGAINST ESD
   A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and
   ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as
   much as possible, and quickly dissipate it when it has occurred. Environmental control must be
   adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that
   easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static
   container, static shielding bag or conductive material. All test and measurement tools including work
   benches and floors should be grounded. The operator should be grounded using a wrist strap.
   Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for
   PW boards with mounted semiconductor devices.

4. STATUS BEFORE INITIALIZATION
   Power-on does not necessarily define the initial status of a MOS device. Immediately after the power
   source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does
   not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the
   reset signal is received. A reset operation must be executed immediately after power-on for devices
   with reset functions.

5. POWER ON/OFF SEQUENCE
   In the case of a device that uses different power supplies for the internal operation and external
   interface, as a rule, switch on the external power supply after switching on the internal power supply.
   When switching the power supply off, as a rule, switch off the external power supply and then the
   internal power supply. Use of the reverse power on/off sequences may result in the application of an
   overvoltage to the internal elements of the device, causing malfunction and degradation of internal
   elements due to the passage of an abnormal current.
   The correct power on/off sequence must be judged separately for each device and according to related
   specifications governing the device.

6. INPUT OF SIGNAL DURING POWER OFF STATE
   Do not input signals or an I/O pull-up power supply while the device is not powered. The current
   injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and
   the abnormal current that passes in the device at this time may cause degradation of internal elements.
   Input of signals during the power off state must be judged separately for each device and according to
   related specifications governing the device.
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INTRODUCTION

Target Readers
This application note is intended for users who understand the functions of the 78K0R/Kx3 and who will use this product to design application systems.

Purpose
The purpose of this application note is to help users understand how to develop dedicated flash memory programmers for rewriting the internal flash memory of the 78K0R/Kx3.

The sample programs and circuit diagrams shown in this document are for reference only and are not intended for use in actual design-ins. Therefore, these sample programs must be used at the user's own risk. Correct operation is not guaranteed if these sample programs are used.

Organization
This manual consists of the following main sections.

• Flash memory programming
• Programmer operating environment
• Basic programmer operation
• Command/data frame format
• Description of command processing
• UART communication mode
• Flash memory programming parameter characteristics

How to Read This Manual
It is assumed that the reader of this manual has general knowledge in the fields of electrical engineering, logic circuits, and microcontrollers.

• To gain a general understanding of functions:
  → Read this manual in the order of the CONTENTS.
• To learn more about the 78K0R/Kx3's hardware functions:
  → See the user's manual of each 78K0R/Kx3 product.

Conventions
Data significance: Higher digits on the left and lower digits on the right
Active low representation: xxx (overscore over pin or signal name)
Note: Footnote for item marked with Note in the text
Caution: Information requiring particular attention
Remark: Supplementary information
Numerical representation: Binary ..........................xxxx or xxxxB
                 Decimal ..........................xxxx
                 Hexadecimal ..........................xxxxH
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CHAPTER 1  FLASH MEMORY PROGRAMMING

To rewrite the contents of the internal flash memory of the 78K0R/Kx3, a dedicated flash memory programmer (hereafter referred to as the “programmer”) is usually used.

This application note explains how to develop a dedicated programmer.

1.1 Overview

The 78K0R/Kx3 incorporates firmware that controls flash memory programming. The programming to the internal flash memory is performed by transmitting/receiving commands between the programmer and the 78K0R/Kx3 via serial communication.

Figure 1-1. System Outline of Flash Memory Programming in 78K0R/Kx3
1.2 System Configuration

Examples of the system configuration for programming the flash memory are illustrated in Figure 1-2. This figure illustrates how to program the flash memory with the programmer, under control of a host machine. Depending on how the programmer is connected, the programmer can be used in a standalone mode without using the host machine, if a user program has been downloaded to the programmer in advance.

For example, NEC Electronics’ flash memory programmer PG-FP4 can execute programming either by using the GUI software with a host machine connected or by itself (standalone).

**Figure 1-2. System Configuration**

![System Configuration Diagram]

**Remark** The 78K0R/Kx3 can only communicate via the single-wire UART communication mode.
1.3 Programming Overview

To rewrite the contents of the flash memory with the programmer, the 78K0R/Kx3 must first be set to the flash memory programming mode. After that, transmit commands from the programmer via serial communication, and then rewrite the flash memory. The flowchart of programming is illustrated in Figure 1-3.

Figure 1-3. Programming Flowchart

1.3.1 Setting flash memory programming mode

Supply a specific voltage to the flash memory programming mode setting pin (FLMD0) in the 78K0R/Kx3 and release a reset; the flash memory programming mode is then set.
1.3.2 Manipulating flash memory via command transmission/reception

The flash memory incorporated in the 78K0R/Kx3 has functions to rewrite the flash memory contents. The flash memory manipulating functions shown in Table 1-1 are available.

Table 1-1. Outline of Flash Memory Functions

<table>
<thead>
<tr>
<th>Function</th>
<th>Outline</th>
</tr>
</thead>
<tbody>
<tr>
<td>Erase</td>
<td>Erases the flash memory contents.</td>
</tr>
<tr>
<td>Write</td>
<td>Writes data to the flash memory.</td>
</tr>
<tr>
<td>Verify</td>
<td>Compares the flash memory contents with data for verify.</td>
</tr>
<tr>
<td>Acquisition of information</td>
<td>Reads information related to the flash memory.</td>
</tr>
</tbody>
</table>

To control these functions, the programmer transmits commands to the 78K0R/Kx3 via serial communication. The 78K0R/Kx3 returns the response status for the commands. The programming to the flash memory is performed by repeating these series of serial communications.
1.4 Information Specific to 78K0R/Kx3

The programmer must manage product-specific information (such as a device name and memory information). Table 1-2 shows the flash memory size of the 78K0R/Kx3 and Figure 1-4 shows the configuration of the flash memory.

<table>
<thead>
<tr>
<th>Device Name</th>
<th>Flash Memory Size</th>
</tr>
</thead>
<tbody>
<tr>
<td>μPD78F1142</td>
<td>64 KB</td>
</tr>
<tr>
<td>μPD78F1143</td>
<td>96 KB</td>
</tr>
<tr>
<td>μPD78F1144</td>
<td>128 KB</td>
</tr>
<tr>
<td>μPD78F1145</td>
<td>192 KB</td>
</tr>
<tr>
<td>μPD78F1146</td>
<td>256 KB</td>
</tr>
<tr>
<td>μPD78F1152</td>
<td>64 KB</td>
</tr>
<tr>
<td>μPD78F1153</td>
<td>96 KB</td>
</tr>
<tr>
<td>μPD78F1154</td>
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</tr>
<tr>
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</tr>
<tr>
<td>μPD78F1166</td>
<td>256 KB</td>
</tr>
<tr>
<td>μPD78F1167</td>
<td>384 KB</td>
</tr>
<tr>
<td>μPD78F1168</td>
<td>512 KB</td>
</tr>
</tbody>
</table>
Remark Each block consists of 2 KB (this figure only illustrates some parts of entire blocks in the flash memory).
CHAPTER 2 PROGRAMMER OPERATING ENVIRONMENT

2.1 Programmer Control Pins

Table 2-1 lists the pins that the programmer must control to implement the programmer function in the user system. See the following pages for details on each pin.

Table 2-1. Pin Description

<table>
<thead>
<tr>
<th>Signal Name</th>
<th>I/O</th>
<th>Pin Function</th>
<th>Pin Name</th>
<th>Procedure When Connecting</th>
</tr>
</thead>
<tbody>
<tr>
<td>FLMD0</td>
<td>Output</td>
<td>Mode signal</td>
<td>FLMD0</td>
<td>√</td>
</tr>
<tr>
<td>VDD</td>
<td>I/O</td>
<td>VDD voltage generation/monitoring</td>
<td>VDD</td>
<td>√</td>
</tr>
<tr>
<td>EVDD (0/1)</td>
<td></td>
<td></td>
<td>EVDD (0/1)</td>
<td></td>
</tr>
<tr>
<td>AVREF (0/1)</td>
<td></td>
<td></td>
<td>AVREF (0/1)</td>
<td></td>
</tr>
<tr>
<td>GND</td>
<td>–</td>
<td>Ground</td>
<td>–</td>
<td>√</td>
</tr>
<tr>
<td>CLK</td>
<td>Output</td>
<td>Clock output</td>
<td>–</td>
<td>×</td>
</tr>
<tr>
<td>/RESET</td>
<td>Output</td>
<td>Reset signal</td>
<td>RESET</td>
<td>√</td>
</tr>
<tr>
<td>SI/RxD</td>
<td>Input</td>
<td>Receive signal</td>
<td>TOOLD</td>
<td>√</td>
</tr>
<tr>
<td>SO/TxD</td>
<td>Output</td>
<td>Transmit signal</td>
<td>–</td>
<td>×</td>
</tr>
<tr>
<td>SCK</td>
<td>Output</td>
<td>Transfer clock</td>
<td>–</td>
<td>×</td>
</tr>
</tbody>
</table>

Note  When performing off-board write operation, connect this pin to VDD.

When performing on-board write operation, supply the same power as in normal operation mode. (At this time, make sure to set so that $V_{DD} \geq AVREF(0/1)$.)

Remark  
√: Be sure to connect the pin.
×: The pin does not have to be connected.

For the voltage of the pins controlled by the programmer, refer to the user’s manual of the device that is subject to flash memory programming.
2.2 Details of Control Pins

2.2.1 Flash memory programming mode setting pin (FLMD0)

The FLMD0 pin is used to control the operating mode of the 78K0R/Kx3. The 78K0R/Kx3 operates in flash memory programming mode when a specific voltage is supplied to this pin and a reset is released.

2.2.2 Serial interface pin (TOOL0)

The serial interface pin is used to transfer the flash memory writing commands between the programmer and the 78K0R/Kx3.

The following figure illustrates the connection of pins used.

**Figure 2-1. Serial Interface Pin**

![Serial Interface Pin Diagram]
2.2.3 Reset control pin (RESET)

The reset control pin (RESET pin) is used to control the system reset for the 78K0R/Kx3 from the programmer. The flash memory programming mode can be selected when a specific voltage is supplied to the FLMD0 pin and a reset is released.

![Figure 2-2. RESET Pin](image)

2.2.4 VDD/GND control pins

The VDD control pin is used to supply power to the 78K0R/Kx3 from the programmer. Connection of this pin is not necessary when it is not necessary to supply power to the 78K0R/Kx3 from the programmer. However, this pin must be connected regardless of whether the power is supplied from the programmer when the dedicated programmer is used, because the dedicated programmer monitors the power supply status of the 78K0R/Kx3.

The GND control pin must be connected to VSS of the 78K0R/Kx3 regardless of whether the power is supplied from the programmer.

![Figure 2-3. VDD/GND Control Pin](image)

*Note* When performing off-board write operation, connect this pin to VDD.

When performing on-board write operation, supply the same power as in normal operation mode. (At this time, make sure to set so that VDD \( \geq \) AVREF\(_{0/1}\).)

2.2.5 Other pins

For the connection of the pins that are not connected to the programmer, refer to the chapter describing the flash memory in the user’s manual of each device.
2.3 Basic Flowchart

The following illustrates the basic flowchart for performing flash memory rewriting with the programmer.

Figure 2-4. Basic Flowchart for Flash Memory Rewrite Processing

---

- **Basic flow**
- **Power application to target** (See Figure 2-5)
- **Mode setting (reset release)** (See 2.4)
- **Synchronization processing (Reset command)** (See 5.2)
- **Communication speed setting (Baud Rate Set command)** (See 5.3)
- **Signature acquisition (Silicon Signature command)** (See 5.9)
- **Command execution**
  - **Processing completed?**
    - **No**
    - **Yes**
  - **Target power shutdown processing** (See 2.6)
  - **End**

Reset input and power shutdown during rewriting is prohibited because security information may be lost.
2.4 Setting Flash Memory Programming Mode

To rewrite the contents of the flash memory with the programmer, the 78K0R/Kx3 must first be set to the flash memory programming mode by supplying a specific voltage to the flash memory programming mode setting pin (FLMD0) in the 78K0R/Kx3, then releasing a reset.

The following illustrates a timing chart for setting the flash memory programming mode.

![Figure 2-5. Setting Flash Memory Programming Mode](image)

The relationship between the setting of the FLMD0 pin after reset release and the operating mode is shown below.

<table>
<thead>
<tr>
<th>FLMD0</th>
<th>Operating Mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>Low (GND)</td>
<td>Normal operating mode</td>
</tr>
<tr>
<td>High (VDD)</td>
<td>Flash memory programming mode</td>
</tr>
</tbody>
</table>

The relationship between the setting of the FLMD0 pin after reset release and the operating mode is shown below.
2.4.1 Mode setting flowchart

Transition processing to programming mode

RESET pin low output

FLMD0 pin low output

VDD pin high output (Target power supply on)

Wait $t_{DP}$ (min.)

FLMD0 pin high output

Wait $t_{PR}$ (min.)

RESET pin high output

Ready pulse check

OK

Start of time measurement until start of reset command processing $t_{01}$ (min.)

Initialization of UART hardware

Has specified time elapsed until start of reset command processing?

Yes

Normal termination

No

Abnormal termination
2.4.2 Sample program
The following shows a sample program for mode setting processing.

```c
u16 fl_con_dev(void)
{
    extern void init_fl_uart(void);
    extern void init_fl_csi(void);
    extern void stop_UART0(void);

    u16 rc = NO_ERROR;

    SRMK0 = true;       // disable UART Rx INT.
    UARTE0 = false;     // disable UART H.W.
    stop_UART0();       // TxD/RxD = Hi-Z

    pFL_RES = low;      // RESET = low
    pmFL_FLMD0 = PM_OUT; // FLMD0 = Low output
    pFL_FLMD0 = low;
    FL_VDD_HI();        // VDD = high

    fl_wait(tDP);       // wait

    pFL_FLMD0 = hi;      // FLMD0 = high
    fl_wait(tPR);       // wait

    pFL_RES = hi;        // RESET = high

    rc = check_ready_pulse(); // check "READY PULSE" from target device
    if (rc){
        return rc;        // pulse width/timing error
    }
    start_flto(t01);    // start "t01" wait timer

    init_fl_uart();     // Initialize UART h.w.(for Flash device control)
    UARTE0 = true;      // enable UART h.w.
    SRIF0 = false;      // clear UART Rx IRQ flag
    SRMK0 = false;      // enable UART Rx INT.

    while(!check_flto()) // timeout "t01" ?
        ;               // no

    return rc;
    // start RESET command proc.
}
```
2.5 Single-Wire UART Communication Mode

The TOOL0 pin of the 78K0R/Kx3 is used for single-wire UART communication. The communication conditions are as shown below.

<table>
<thead>
<tr>
<th>Item</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Baud rate</td>
<td>Communication is performed at 9,600 bps until the Baud Rate Set command for baud rate setting command processing is transmitted. The transmission rate is changed to the baud rate set by the Baud Rate Set command from the transmission of the Reset command for baud rate command processing. For details of the settable baud rate, refer to 5.3 Baud Rate Set Command.</td>
</tr>
<tr>
<td>Parity bit</td>
<td>None</td>
</tr>
<tr>
<td>Data length</td>
<td>8 bits (LSB first)</td>
</tr>
<tr>
<td>Stop bit</td>
<td>2 bits (programmer → 78K0R/Kx3)/1 bit (78K0R/Kx3 → programmer)</td>
</tr>
</tbody>
</table>

Caution Set the same baud rate to the programmer and 78K0R/Kx3.

2.6 Shutting Down Target Power Supply

After each command execution is completed, shut down the power supply to the target after setting the \texttt{RESET} pin to low level, as shown below.

Set other pins to Hi-Z when shutting down the power supply to the target.

Caution Shutting down the power supply and inputting a reset during command processing are prohibited.

![Figure 2-6. Timing for Terminating Flash Memory Programming Mode](image-url)
2.7 Manipulation of Flash Memory

The flash memory incorporated in the 78K0R/Kx3 has functions to manipulate the flash memory, as listed in Table 2-4. The programmer transmits commands to control these functions to the 78K0R/Kx3, and checks the response status sent from the 78K0R/Kx3, to manipulate the flash memory.

<table>
<thead>
<tr>
<th>Classification</th>
<th>Function Name Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Erase</td>
<td>Chip erase: Erases the entire flash memory area. Clears the security flag.</td>
</tr>
<tr>
<td></td>
<td>Block erase: Erases a specified block in the flash memory.</td>
</tr>
<tr>
<td>Write</td>
<td>Write: Writes data to a specified area in the flash memory.</td>
</tr>
<tr>
<td>Verify</td>
<td>Verify: Compares data acquired from a specified address in the flash memory with data transmitted from the programmer, on the 78K0R/Kx3 side.</td>
</tr>
<tr>
<td>Blank check</td>
<td>Block blank check: Checks the erase status of a specified area in the flash memory.</td>
</tr>
<tr>
<td>Information acquisition</td>
<td>Silicon signature acquisition: Acquires writing protocol information.</td>
</tr>
<tr>
<td></td>
<td>Version acquisition: Acquires version information of the 78K0R/Kx3 and firmware.</td>
</tr>
<tr>
<td></td>
<td>Checksum acquisition: Acquires checksum data of a specified area.</td>
</tr>
<tr>
<td>Other</td>
<td>Reset: Detects synchronization in communication.</td>
</tr>
</tbody>
</table>

2.8 Command List

The commands used by the programmer and their functions are listed below.

<table>
<thead>
<tr>
<th>Command Number</th>
<th>Command Name</th>
<th>Function Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>00H</td>
<td>Reset</td>
<td>Detects synchronization in communication.</td>
</tr>
<tr>
<td>9AH</td>
<td>Baud Rate Set</td>
<td>Sets the baud rate for single-wire UART.</td>
</tr>
<tr>
<td>20H</td>
<td>Chip Erase</td>
<td>Erases the entire flash memory area.</td>
</tr>
<tr>
<td>22H</td>
<td>Block Erase</td>
<td>Erases a specified area in the flash memory.</td>
</tr>
<tr>
<td>40H</td>
<td>Programming</td>
<td>Writes data to a specified area in the flash memory.</td>
</tr>
<tr>
<td>13H</td>
<td>Verify</td>
<td>Compares the contents in a specified area in the flash memory with data transmitted from the programmer.</td>
</tr>
<tr>
<td>32H</td>
<td>Block Blank Check</td>
<td>Checks the erase status of a specified block in the flash memory.</td>
</tr>
<tr>
<td>C0H</td>
<td>Silicon Signature</td>
<td>Acquires 78K0R/Kx3 information (part number, flash memory configuration, etc.).</td>
</tr>
<tr>
<td>C5H</td>
<td>Version Get</td>
<td>Acquires version information of the 78K0R/Kx3 and firmware.</td>
</tr>
<tr>
<td>B0H</td>
<td>Checksum</td>
<td>Acquires checksum data of a specified area.</td>
</tr>
<tr>
<td>A0H</td>
<td>Security Set</td>
<td>Sets security information.</td>
</tr>
</tbody>
</table>
2.9 Status List

The following table lists the status codes the programmer receives from the 78K0R/Kx3.

<table>
<thead>
<tr>
<th>Status Code</th>
<th>Status Description</th>
<th>Status Code</th>
<th>Status Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>04H</td>
<td>Command number error</td>
<td>05H</td>
<td>Parameter error</td>
</tr>
<tr>
<td>06H</td>
<td>Normal acknowledgment</td>
<td>07H</td>
<td>Checksum error</td>
</tr>
<tr>
<td>09H</td>
<td>Negative acknowledgment</td>
<td></td>
<td></td>
</tr>
<tr>
<td>10H</td>
<td>Protect error</td>
<td>11H</td>
<td>MRG10 error</td>
</tr>
<tr>
<td>15H</td>
<td>Negative acknowledgment</td>
<td></td>
<td></td>
</tr>
<tr>
<td>16H</td>
<td>Write error</td>
<td>17H</td>
<td>MRG11 error</td>
</tr>
<tr>
<td>FFH</td>
<td>Processing in progress</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Note** During CSI communication, 1-byte “FFH” may be transmitted, as well as “FFH” as the data frame format.

Reception of a checksum error or NACK is treated as an immediate abnormal end in this manual. When a dedicated programmer is developed, however, the processing may be retried without problem from the wait immediately before transmission of the command that results a checksum error or NACK. In this event, limiting the retry count is recommended for preventing infinite repetition of the retry operation.

Although not listed in the above table, if a time-out error (BUSY time-out or time-out in data frame reception during UART communication) occurs, it is recommended to shutdown the power supply to the 78K0R/Kx3 (refer to 2.6 Shutting Down Target Power Supply) and then connect the power supply again.
CHAPTER 3 BASIC PROGRAMMER OPERATION

Figure 3-1 illustrates the general command execution flow when flash memory rewriting is performed with the programmer.

Figure 3-1. General Command Execution Flow at Flash Memory Rewriting

Remark The Verify command and Checksum command can also be supported.
CHAPTER 4 COMMAND/DATA FRAME FORMAT

The programmer uses the command frame to transmit commands to the 78K0R/Kx3. The 78K0R/Kx3 uses the data frame to transmit write data or verify data to the programmer. A header, footer, data length information, and checksum are appended to each frame to enhance the reliability of the transferred data.

The following shows the format of a command frame and data frame.

**Figure 4-1. Command Frame Format**

<table>
<thead>
<tr>
<th>SOH</th>
<th>LEN</th>
<th>COM</th>
<th>Command information (variable length) (Max. 255 bytes)</th>
<th>SUM</th>
<th>ETX</th>
</tr>
</thead>
<tbody>
<tr>
<td>01H</td>
<td>1 byte</td>
<td>1 byte</td>
<td></td>
<td>1 byte</td>
<td>1 byte</td>
</tr>
</tbody>
</table>

**Figure 4-2. Data Frame Format**

<table>
<thead>
<tr>
<th>STX</th>
<th>LEN</th>
<th>Data (variable length) (Max. 256 bytes)</th>
<th>SUM</th>
<th>ETX or ETB</th>
</tr>
</thead>
<tbody>
<tr>
<td>02H</td>
<td>1 byte</td>
<td></td>
<td>1 byte</td>
<td>1 byte</td>
</tr>
</tbody>
</table>

**Table 4-1. Description of Symbols in Each Frame**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>SOH</td>
<td>01H</td>
<td>Command frame header</td>
</tr>
<tr>
<td>STX</td>
<td>02H</td>
<td>Data frame header</td>
</tr>
<tr>
<td>LEN</td>
<td>–</td>
<td>Data length information (00H indicates 256). Command frame: COM + command information length Data frame: Data field length</td>
</tr>
<tr>
<td>COM</td>
<td>–</td>
<td>Command number</td>
</tr>
<tr>
<td>SUM</td>
<td>–</td>
<td>Checksum data for a frame Obtained by sequentially subtracting all of calculation target data from the initial value (00H) in 1-byte units (borrow is ignored). The calculation targets are as follows. Command frame: LEN + COM + all of command information Data frame: LEN + all of data</td>
</tr>
<tr>
<td>ETB</td>
<td>17H</td>
<td>Footer of data frame other than the last frame</td>
</tr>
<tr>
<td>ETX</td>
<td>03H</td>
<td>Command frame footer, or footer of last data frame</td>
</tr>
</tbody>
</table>

The following shows examples of calculating the checksum (SUM) for a frame.
CHAPTER 4  COMMAND/DATA FRAME FORMAT

[Command frame]
No command information is included in the following example of a Status command frame, so LEN and COM are targets of checksum calculation.

<table>
<thead>
<tr>
<th>SOH</th>
<th>LEN</th>
<th>COM</th>
<th>SUM</th>
<th>ETX</th>
</tr>
</thead>
<tbody>
<tr>
<td>01H</td>
<td>01H</td>
<td>70H</td>
<td>Checksum</td>
<td>03H</td>
</tr>
</tbody>
</table>

Checksum calculation targets

For this command frame, checksum data is obtained as follows.

00H (initial value) \(\rightarrow\) 01H (LEN) \(\rightarrow\) 70H (COM) = 8FH (Borrow ignored. Lower 8 bits only.)

The command frame finally transmitted is as follows.

<table>
<thead>
<tr>
<th>SOH</th>
<th>LEN</th>
<th>COM</th>
<th>SUM</th>
<th>ETX</th>
</tr>
</thead>
<tbody>
<tr>
<td>01H</td>
<td>01H</td>
<td>70H</td>
<td>8FH</td>
<td>03H</td>
</tr>
</tbody>
</table>

[Data frame]
To transmit a data frame as shown below, LEN and D1 to D4 are targets of checksum calculation.

<table>
<thead>
<tr>
<th>STX</th>
<th>LEN</th>
<th>D1</th>
<th>D2</th>
<th>D3</th>
<th>D4</th>
<th>SUM</th>
<th>ETX</th>
</tr>
</thead>
<tbody>
<tr>
<td>02H</td>
<td>04H</td>
<td>FFH</td>
<td>80H</td>
<td>40H</td>
<td>22H</td>
<td>Checksum</td>
<td>03H</td>
</tr>
</tbody>
</table>

Checksum calculation targets

For this data frame, checksum data is obtained as follows.

00H (initial value) \(\rightarrow\) 04H (LEN) \(\rightarrow\) FFH (D1) \(\rightarrow\) 80H (D2) \(\rightarrow\) 40H (D3) \(\rightarrow\) 22H (D4) = 1BH (Borrow ignored. Lower 8 bits only.)

The data frame finally transmitted is as follows.

<table>
<thead>
<tr>
<th>STX</th>
<th>LEN</th>
<th>D1</th>
<th>D2</th>
<th>D3</th>
<th>D4</th>
<th>SUM</th>
<th>ETX</th>
</tr>
</thead>
<tbody>
<tr>
<td>02H</td>
<td>04H</td>
<td>FFH</td>
<td>80H</td>
<td>40H</td>
<td>22H</td>
<td>1BH</td>
<td>03H</td>
</tr>
</tbody>
</table>

When a data frame is received, the checksum data is calculated in the same manner, and the obtained value is used to detect a checksum error by judging whether the value is the same as that stored in the SUM field of the receive data. When a data frame as shown below is received, for example, a checksum error is detected.

<table>
<thead>
<tr>
<th>STX</th>
<th>LEN</th>
<th>D1</th>
<th>D2</th>
<th>D3</th>
<th>D4</th>
<th>SUM</th>
<th>ETX</th>
</tr>
</thead>
<tbody>
<tr>
<td>02H</td>
<td>04H</td>
<td>FFH</td>
<td>80H</td>
<td>40H</td>
<td>22H</td>
<td>1AH</td>
<td>03H</td>
</tr>
</tbody>
</table>

↑ Should be 1BH, if normal
4.1 Command Frame Transmission Processing

For details of the flowchart of processing to transmit command frames, read 6.1 Command Frame Transmission Processing Flowchart.

4.2 Data Frame Transmission Processing

The write data frame (user program), verify data frame (user program), and security data frame (security flag) are transmitted as a data frame.

For details of the flowchart of processing to transmit data frames, read 6.2 Data Frame Transmission Processing Flowchart.

4.3 Data Frame Reception Processing

The status frame, silicon signature data frame, version data frame, and checksum data frame are received as a data frame.

For details of the flowchart of processing to receive data frames, read 6.3 Data Frame Reception Processing Flowchart.
5.1 Status Command

5.1.1 Description

The 78K0R/Kx3 automatically transmits a status frame within a given period of time to report its operation status after issuing various commands, such as write or erase.

After the programmer has issued each command, if the Status command frame cannot be received normally by the 78K0R/Kx3 due to problems based on communication or the like, the status setting will not be performed with the 78K0R/Kx3. As a result, a busy response (FFH), not the status frame, may be received. In such a case, retry each command.

5.1.2 Status frame

Figure 5-1 shows the status frame corresponding to each command.

<table>
<thead>
<tr>
<th>STX</th>
<th>LEN</th>
<th>Data</th>
<th>SUM</th>
<th>ETX</th>
</tr>
</thead>
<tbody>
<tr>
<td>02H</td>
<td>n</td>
<td>ST1</td>
<td></td>
<td>03H</td>
</tr>
</tbody>
</table>

Remarks 1. ST1 to STn: Status #1 to Status #n
2. The length of a status frame varies according to each command (such as write or erase) to be transmitted to the 78K0R/Kx3.
5.2 Reset Command

5.2.1 Description

This command is used to check the establishment of communication between the programmer and the 78K0R/Kx3 after the communication mode is set.

The same baud rate must be set for the programmer and 78K0R/Kx3, however, the 78K0R/Kx3 cannot detect its own baud rate generation clock frequency so the baud rate cannot be set. The 78K0R/Kx3 is enabled to detect the baud rate generation clock frequency by itself, when "00H" is transmitted twice at 9,600 bps from the programmer, and the 78K0R/Kx3 measures the low-level width of "00H" and calculates the average of the two sent signals. The baud rate can consequently be set, which enables synchronous detection in communication.

5.2.2 Command frame and status frame

Figure 5-2 shows the format of a command frame for the Reset command, and Figure 5-3 shows the status frame for the command.

### Figure 5-2. Reset Command Frame (from Programmer to 78K0R/Kx3)

<table>
<thead>
<tr>
<th>SOH</th>
<th>LEN</th>
<th>COM</th>
<th>SUM</th>
<th>ETX</th>
</tr>
</thead>
<tbody>
<tr>
<td>01H</td>
<td>01H</td>
<td>00H (Reset)</td>
<td>Checksum</td>
<td>03H</td>
</tr>
</tbody>
</table>

### Figure 5-3. Status Frame for Reset Command (from 78K0R/Kx3 to Programmer)

<table>
<thead>
<tr>
<th>STX</th>
<th>LEN</th>
<th>Data</th>
<th>SUM</th>
<th>ETX</th>
</tr>
</thead>
<tbody>
<tr>
<td>02H</td>
<td>1</td>
<td>ST1</td>
<td>Checksum</td>
<td>03H</td>
</tr>
</tbody>
</table>

**Remark**  ST1: Synchronization detection result

Read 6.4 Reset Command for details on the flowchart of the processing sequence between the programmer and the 78K0R/Kx3, the flowchart of command processing, and the sample program.
5.3 Baud Rate Set Command

5.3.1 Description
This command is used to change the baud rate for UART communication (9,600 bps by default).

After the Baud Rate Set command has been executed, the Reset command must be executed to check synchronization at the changed baud rate.

The baud rate setting data is represented in 1-byte values.

5.3.2 Command frame and status frame
Figure 5-4 shows the format of a command frame for the Baud Rate Set command, and Figure 5-5 shows the status frame for the command.

**Figure 5-4. Baud Rate Set Command Frame (from Programmer to 78K0R/Kx3)**

<table>
<thead>
<tr>
<th>SOH</th>
<th>LEN</th>
<th>COM</th>
<th>Command Information&lt;sup&gt;Note&lt;/sup&gt;</th>
<th>SUM</th>
<th>ETX</th>
</tr>
</thead>
<tbody>
<tr>
<td>01H</td>
<td>05H</td>
<td>9AH</td>
<td>D01</td>
<td>D02H</td>
<td>D02L</td>
</tr>
</tbody>
</table>

**Note** For details of the command information setting, refer to Table 5-1. If data other than in Table 5-1 is set, a time-out error will occur.

If a time-out error has occurred, execute a hardware reset and re-set the flash memory programming mode.

**Remark**
- D01: Synchronization correction mode
- D02H, D02L: Baud rate setting
- D03: Noise filter setting

**Table 5-1. Command Information Setting**

<table>
<thead>
<tr>
<th>Synchronization Correction Mode</th>
<th>D01</th>
<th>D02H</th>
<th>D02L</th>
<th>D03</th>
</tr>
</thead>
<tbody>
<tr>
<td>Microcontroller correction mode</td>
<td>00H</td>
<td>Fixed to 00H</td>
<td>Fixed to 0AH (115,200 bps)</td>
<td>Noise filter 00H: Off 01H: On</td>
</tr>
<tr>
<td>Programmer correction mode</td>
<td>01H</td>
<td>Note</td>
<td>Note</td>
<td></td>
</tr>
</tbody>
</table>

**Note** Substitute the k value calculated by the expression below for D02H/D02L in hexadecimal. Make sure that the k value is greater than 0003H.

\[ k = \left(8 \times 10^5 \times E\right) / \text{BAUD RATE} \]

E: READY pulse (9,600 bps) error of the 78K0R during flash lead-in

**Example 1**: 0% error for READY pulse (low-level 9 bits @ 9,600 bps) length

(READY pulse = 937.5 μs)

When set to 250,000 bps

\[ E = 1.00 \]

\[ k = 0020H \]

D02H = 00H

D02L = 20H
Example 2: +5% error for READY pulse (low-level 9 bits @ 9,600 bps) length
(READY pulse = 984.375 μs)
When set to 250,000 bps
E = 1.05
k = 0021H
D02H = 00H
D02L = 21H

Example 3: −5% error for READY pulse (low-level 9 bits @ 9,600 bps) length
(READY pulse = 890.625 μs)
When set to 250,000 bps
E = 0.95
k = 001EH
D02H = 00H
D02L = 1EH

Figure 5-5. Status Frame for Baud Rate Set Command (from 78K0R/Kx3 to Programmer)

<table>
<thead>
<tr>
<th>STX</th>
<th>LEN</th>
<th>Data</th>
<th>SUM</th>
<th>ETX</th>
</tr>
</thead>
<tbody>
<tr>
<td>02H</td>
<td>01H</td>
<td>ST1</td>
<td>checksum</td>
<td>03H</td>
</tr>
</tbody>
</table>

Remark ST1: Synchronization detection result

Read 6.5 Baud Rate Set Command for details on the flowchart of the processing sequence between the programmer and the 78K0R/Kx3, the flowchart of command processing, and the sample program.
5.4 Chip Erase Command

5.4.1 Description
This command is used to erase the entire contents of the flash memory. In addition, all of the information that is set by security setting processing can be initialized by chip erase processing, as long as erasure is not prohibited by the security setting (see 5.12 Security Set Command).

5.4.2 Command frame and status frame
Figure 5-6 shows the format of a command frame for the Chip Erase command, and Figure 5-7 shows the status frame for the command.

**Figure 5-6. Chip Erase Command Frame (from Programmer to 78K0R/Kx3)**

<table>
<thead>
<tr>
<th>SOH</th>
<th>LEN</th>
<th>COM</th>
<th>SUM</th>
<th>ETX</th>
</tr>
</thead>
<tbody>
<tr>
<td>01H</td>
<td>01H</td>
<td>20H</td>
<td>Checksum</td>
<td>03H</td>
</tr>
</tbody>
</table>

*(Chip Erase)*

**Figure 5-7. Status Frame for Chip Erase Command (from 78K0R/Kx3 to Programmer)**

<table>
<thead>
<tr>
<th>STX</th>
<th>LEN</th>
<th>Data</th>
<th>SUM</th>
<th>ETX</th>
</tr>
</thead>
<tbody>
<tr>
<td>02H</td>
<td>01H</td>
<td>ST1</td>
<td>Checksum</td>
<td>03H</td>
</tr>
</tbody>
</table>

**Remark**  ST1: Chip erase result

Read 6.6 Chip Erase Command for details on the flowchart of the processing sequence between the programmer and the 78K0R/Kx3, the flowchart of command processing, and the sample program.
5.5 Block Erase Command

5.5.1 Description
This command is used to erase the content of flash memory of the block with the specified number. A block can be specified with the first address of the block where erasing starts and the last address where erasing ends. Successive multiple blocks can be specified.

Erasing cannot be performed, however, if erasing is prohibited due to the security setting (see 5.12 Security Set Command).

5.5.2 Command frame and status frame
Figure 5-8 shows the format of a command frame for the Block Erase command, and Figure 5-9 shows the status frame for the command.

Figure 5-8. Block Erase Command Frame (from Programmer to 78K0R/Kx3)

<table>
<thead>
<tr>
<th>SOH</th>
<th>LEN</th>
<th>COM</th>
<th>Command Information</th>
<th>SUM</th>
<th>ETX</th>
</tr>
</thead>
<tbody>
<tr>
<td>01H</td>
<td>07H</td>
<td>22H</td>
<td>(Block Erase)</td>
<td>SAHSAMSALEHAMEAL Checksum</td>
<td>03H</td>
</tr>
</tbody>
</table>

Remark  SAH, SAM, SAL: Block erase start address (start address of any block)
SAH: Start address, high (bits 23 to 16)
SAM: Start address, middle (bits 15 to 8)
SAL: Start address, low (bits 7 to 0)
EAH, EAM, EAL: Block erase end address (last address of any block)
EAH: End address, high (bits 23 to 16)
EAM: End address, middle (bits 15 to 8)
EAL: End address, low (bits 7 to 0)

Figure 5-9. Status Frame for Block Erase Command (from 78K0R/Kx3 to Programmer)

<table>
<thead>
<tr>
<th>STX</th>
<th>LEN</th>
<th>Data</th>
<th>SUM</th>
<th>ETX</th>
</tr>
</thead>
<tbody>
<tr>
<td>02H</td>
<td>01H</td>
<td>ST1</td>
<td>Checksum</td>
<td>03H</td>
</tr>
</tbody>
</table>

Remark  ST1: Block erase result

Read 6.7 Block Erase Command for details on the flowchart of the processing sequence between the programmer and the 78K0R/Kx3, the flowchart of command processing, and the sample program.
5.6 Programming Command

5.6.1 Description
This command is used to write the user program to the flash memory by transmitting write data after having transmitted the write start address and the write end address. Internal verification is then executed after the last data has been transmitted and writing has been completed.

The write start/end address can be set only in the block start/end address units.

If both of the status frames (ST1 and ST2) after the last data transmission indicate ACK, the 78K0R/Kx3 firmware automatically executes internal verify. Therefore, the Status command for this internal verify must be transmitted.

5.6.2 Command frame and status frame
Figure 5-10 shows the format of a command frame for the Programming command, and Figure 5-11 shows the status frame for the command.

![Figure 5-10. Programming Command Frame (from Programmer to 78K0R/Kx3)](image)

<table>
<thead>
<tr>
<th>SOH</th>
<th>LEN</th>
<th>COM</th>
<th>Command Information</th>
<th>SUM</th>
<th>ETX</th>
</tr>
</thead>
<tbody>
<tr>
<td>01H</td>
<td>07H</td>
<td>40H</td>
<td>(Programming)</td>
<td>SAH</td>
<td>EAH</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>SAM</td>
<td>EAM</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>SAL</td>
<td>EAL</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Checksum</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>03H</td>
<td></td>
</tr>
</tbody>
</table>

Remark  SAH, SAM, SAL: Write start addresses  EAH, EAM, EAL: Write end addresses

![Figure 5-11. Status Frame for Programming Command (from 78K0R/Kx3 to Programmer)](image)

<table>
<thead>
<tr>
<th>STX</th>
<th>LEN</th>
<th>Data</th>
<th>SUM</th>
<th>ETX</th>
</tr>
</thead>
<tbody>
<tr>
<td>02H</td>
<td>01H</td>
<td>ST1 (a)</td>
<td>Checksum</td>
<td>03H</td>
</tr>
</tbody>
</table>

Remark  ST1 (a): Command reception result

5.6.3 Data frame and status frame
Figure 5-12 shows the format of a frame that includes data to be written, and Figure 5-13 shows the status frame for the data.

![Figure 5-12. Data Frame to Be Written (from Programmer to 78K0R/Kx3)](image)

<table>
<thead>
<tr>
<th>STX</th>
<th>LEN</th>
<th>Data</th>
<th>SUM</th>
<th>ETX/ETB</th>
</tr>
</thead>
<tbody>
<tr>
<td>02H</td>
<td>00H</td>
<td>00H to FFH (00H = 256)</td>
<td>Checksum</td>
<td>03H/17H</td>
</tr>
</tbody>
</table>

Remark  Write Data: User program to be written

![Figure 5-13. Status Frame for Data Frame (from 78K0R/Kx3 to Programmer)](image)

<table>
<thead>
<tr>
<th>STX</th>
<th>LEN</th>
<th>Data</th>
<th>SUM</th>
<th>ETX</th>
</tr>
</thead>
<tbody>
<tr>
<td>02H</td>
<td>02H</td>
<td>ST1 (b)</td>
<td>ST2 (b)</td>
<td>Checksum</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>03H</td>
</tr>
</tbody>
</table>

Remark  ST1 (b): Data reception check result  ST2 (b): Write result
5.6.4 Completion of transferring all data and status frame

Figure 5-14 shows the status frame after transfer of all data is completed.

**Figure 5-14. Status Frame After Completion of Transferring All Data (from 78K0R/Kx3 to Programmer)**

<table>
<thead>
<tr>
<th>STX</th>
<th>LEN</th>
<th>Data</th>
<th>SUM</th>
<th>ETX</th>
</tr>
</thead>
<tbody>
<tr>
<td>02H</td>
<td>01H</td>
<td>ST1 (c)</td>
<td>Checksum</td>
<td>03H</td>
</tr>
</tbody>
</table>

**Remark**  ST1 (c): Internal verify result

Read **6.8 Programming Command** for details on the flowchart of the processing sequence between the programmer and the 78K0R/Kx3, the flowchart of command processing, and the sample program.
5.7 Verify Command

5.7.1 Description
This command is used to compare the data transmitted from the programmer with the data read from the
78K0R/Kx3 (read level) in the specified address range, and check whether they match.
The verify start/end address can be set only in the block start/end address units.

5.7.2 Command frame and status frame
Figure 5-15 shows the format of a command frame for the Verify command, and Figure 5-16 shows the status
frame for the command.

Figure 5-15. Verify Command Frame (from Programmer to 78K0R/Kx3)

<table>
<thead>
<tr>
<th>SOH</th>
<th>LEN</th>
<th>COM</th>
<th>Command Information</th>
<th>SUM</th>
<th>ETX</th>
</tr>
</thead>
<tbody>
<tr>
<td>01H</td>
<td>07H</td>
<td>13H</td>
<td>SAH, SAM, SAL, EAH, EAM, EAL</td>
<td>03H</td>
<td></td>
</tr>
</tbody>
</table>

Remark SAH, SAM, SAL: Verify start addresses
EAH, EAM, EAL: Verify end addresses

Figure 5-16. Status Frame for Verify Command (from 78K0R/Kx3 to Programmer)

<table>
<thead>
<tr>
<th>STX</th>
<th>LEN</th>
<th>Data</th>
<th>SUM</th>
<th>ETX</th>
</tr>
</thead>
<tbody>
<tr>
<td>02H</td>
<td>01H</td>
<td>ST1 (a)</td>
<td>Checksum</td>
<td>03H</td>
</tr>
</tbody>
</table>

Remark ST1 (a): Command reception result

5.7.3 Data frame and status frame
Figure 5-17 shows the format of a frame that includes data to be verified, and Figure 5-18 shows the status frame
for the data.

Figure 5-17. Data Frame of Data to Be Verified (from Programmer to 78K0R/Kx3)

<table>
<thead>
<tr>
<th>STX</th>
<th>LEN</th>
<th>Data</th>
<th>SUM</th>
<th>ETX/ETB</th>
</tr>
</thead>
<tbody>
<tr>
<td>02H</td>
<td>00H to FFH (00H = 256)</td>
<td>Verify Data</td>
<td>Checksum</td>
<td>03H/17H</td>
</tr>
</tbody>
</table>

Remark Verify Data: User program to be verified
Figure 5-18. Status Frame for Data Frame (from 78K0R/Kx3 to Programmer)

<table>
<thead>
<tr>
<th>STX</th>
<th>LEN</th>
<th>Data</th>
<th>SUM</th>
<th>ETX</th>
</tr>
</thead>
<tbody>
<tr>
<td>02H</td>
<td>02H</td>
<td>ST1 (b)</td>
<td>ST2 (b)</td>
<td>03H</td>
</tr>
</tbody>
</table>

**Remark**  
ST1 (b): Data reception check result  
ST2 (b): Verify result

**Note**  
Even if a verify error occurs in the specified address range, ACK is always returned as the verify result. The status of all verify errors are reflected in the verify result for the last data. Therefore, the occurrence of verify errors can be checked only when all the verify processing for the specified address range is completed.

Read **6.9 Verify Command** for details on the flowchart of the processing sequence between the programmer and the 78K0R/Kx3, the flowchart of command processing, and the sample program.
5.8  Block Blank Check Command

5.8.1  Description
This command is used to check if a block in the flash memory, with a specified block number, is blank (erased state).

A block can be specified with the start address of the blank check start block and the last address of the blank check end block. Successive multiple blocks can be specified.

5.8.2  Command frame and status frame
Figure 5-19 shows the format of a command frame for the Block Blank Check command, and Figure 5-20 shows the status frame for the command.

**Figure 5-19. Block Blank Check Command Frame (from Programmer to 78K0R/Kx3)**

<table>
<thead>
<tr>
<th>SOH</th>
<th>LEN</th>
<th>COM</th>
<th>Command Information</th>
<th>SUM</th>
<th>ETX</th>
</tr>
</thead>
<tbody>
<tr>
<td>01H</td>
<td>08H</td>
<td>32H</td>
<td>SAH</td>
<td>SAM</td>
<td>SAL</td>
</tr>
</tbody>
</table>

**Remark**
SAH, SAM, SAL: Block blank check start address (start address of any block)
SAH: Start address, high (bits 23 to 16)
SAM: Start address, middle (bits 15 to 8)
SAL: Start address, low (bits 7 to 0)
EAH, EAM, EAL: Block blank check end address (last address of any block)
EAH: End address, high (bits 23 to 16)
EAM: End address, middle (bits 15 to 8)
EAL: End address, low (bits 7 to 0)
D01: 00H: When performing a block blank check for a single block
      01H: When performing a block blank check for the complete area before erasing the chip

**Figure 5-20. Status Frame for Block Blank Check Command (from 78K0R/Kx3 to Programmer)**

<table>
<thead>
<tr>
<th>STX</th>
<th>LEN</th>
<th>Data</th>
<th>SUM</th>
<th>ETX</th>
</tr>
</thead>
<tbody>
<tr>
<td>02H</td>
<td>01H</td>
<td>ST1</td>
<td>Checksum</td>
<td>03H</td>
</tr>
</tbody>
</table>

**Remark**
ST1: Block blank check result

Read 6.10 Block Blank Check Command for details on the flowchart of the processing sequence between the programmer and the 78K0R/Kx3, the flowchart of command processing, and the sample program.
5.9 Silicon Signature Command

5.9.1 Description
This command is used to read information such as the write protocol information (silicon signature) of the device and security flag information.

If the programmer supports a programming protocol that is not supported in the 78K0R/Kx3, for example, execute this command to select an appropriate protocol in accordance with the values of the second and third bytes.

5.9.2 Command frame and status frame
Figure 5-21 shows the format of a command frame for the Silicon Signature command, and Figure 5-22 shows the status frame for the command.

![Figure 5-21. Silicon Signature Command Frame (from Programmer to 78K0R/Kx3)](image)

<table>
<thead>
<tr>
<th>SOH</th>
<th>LEN</th>
<th>COM</th>
<th>SUM</th>
<th>ETX</th>
</tr>
</thead>
<tbody>
<tr>
<td>01H</td>
<td>01H</td>
<td>C0H</td>
<td>Checksum</td>
<td>03H</td>
</tr>
</tbody>
</table>

(Silicon Signature)

![Figure 5-22. Status Frame for Silicon Signature Command (from 78K0R/Kx3 to Programmer)](image)

<table>
<thead>
<tr>
<th>STX</th>
<th>LEN</th>
<th>Data</th>
<th>SUM</th>
<th>ETX</th>
</tr>
</thead>
<tbody>
<tr>
<td>02H</td>
<td>01H</td>
<td>ST1</td>
<td>Checksum</td>
<td>03H</td>
</tr>
</tbody>
</table>

Remark ST1: Command reception result
5.9.3 Silicon signature data frame

Figure 5-23 shows the format of a frame that includes silicon signature data.

Figure 5-23. Silicon Signature Data Frame (from 78K0R/Kx3 to Programmer)

<table>
<thead>
<tr>
<th>STX</th>
<th>LEN</th>
<th>Data</th>
</tr>
</thead>
<tbody>
<tr>
<td>02H</td>
<td>n</td>
<td>VEN  MET  MSC  DEC1  DEC2  UAE(3)  DEV(10)</td>
</tr>
</tbody>
</table>

Data (continued) | SUM | ETX |
<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>SCF  BOT  FSWSH  FSWSL  FSWEH  FSWEL</td>
<td>checksum</td>
<td>03H</td>
</tr>
</tbody>
</table>

Remarks 1.

1. n (LEN): Data length
   VEN: Vendor code (NEC: 10H)
   MET: Macro extension code
   MSC: Macro function code
   DEC1: Device extension code 1
   DEC2: Device extension code 2
   UAE: User flash ROM last address (3 bytes)
   DEV: Device name (10 bytes)
   SCF: Security flag information
   BOT: Boot block number
   FSWSH: Higher 8-bit side of flash shield window (FSW) start block
   FSWSL: Lower 8-bit side of flash shield window (FSW) start block
   FSWEH: Higher 8-bit side of flash shield window (FSW) end block
   FSWEL: Lower 8-bit side of flash shield window (FSW) end block

2. For the vendor code (VEN), extension code (MET), function code (MSC), device extension code 1 (DEC1), and device extension code 2 (DEC2), the lower 7 bits are used as data entity, and the highest bit is used as an odd parity. The following shows an example.
### Table 5-2. Example of Silicon Signature Data

<table>
<thead>
<tr>
<th>Field</th>
<th>Content</th>
<th>Length (Byte)</th>
<th>Example of Silicon Signature Data</th>
<th>Actual Value</th>
<th>Parity</th>
</tr>
</thead>
<tbody>
<tr>
<td>VEN</td>
<td>Vendor code (NEC)</td>
<td>1</td>
<td>10H (00010000B )</td>
<td>10H</td>
<td>Added</td>
</tr>
<tr>
<td>MET</td>
<td>Macro extension code</td>
<td>1</td>
<td>7FH (01111111B )</td>
<td>7FH</td>
<td>Added</td>
</tr>
<tr>
<td>MSC</td>
<td>Macro function code</td>
<td>1</td>
<td>04H (01000000B )</td>
<td>04H</td>
<td>Added</td>
</tr>
<tr>
<td>DEC1</td>
<td>Device extension code 1</td>
<td>1</td>
<td>DCH (11011100B )</td>
<td>DCH</td>
<td>Added</td>
</tr>
<tr>
<td>DEC2</td>
<td>Device extension code 2</td>
<td>1</td>
<td>FDH (11111101B )</td>
<td>FDH</td>
<td>Added</td>
</tr>
<tr>
<td>UAE</td>
<td>User flash ROM last address</td>
<td>3</td>
<td>FFH (11111111B )</td>
<td>00FFFFH</td>
<td>Not added</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>00H (00000000B )</td>
<td></td>
<td></td>
</tr>
<tr>
<td>DEV</td>
<td>Device name</td>
<td>10</td>
<td>44H (01000100B) = 'D'</td>
<td>'D'</td>
<td>Not added</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>37H (00110111B) = '7'</td>
<td>'7'</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>38H (00111000B) = '8'</td>
<td>'8'</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>46H (01001111B) = 'F'</td>
<td>'F'</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>31H (00110001B) = '1'</td>
<td>'1'</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>31H (00110001B) = '1'</td>
<td>'1'</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>34H (00110100B) = '4'</td>
<td>'4'</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>32H (00110010B) = '2'</td>
<td>'2'</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>20H (00100000B) = ' '</td>
<td>' '</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>20H (00100000B) = ' '</td>
<td>' '</td>
<td></td>
</tr>
<tr>
<td>SCF</td>
<td>Security flag information</td>
<td>1</td>
<td>Any</td>
<td>Same as left column</td>
<td>Not added</td>
</tr>
<tr>
<td>BOT</td>
<td>Boot block number (fixed)</td>
<td>1</td>
<td>01H (00000001B)</td>
<td>01H</td>
<td>Not added</td>
</tr>
<tr>
<td>FSWS(H)</td>
<td>Higher 8-bit side of flash shield window start block</td>
<td>1</td>
<td>Any</td>
<td>Same as left column</td>
<td>Not added</td>
</tr>
<tr>
<td>FSWS(L)</td>
<td>Lower 8-bit side of flash shield window start block</td>
<td>1</td>
<td>Any</td>
<td>Same as left column</td>
<td>Not added</td>
</tr>
<tr>
<td>FSWE(H)</td>
<td>Higher 8-bit side of flash shield window end block</td>
<td>1</td>
<td>Any</td>
<td>Same as left column</td>
<td>Not added</td>
</tr>
<tr>
<td>FSWE(L)</td>
<td>Lower 8-bit side of flash shield window end block</td>
<td>1</td>
<td>Any</td>
<td>Same as left column</td>
<td>Not added</td>
</tr>
</tbody>
</table>

Read 6.11 Silicon Signature Command for details on the flowchart of the processing sequence between the programmer and the 78K0R/Kx3, the flowchart of command processing, and the sample program.
5.9.4 78K0R/Kx3 silicon signature list

Table 5-3. 78K0R/Kx3 Silicon Signature Data List

<table>
<thead>
<tr>
<th>Item</th>
<th>Description</th>
<th>Length (Byte)</th>
<th>Data (Hex)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vendor code</td>
<td>NEC</td>
<td>1</td>
<td>10</td>
</tr>
<tr>
<td>Extension code</td>
<td>Extension code</td>
<td>1</td>
<td>7F</td>
</tr>
<tr>
<td>Function code</td>
<td>Function information</td>
<td>1</td>
<td>04</td>
</tr>
<tr>
<td>Device information</td>
<td>Device information</td>
<td>2</td>
<td>DC</td>
</tr>
<tr>
<td>Internal flash ROM last address</td>
<td>Transmitted from lower bytes of address</td>
<td>3</td>
<td>Note 1</td>
</tr>
<tr>
<td>Device name (μPD)</td>
<td>78F1142/78F1152/78F1162</td>
<td>10</td>
<td>Note 2</td>
</tr>
<tr>
<td></td>
<td>78F1143/78F1153/78F1163</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>78F1144/78F1154/78F1164</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>78F1145/78F1155/78F1165</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>78F1146/78F1156/78F1166</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>78F1167/78F1168</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Security information</td>
<td>Security information</td>
<td>1</td>
<td>Any</td>
</tr>
<tr>
<td>Boot block number</td>
<td>The last block number of the boot cluster that is currently selected</td>
<td>1</td>
<td>01</td>
</tr>
<tr>
<td>FSW block number</td>
<td>FSW information</td>
<td>4</td>
<td>Any</td>
</tr>
</tbody>
</table>

**Note 1.** List of internal flash ROM last addresses

<table>
<thead>
<tr>
<th>Item</th>
<th>Description</th>
<th>Length (Byte)</th>
<th>Data (Hex)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Internal flash ROM last address</td>
<td>64 KB (00FFFFH)</td>
<td>3</td>
<td>FFFF00</td>
</tr>
<tr>
<td></td>
<td>96 KB (017FFFH)</td>
<td></td>
<td>FFF701</td>
</tr>
<tr>
<td></td>
<td>128 KB (01FFFFH)</td>
<td></td>
<td>FFFF01</td>
</tr>
<tr>
<td></td>
<td>192 KB (02FFFFH)</td>
<td></td>
<td>FFFF02</td>
</tr>
<tr>
<td></td>
<td>256 KB (03FFFFH)</td>
<td></td>
<td>FFFF03</td>
</tr>
<tr>
<td></td>
<td>384 KB (05FFFFH)</td>
<td></td>
<td>FFFF05</td>
</tr>
<tr>
<td></td>
<td>512 KB (07FFFFH)</td>
<td></td>
<td>FFFF07</td>
</tr>
</tbody>
</table>

(Note 2 is on the next page.)
Note 2. The device names are listed below.

<table>
<thead>
<tr>
<th>Device name list (1/4)</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Item</strong></td>
</tr>
</tbody>
</table>
| Device name | D78F1142 | 10 | 44 = 'D'  
37 = '7'  
38 = '8'  
46 = 'F'  
31 = '1'  
31 = '1'  
34 = '4'  
32 = '2'  
20 = ' ' |
|          | D78F1143 |    | 44 = 'D'  
37 = '7'  
38 = '8'  
46 = 'F'  
31 = '1'  
31 = '1'  
34 = '4'  
33 = '3'  
20 = ' ' |
|          | D78F1144 |    | 44 = 'D'  
37 = '7'  
38 = '8'  
46 = 'F'  
31 = '1'  
31 = '1'  
34 = '4'  
34 = '4'  
20 = ' ' |
|          | D78F1145 |    | 44 = 'D'  
37 = '7'  
38 = '8'  
46 = 'F'  
31 = '1'  
31 = '1'  
34 = '4'  
35 = '5'  
20 = ' ' |
|          | D78F1146 |    | 44 = 'D'  
37 = '7'  
38 = '8'  
46 = 'F'  
31 = '1'  
31 = '1'  
34 = '4'  
36 = '6'  
20 = ' ' |
## Device name list (2/4)

<table>
<thead>
<tr>
<th>Item</th>
<th>Description</th>
<th>Length (Byte)</th>
<th>Actual Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Device name</td>
<td>D78F1152</td>
<td>10</td>
<td>44 = 'D'</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>37 = '7'</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>38 = '8'</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>46 = 'F'</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>31 = '1'</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>31 = '1'</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>35 = '5'</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>32 = '2'</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>20 = '.'</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>20 = '.'</td>
</tr>
<tr>
<td>D78F1153</td>
<td></td>
<td></td>
<td>44 = 'D'</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>37 = '7'</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>38 = '8'</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>46 = 'F'</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>31 = '1'</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>31 = '1'</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>35 = '5'</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>33 = '3'</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>20 = '.'</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>20 = '.'</td>
</tr>
<tr>
<td>D78F1154</td>
<td></td>
<td></td>
<td>44 = 'D'</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>37 = '7'</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>38 = '8'</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>46 = 'F'</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>31 = '1'</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>31 = '1'</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>35 = '5'</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>34 = '4'</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>20 = '.'</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>20 = '.'</td>
</tr>
<tr>
<td>D78F1155</td>
<td></td>
<td></td>
<td>44 = 'D'</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>37 = '7'</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>38 = '8'</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>46 = 'F'</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>31 = '1'</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>31 = '1'</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>35 = '5'</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>35 = '5'</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>20 = '.'</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>20 = '.'</td>
</tr>
<tr>
<td>D78F1156</td>
<td></td>
<td></td>
<td>44 = 'D'</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>37 = '7'</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>38 = '8'</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>46 = 'F'</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>31 = '1'</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>31 = '1'</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>35 = '5'</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>36 = '6'</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>20 = '.'</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>20 = '.'</td>
</tr>
</tbody>
</table>
### Device name list (3/4)

<table>
<thead>
<tr>
<th>Item</th>
<th>Description</th>
<th>Length (Byte)</th>
<th>Actual Value</th>
</tr>
</thead>
</table>
| Device name | D78F1162    | 10            | 44 = ‘D’  
37 = ‘7’  
38 = ‘8’  
46 = ‘F’  
31 = ‘1’  
31 = ‘1’  
36 = ‘6’  
32 = ‘2’  
20 = ‘ ’  
20 = ‘ ’ |
|           | D78F1163    |               | 44 = ‘D’  
37 = ‘7’  
38 = ‘8’  
46 = ‘F’  
31 = ‘1’  
31 = ‘1’  
36 = ‘6’  
33 = ‘3’  
20 = ‘ ’  
20 = ‘ ’ |
|           | D78F1164    |               | 44 = ‘D’  
37 = ‘7’  
38 = ‘8’  
46 = ‘F’  
31 = ‘1’  
31 = ‘1’  
36 = ‘6’  
34 = ‘4’  
20 = ‘ ’  
20 = ‘ ’ |
|           | D78F1165    |               | 44 = ‘D’  
37 = ‘7’  
38 = ‘8’  
46 = ‘F’  
31 = ‘1’  
31 = ‘1’  
36 = ‘6’  
35 = ‘5’  
20 = ‘ ’  
20 = ‘ ’ |
|           | D78F1166    |               | 44 = ‘D’  
37 = ‘7’  
38 = ‘8’  
46 = ‘F’  
31 = ‘1’  
31 = ‘1’  
36 = ‘6’  
36 = ‘6’  
20 = ‘ ’  
20 = ‘ ’ |
### Device name list (4/4)

<table>
<thead>
<tr>
<th>Item</th>
<th>Description</th>
<th>Length (Byte)</th>
<th>Actual Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Device name</td>
<td>D78F1167</td>
<td>10</td>
<td>44 = 'D'</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>37 = '7'</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>38 = '8'</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>46 = 'F'</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>31 = '1'</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>31 = '1'</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>36 = '6'</td>
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<tr>
<td></td>
<td></td>
<td></td>
<td>37 = '7'</td>
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<tr>
<td></td>
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<td>20 = ''</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>20 = ''</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Device name</th>
<th>D78F1168</th>
<th>10</th>
<th>44 = 'D'</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>37 = '7'</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>38 = '8'</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>46 = 'F'</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>31 = '1'</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>31 = '1'</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>36 = '6'</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>38 = '8'</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>20 = ''</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>20 = ''</td>
</tr>
</tbody>
</table>
5.10 Version Get Command

5.10.1 Description
This command is used to acquire information on the 78K0R/Kx3 device version and firmware version.
The device version value is fixed to 00H.
Use this command when the programming parameters must be changed in accordance with the 78K0R/Kx3 firmware version.

**Caution**  The firmware version may be updated during firmware update that does not affect the change of flash programming parameters (at this time, update of the firmware version is not reported).

**Example**  Firmware version and reprogramming parameters

<table>
<thead>
<tr>
<th>Firmware version</th>
<th>Programming parameters</th>
</tr>
</thead>
<tbody>
<tr>
<td>V1.00</td>
<td>Parameter A</td>
</tr>
<tr>
<td>V2.00</td>
<td>Parameter B</td>
</tr>
<tr>
<td>V3.00</td>
<td></td>
</tr>
</tbody>
</table>

5.10.2 Command frame and status frame

Figure 5-24 shows the format of a command frame for the Version Get command, and Figure 5-25 shows the status frame for the command.

**Figure 5-24. Version Get Command Frame (from Programmer to 78K0R/Kx3)**

<table>
<thead>
<tr>
<th>SOH</th>
<th>LEN</th>
<th>COM</th>
<th>SUM</th>
<th>ETX</th>
</tr>
</thead>
<tbody>
<tr>
<td>01H</td>
<td>01H</td>
<td>C5H</td>
<td>Checksum</td>
<td>03H</td>
</tr>
</tbody>
</table>

**Figure 5-25. Status Frame for Version Get Command (from 78K0R/Kx3 to Programmer)**

<table>
<thead>
<tr>
<th>STX</th>
<th>LEN</th>
<th>Data</th>
<th>SUM</th>
<th>ETX</th>
</tr>
</thead>
<tbody>
<tr>
<td>02H</td>
<td>01H</td>
<td>ST1</td>
<td>Checksum</td>
<td>03H</td>
</tr>
</tbody>
</table>

**Remark**  ST1: Command reception result
5.10.3 Version data frame

Figure 5-26 shows the data frame of version data.

Figure 5-26. Version Data Frame (from 78K0R/Kx3 to Programmer)

<table>
<thead>
<tr>
<th>STX</th>
<th>LEN</th>
<th>Data</th>
<th>SUM</th>
<th>ETX</th>
</tr>
</thead>
<tbody>
<tr>
<td>02H</td>
<td>06H</td>
<td>DV1</td>
<td>DV2</td>
<td>DV3</td>
</tr>
<tr>
<td></td>
<td></td>
<td>FV1</td>
<td>FV2</td>
<td>FV3</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Checksum</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>03H</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Remark
DV1: Integer of device version (fixed to 00H)
DV2: First decimal place of device version (fixed to 00H)
DV3: Second decimal place of device version (fixed to 00H)
FV1: Integer of firmware version
FV2: First decimal place of firmware version
FV3: Second decimal place of firmware version

Read 6.12 Version Get Command for details on the flowchart of the processing sequence between the programmer and the 78K0R/Kx3, the flowchart of command processing, and the sample program.
5.11 Checksum Command

5.11.1 Description

This command is used to acquire the checksum data in the specified area. For the checksum calculation start/end address, specify a fixed address in block units (2 KB) starting from the top of the flash memory. Checksum data is obtained by sequentially subtracting data in the specified address range from the initial value (0000H) in 1-byte units.

5.11.2 Command frame and status frame

Figure 5-27 shows the format of a command frame for the Checksum command, and Figure 5-28 shows the status frame for the command.

Figure 5-27. Checksum Command Frame (from Programmer to 78K0R/Kx3)

<table>
<thead>
<tr>
<th>SOH</th>
<th>LEN</th>
<th>COM</th>
<th>Command Information</th>
<th>SUM</th>
<th>ETX</th>
</tr>
</thead>
<tbody>
<tr>
<td>01H</td>
<td>07H</td>
<td>B0H (Checksum)</td>
<td>SAH</td>
<td>SAM</td>
<td>SAL</td>
</tr>
</tbody>
</table>

Remark  SAH, SAM, SAL: Checksum calculation start addresses
EAH, EAM, EAL: Checksum calculation end addresses

Figure 5-28. Status Frame for Checksum Command (from 78K0R/Kx3 to Programmer)

<table>
<thead>
<tr>
<th>STX</th>
<th>LEN</th>
<th>Data</th>
<th>SUM</th>
<th>ETX</th>
</tr>
</thead>
<tbody>
<tr>
<td>02H</td>
<td>01H</td>
<td>ST1</td>
<td>Checksum</td>
<td>03H</td>
</tr>
</tbody>
</table>

Remark  ST1: Command reception result

5.11.3 Checksum data frame

Figure 5-29 shows the format of a frame that includes checksum data.

Figure 5-29. Checksum Data Frame (from 78K0R/Kx3 to Programmer)

<table>
<thead>
<tr>
<th>STX</th>
<th>LEN</th>
<th>Data</th>
<th>SUM</th>
<th>ETX</th>
</tr>
</thead>
<tbody>
<tr>
<td>02H</td>
<td>02H</td>
<td>CK1</td>
<td>CK2</td>
<td>Checksum</td>
</tr>
</tbody>
</table>

Remark  CK1: Higher 8 bits of checksum data
CK2: Lower 8 bits of checksum data

Read 6.13 Checksum Command for details on the flowchart of the processing sequence between the programmer and the 78K0R/Kx3, the flowchart of command processing, and the sample program.
5.12 Security Set Command

5.12.1 Description
This command is used to perform security settings (enabling/disabling of write, block erase, chip erase, and boot block rewriting, and setting of flash shield window start/end block number). By performing these settings with this command, rewriting of the flash memory by an unauthorized party can be restricted and the rewrite area for self programming can be specified.

Caution Even after the security setting, additional setting of changing from enable to disable can be performed; however, changing from disable to enable is not possible. If an attempt is made to perform such a setting, a protect error (10H) will occur. If such setting is required, all of the security flags must first be initialized by executing the Chip Erase command (the Block Erase command cannot be used to initialize the security flags). If chip erase or boot block rewrite has been disabled, however, chip erase itself will be impossible, so the settings cannot be erased from the programmer. Re-confirmation of security setting execution is therefore recommended before disabling chip erase, due to this programmer specification.

5.12.2 Command frame and status frame
Figure 5-30 shows the format of a command frame for the Security Set command, and Figure 5-31 shows the status frame for the command.

Figure 5-30. Security Set Command Frame (from Programmer to 78K0R/Kx3)

<table>
<thead>
<tr>
<th>SOH</th>
<th>LEN</th>
<th>COM</th>
<th>Command Information</th>
<th>SUM</th>
<th>ETX</th>
</tr>
</thead>
<tbody>
<tr>
<td>01H</td>
<td>03H</td>
<td>A0H (Security Set)</td>
<td>00H (fixed)</td>
<td>00H (fixed)</td>
<td>Checksum</td>
</tr>
</tbody>
</table>

Figure 5-31. Status Frame for Security Set Command (from 78K0R/Kx3 to Programmer)

<table>
<thead>
<tr>
<th>STX</th>
<th>LEN</th>
<th>Data</th>
<th>SUM</th>
<th>ETX</th>
</tr>
</thead>
<tbody>
<tr>
<td>02H</td>
<td>01H</td>
<td>ST1 (a)</td>
<td>Checksum</td>
<td>03H</td>
</tr>
</tbody>
</table>

Remark ST1 (a): Command reception result
5.12.3 Data frame and status frame

Figure 5-32 shows the format of a security data frame, and Figure 5-33 shows the status frame for the data.

**Figure 5-32. Security Data Frame (from Programmer to 78K0R/Kx3)**

<table>
<thead>
<tr>
<th>STX</th>
<th>LEN</th>
<th>Data</th>
<th>SUM</th>
<th>ETX</th>
</tr>
</thead>
<tbody>
<tr>
<td>02H</td>
<td>06H</td>
<td>FLG</td>
<td>BOT</td>
<td>FSWS(H)</td>
</tr>
</tbody>
</table>

**Remarks 1.**
- FLG: Security flag
- BOT: Boot cluster last block number (fixed to 01H)
- FSWS(H): Higher 8 bits of flash shield window start block number (fixed to 00H)
- FSWS(L): Lower 8 bits of flash shield window start block number
- FSWE(H): Higher 8 bits of flash shield window end block number (fixed to 00H)
- FSWE(L): Lower 8 bits of flash shield window end block number

2. If the flash shield window is not to be set, set FSWS to 0000H and the end block to the target device end block number.

**Figure 5-33. Status Frame for Security Data Writing (from 78K0R/Kx3 to Programmer)**

<table>
<thead>
<tr>
<th>STX</th>
<th>LEN</th>
<th>Data</th>
<th>SUM</th>
<th>ETX</th>
</tr>
</thead>
<tbody>
<tr>
<td>02H</td>
<td>01H</td>
<td>ST1 (b)</td>
<td>Checksum</td>
<td>03H</td>
</tr>
</tbody>
</table>

**Remark** ST1 (b): Security data write result

5.12.4 Internal verify check and status frame

Figure 5-34 shows the status frame for internal verify check.

**Figure 5-34. Status Frame for Internal Verify Check (from 78K0R/Kx3 to Programmer)**

<table>
<thead>
<tr>
<th>STX</th>
<th>LEN</th>
<th>Data</th>
<th>SUM</th>
<th>ETX</th>
</tr>
</thead>
<tbody>
<tr>
<td>02H</td>
<td>01H</td>
<td>ST1 (c)</td>
<td>Checksum</td>
<td>03H</td>
</tr>
</tbody>
</table>

**Remark** ST1 (c): Internal verify result

The following table shows the contents in the security flag field.

**Table 5-4. Contents of Security Flag Field**

<table>
<thead>
<tr>
<th>Item</th>
<th>Contents</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bit 7</td>
<td>Fixed to “1”</td>
</tr>
<tr>
<td>Bit 6</td>
<td></td>
</tr>
<tr>
<td>Bit 5</td>
<td></td>
</tr>
<tr>
<td>Bit 4</td>
<td>Boot block rewrite disable flag (1: Enables boot block rewrite, 0: Disable boot block rewrite)</td>
</tr>
<tr>
<td>Bit 3</td>
<td>Fixed to “1”</td>
</tr>
<tr>
<td>Bit 2</td>
<td>Programming disable flag (1: Enables programming, 0: Disable programming)</td>
</tr>
<tr>
<td>Bit 1</td>
<td>Block erase disable flag (1: Enables block erase, 0: Disable block erase)</td>
</tr>
<tr>
<td>Bit 0</td>
<td>Chip erase disable flag (1: Enables chip erase, 0: Disable chip erase)</td>
</tr>
</tbody>
</table>
The following table shows the relationship between the security flag field settings and the enable/disable status of each operation.

**Table 5-5. Security Flag Field and Enable/Disable Status of Each Operation**

<table>
<thead>
<tr>
<th>Operating Mode</th>
<th>Flash Memory Programming Mode</th>
<th>Self-Programming Mode</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Command Operation After Security Setting</td>
<td>• All commands can be executed regardless of the security setting values</td>
</tr>
<tr>
<td></td>
<td>√: Execution possible, ×: Execution impossible</td>
<td>• Only retention of security setting values is possible</td>
</tr>
<tr>
<td></td>
<td>△: Writing and block erase in boot area are impossible</td>
<td>Same condition as that in flash memory programming mode (on-board/off-board programming)</td>
</tr>
<tr>
<td>Security Setting Item</td>
<td>Programming</td>
<td>Chip Erase</td>
</tr>
<tr>
<td>-------------------</td>
<td>-------------</td>
<td>-----------</td>
</tr>
<tr>
<td>Disable programming</td>
<td>×</td>
<td>√</td>
</tr>
<tr>
<td>Disable chip erase</td>
<td>√</td>
<td>×</td>
</tr>
<tr>
<td>Disable block erase</td>
<td>√</td>
<td>√</td>
</tr>
<tr>
<td>Boot block rewrite disable flag</td>
<td>△</td>
<td>×</td>
</tr>
</tbody>
</table>

Read 6.14 **Security Set Command** for details on the flowchart of the processing sequence between the programmer and the 78K0R/Kx3, the flowchart of command processing, and the sample program.
6.1 Command Frame Transmission Processing Flowchart

![Flowchart Image]

- Command frame transmission processing
- Command frame header (SOH = 01H) transmission
- Wait between data transmissions
  - (LEN - 1) bytes transmitted?
    - Yes
    - Command number (COM) transmission
    - Wait between data transmissions
    - Transmits 1-byte command information
    - Wait between data transmissions
    - Checksum data (SUM) transmission
    - Wait between data transmissions
    - Command frame footer (ETX = 03H) transmission
    - End of command frame transmission
  - No
    - Wait between data transmissions
6.2 Data Frame Transmission Processing Flowchart
6.3 Data Frame Reception Processing Flowchart

![Flowchart Image]
6.4 Reset Command

6.4.1 Processing sequence chart

Note  Do not exceed the retry count for the reset command transmission (up to 16 times).
6.4.2 Description of processing sequence

<1> Waits from the previous frame reception until the next command processing starts (wait time \( t_{com} \)).

<2> The low level is output (data 00H is transmitted at 9,600 bps).

<3> Wait state (wait time \( t_{12} \)).

<4> The low level is output (data 00H is transmitted at 9,600 bps).

<5> Wait state (wait time \( t_{2c} \)).

<6> The Reset command is transmitted by command frame transmission processing.

<7> A time-out check is performed from command transmission until status frame reception. If a time-out occurs, a time-out error [C] is returned (time-out time \( t_{WT0} \) (MAX.).)

<8> The status code is checked.

When ST1 = ACK: Normal completion [A]

When ST1 ≠ ACK: The retry count (\( t_{RS} \)) is checked.

The sequence is re-executed from <5> if the retry count is not over.

If the retry count is over, the processing ends abnormally [B].

6.4.3 Status at processing completion

<table>
<thead>
<tr>
<th>Status at Processing Completion</th>
<th>Status Code</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Normal completion [A]</td>
<td>Normal acknowledgment (ACK)</td>
<td>06H</td>
</tr>
<tr>
<td>Abnormal termination [B]</td>
<td>Checksum error</td>
<td>07H</td>
</tr>
<tr>
<td></td>
<td>Negative acknowledgment (NACK)</td>
<td>15H</td>
</tr>
<tr>
<td>Time-out error [C]</td>
<td>–</td>
<td>–</td>
</tr>
</tbody>
</table>
6.4.4 Flowchart

Reset command processing

Wait from previous frame reception until next command transmission

Transmits "00" at 9,600 bps

Wait

Transmits "00" at 9,600 bps

Wait

Command frame transmission processing (Reset)

Status frame received?

Yes

Status = ACK?

Yes

Normal completion [A]

No

Status frame received?

No

Timed out?

Yes

Time-out error [C]

No

Retry count over?

Yes

Abnormal termination [B]

No

Transmits "00" at 9,600 bps

Retry count over?
6.4.5 Sample program
The following shows a sample program for Reset command processing.

```c
u16 fl_ua_reset(void)
{
    u16 rc;
    u32 retry;

    set_uart0_br(BR_9600); // change to 9600bps
    fl_wait(tCOM); // wait
    set_ua_dir_tx(); // Change Mono-wire UART transmit mode
    putc_ua(0x00); // send 0x00 @ 9600bps
    fl_wait(t12); // wait
    putc_ua(0x00); // send 0x00 @ 9600bps
    set_ua_dir_rx(); // Change Mono-wire UART receive mode

    for (retry = 0; retry < tRS; retry++){
        fl_wait(t2C); // wait
        put_cmd_ua(FL_COM_RESET, 1, fl_cmd_prm); // send RESET command

        rc = get_sfrm_ua(fl_ua_sfrm, tWT0_MAX);
        if (rc == FLC_DFTO_ERR) // t.o. ?
            break; // yes // case [C]
        if (rc == FLC_ACK){ // ACK ?
            break; // yes // case [A]
        }
        else{
            NOP();
        }
        //continue; // case [B] (if exit from loop)
    }
    // switch(rc) {
    //     case FLC_NO_ERR: return rc; break; // case [A]
    //     case FLC_DFTO_ERR: return rc; break; // case [C]
    //     default: return rc; break; // case [B]
    // }
    return rc;
}
```
6.5 Baud Rate Set Command

6.5.1 Processing sequence chart

Baud Rate Set command processing sequence

**Programmer 78K0R/Kx3**

- <1> Wait from previous frame reception until next command transmission
- <2> Baud Rate Set command frame transmission
- <3> Wait from command frame transmission until Reset command transmission
- <4> The baud rate of UART is switched to the value set by the Baud Rate Set command.
- <5> Reset command frame transmission
- <6> Time-out check for status frame reception
- <7> Status frame reception

**Note**
Do not exceed the retry count for the reset command transmission (up to 16 times).
6.5.2 Description of processing sequence

<1> Waits from the previous frame reception until the next command transmission (wait time $t_{COM}$).

<2> The Baud Rate Set command is transmitted by command frame transmission processing.

<3> Waits from command transmission until Reset command transmission (wait time $t_{WT10}$).

<4> The baud rate of UART communication is switched to the value set by the Baud Rate Set command.

<5> The Reset command is transmitted by command frame transmission processing.

<6> A time-out check is performed from command transmission until status frame reception.
   If a time-out occurs, a time-out error [C] is returned (time-out time $t_{WT0}(\text{MAX.})$).

<7> Since the status code should be ACK, the processing ends normally [A].

6.5.3 Status at processing completion

<table>
<thead>
<tr>
<th>Status at Processing Completion</th>
<th>Status Code</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Normal completion [A]</td>
<td>Normal acknowledgment (ACK)</td>
<td>06H</td>
</tr>
<tr>
<td>Abnormal termination [B]</td>
<td>Checksum error</td>
<td>07H</td>
</tr>
<tr>
<td></td>
<td>Negative acknowledgment (NACK)</td>
<td>15H</td>
</tr>
<tr>
<td>Time-out error [C]</td>
<td>–</td>
<td>Data frame reception was timed out. With the 78K0R/Kx3, this command also results in errors in the following cases.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Command information (D01, D02H, D02L, D03) is invalid</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• The command frame includes the checksum error</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• The data length of the command frame (LEN) is invalid</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• The footer of the command frame (ETX) is missing</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• The Reset command was not detected after setting the baud rate and receiving command frame data for 16 times.</td>
</tr>
</tbody>
</table>

Note: If a time-out error has occurred, execute a hardware reset and re-set to the flash memory programming mode.
6.5.4 Flowchart

Baud Rate Set command processing

Wait from previous frame reception until next command transmission

Command frame transmission processing (Baud Rate Set)

Wait from command frame transmission until Reset command transmission

Command frame transmission processing (Reset)

Status frame received?

Yes

Timed out?

No

Yes

Normal completion [A]

Time-out error [C]

No

twt10

tCOM
6.5.5 Sample program

The following shows a sample program for Baud Rate Set command processing.

```c
/** ******************************************/
/*                                      */
/* Set baudrate command                  */
/*                                      */
/** ******************************************/
/* [i] u8 brid ... baudrate ID           */
/* [r] u16 ... error code                */
/** ******************************************/

u16 fl_ua_setbaud(u8 brid) {  
  u16 rc;  
  u8 br;  
  u32 retry;  

  fl_cmd_prm[0] = 0x00; // "D01": adjust by target device (115200bps)
  fl_cmd_prm[1] = 0x00; // "D02": adjust by target device (115200bps)
  fl_cmd_prm[2] = 0x0a; // "D03": (fixed value)
  fl_cmd_prm[3] = 0x01; // "D04": noise filter on

  fl_wait(tCOM); // wait before sending command
  put_cmd_ua(FL_COM_SET_BAUDRATE, 1+4, fl_cmd_prm); // send "Baudrate Set" command
  set_flbaud(brid); // change baud-rate
  set_uart0_br(brid); // change baud-rate (h.w.)

  retry = tRS;
  while(1){
    fl_wait(tWT10);

    put_cmd_ua(FL_COM_RESET, 1, fl_cmd_prm); // send RESET command
    rc = get_sfrm_ua(fl_ua_sfrm, tWT0_MAX); // get status frame
    if (rc){
      if (retry--)
        continue;
      else
        return rc;
    }
    break; // got ACK !!
  }

  switch(rc) {  
    case FLC_NO_ERR: return rc; break; // case [A]
    case FLC_DFTO_ERR: return rc; break; // case [C]
    default: return rc; break; // case [B]
  }

  return rc;
}
```
6.6 Chip Erase Command

6.6.1 Processing sequence chart

Chip Erase command processing sequence
6.6.2 Description of processing sequence

<1> Waits from the previous frame reception until the next command transmission (wait time t<sub>com</sub>).
<2> The Chip Erase command is transmitted by command frame transmission processing.
<3> A time-out check is performed from command transmission until status frame reception. If a time-out occurs, a time-out error [C] is returned (time-out time t<sub>WT1</sub>(MAX.)).
<4> The status code is checked.

When ST1 = ACK: Normal completion [A]
When ST1 ≠ ACK: Abnormal termination [B]

6.6.3 Status at processing completion

<table>
<thead>
<tr>
<th>Status at Processing Completion</th>
<th>Status Code</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Normal completion [A]</td>
<td>Normal acknowledgment (ACK)</td>
<td>06H</td>
</tr>
<tr>
<td>Abnormal termination [B]</td>
<td>Checksum error</td>
<td>07H</td>
</tr>
<tr>
<td>Protect error</td>
<td>10H</td>
<td>Chip erase or boot block rewrite is prohibited in the security setting.</td>
</tr>
<tr>
<td>Negative acknowledgment (NACK)</td>
<td>15H</td>
<td>Command frame data is abnormal (such as invalid data length (LEN) or no ETX).</td>
</tr>
<tr>
<td>MRG10 error</td>
<td>1AH</td>
<td>An erase error has occurred.</td>
</tr>
<tr>
<td>MRG11 error</td>
<td>1BH</td>
<td>–</td>
</tr>
<tr>
<td>Write error</td>
<td>1CH</td>
<td>The status frame was not received within the specified time.</td>
</tr>
<tr>
<td>Time-out error [C]</td>
<td>–</td>
<td>–</td>
</tr>
</tbody>
</table>
6.6.4 Flowchart

- Chip Erase command processing
- Waits from previous frame reception until next command transmission
- Command frame transmission processing (Chip Erase)
- Status frame received?
  - Yes
    - Status = ACK?
      - Yes
        - Normal completion [A]
      - No
        - Abnormal termination [B]
  - No
    - Timed out?
      - No
        - Status frame received?
          - Yes
            - Status = ACK?
              - Yes
                - Normal completion [A]
              - No
                - Abnormal termination [B]
          - No
            - Timed out [A] (MAX.)
              - Yes
                - Time-out error [C]
              - No

- No
6.6.5 Sample program

The following shows a sample program for Chip Erase command processing.

```c
/* *************************************************************************/
/*                        */
/* Erase all (chip) command */
/*                        */
/* *************************************************************************/
/* [r] u16 ... error code */
/* *************************************************************************/

u16 fl_ua_erase_all(void)
{
    u16 rc;

    fl_wait(tCOM);  // wait before sending command

    put_cmd_ua(FL_COM_ERASE_CHIP, 1, fl_cmd_prm); // send ERASE CHIP command

    rc = get_sfrm_ua(fl_ua_sfrm, tWT1_MAX); // get status frame
    // switch(rc) {
    //     // case FLC_NO_ERR: return rc; break; // case [A]
    //     // case FLC_DFTO_ERR: return rc; break; // case [C]
    //     default: return rc; break; // case [B]
    // }
    return rc;
}
```
6.7 Block Erase Command

6.7.1 Processing sequence chart

Block Erase command processing sequence

1. Wait from previous frame reception until next command transmission.

2. Block Erase command frame transmission.

3. Time-out check for status frame reception.


- Normal completion [A]
- Time-out error [C]
- Abnormal termination [B]
- Other than ACK

- Reception status [ACK/other than ACK]
6.7.2 Description of processing sequence

<1> Waits from the previous frame reception until the next command transmission (wait time \(t_{COM}\)).

<2> The Block Erase command is transmitted by command frame transmission processing.

<3> A time-out check is performed from command transmission until status frame reception. If a time-out occurs, a time-out error [C] is returned (time-out time \(t_{WT2(\text{MAX.})}\)).

<4> The status code is checked.

When ST1 = ACK: Normal completion [A]
When ST1 ≠ ACK: Abnormal termination [B]

6.7.3 Status at processing completion

<table>
<thead>
<tr>
<th>Status at Processing Completion</th>
<th>Status Code</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Normal completion [A]</td>
<td>Normal acknowledgment (ACK)</td>
<td>06H</td>
</tr>
<tr>
<td>Abnormal termination [B]</td>
<td>Parameter error</td>
<td>05H</td>
</tr>
<tr>
<td></td>
<td>Checksum error</td>
<td>07H</td>
</tr>
<tr>
<td></td>
<td>Protect error</td>
<td>10H</td>
</tr>
<tr>
<td></td>
<td>Negative acknowledgment (NACK)</td>
<td>15H</td>
</tr>
<tr>
<td></td>
<td>MRG10 error</td>
<td>1AH</td>
</tr>
<tr>
<td>Time-out error [C]</td>
<td>–</td>
<td>The status frame was not received within the specified time.</td>
</tr>
</tbody>
</table>
6.7.4 Flowchart

1. **Block Erase command processing**
2. **Wait from previous frame reception until next command transmission**
3. **Command frame transmission processing (Block Erase)**
4. **Status frame received?**
   - Yes: **Status = ACK?**
     - Yes: **Normal completion [A]**
     - No: **Abnormal termination [B]**
   - No: **Timed out?**
     - Yes: **Time-out error [C]**
     - No: **tWT2 (MAX.)**

**Flowchart Diagram:**
- Start at Block Erase command processing.
- Proceed to Wait from previous frame reception until next command transmission.
- Continue to Command frame transmission processing (Block Erase).
- Evaluate if Status frame received?
  - If Yes, check Status = ACK?
    - If Yes, proceed to Normal completion [A].
    - If No, proceed to Abnormal termination [B].
  - If No, check Timed out?
    - If Yes, proceed to Time-out error [C].
    - If No, proceed to tWT2 (MAX.).
6.7.5 Sample program

The following shows a sample program for Block Erase command processing.

```c
u16  fl_ua_erase_blk(u16 sblk, u16 eblk)
{
    u16  rc;
    u32  wt2_max;
    u32  top, bottom;

    top = get_top_addr(sblk);  // get start address of start block
    bottom = get_bottom_addr(eblk);  // get end address of end block

    set_range_prm(fl_cmd_prm, top, bottom); // set SAH/SAM/SAL, EAH/EAM/EAL

    wt2_max = make_wt2_max(sblk, eblk);

    fl_wait(tCOM);  // wait before sending command

    put_cmd_ua(FL_COM_ERASE_BLOCK, 1+6, fl_cmd_prm); // send ERASE CHIP command

    rc = get_sfrm_ua(fl_ua_sfrm, wt2_max);  // get status frame

    // switch(rc) {
      // case FLC_NO_ERR:  return rc;  break; // case [A]
      // case FLC_DFTO_ERR:  return rc;  break; // case [C]
      // default:  return rc;  break; // case [B]
    // }

    return rc;
}
```
6.8 Programming Command

6.8.1 Processing sequence chart

Programming command processing sequence
6.8.2 Description of processing sequence

<1> Waits from the previous frame reception until the next command transmission (wait time \( t_{\text{COM}} \)).

<2> The Programming command is transmitted by command frame transmission processing.

<3> A time-out check is performed from command transmission until status frame reception.
   If a time-out occurs, a time-out error [C] is returned (time-out time \( t_{\text{WT3}} (\text{MAX.}) \)).

<4> The status code is checked.
   - When \( ST1 = \text{ACK} \): Proceeds to <5>.
   - When \( ST1 \neq \text{ACK} \): Abnormal termination [B]

<5> Waits from the previous frame reception until the next data frame transmission (wait time \( t_{\text{FD3}} \)).

<6> User data is transmitted by data frame transmission processing.

<7> A time-out check is performed from user data transmission until data frame reception.
   If a time-out occurs, a time-out error [C] is returned (time-out time \( t_{\text{WT4}} (\text{MAX.}) \)).

<8> The status code (ST1/ST2) is checked (also refer to the processing sequence chart and flowchart).
   - When \( ST1 \neq \text{ACK} \): Abnormal termination [B]
   - When \( ST1 = \text{ACK} \): The following processing is performed according to the ST2 value.
     - When \( ST2 = \text{ACK} \): Proceeds to <9> when transmission of all data frames is completed.
       If there still remain data frames to be transmitted, the processing re-executes the sequence from <5>.
     - When \( ST2 \neq \text{ACK} \): Abnormal termination [D]

<9> A time-out check is performed until status frame reception.
   If a time-out occurs, a time-out error [C] is returned (time-out time \( t_{\text{WT5}} (\text{MAX.}) \times \text{number of blocks} \)).

<10> The status code is checked.
   - When \( ST1 = \text{ACK} \): Normal completion [A]
   - When \( ST1 \neq \text{ACK} \): Abnormal termination [E]
### 6.8.3 Status at processing completion

<table>
<thead>
<tr>
<th>Status at Processing Completion</th>
<th>Status Code</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Normal completion [A]</td>
<td>Normal acknowledgment (ACK)</td>
<td>06H The command was executed normally and the user data was written normally.</td>
</tr>
<tr>
<td>Abnormal termination [B]</td>
<td>Parameter error</td>
<td>05H The start/end address is out of the flash memory range, the specified start/end address is not the first/end address of the block, or the write start address is larger than the end address.</td>
</tr>
<tr>
<td></td>
<td>Checksum error</td>
<td>07H The checksum of the transmitted command frame or data frame does not match.</td>
</tr>
<tr>
<td></td>
<td>Protect error</td>
<td>10H Write is prohibited in the security setting. A boot block is included in the specified range and boot block rewrite is prohibited.</td>
</tr>
<tr>
<td></td>
<td>Negative acknowledgment (NACK)</td>
<td>15H Command frame data or data frame data is abnormal (such as invalid data length (LEN) or no ETX).</td>
</tr>
<tr>
<td>Time-out error [C]</td>
<td>–</td>
<td>– The status frame was not received within the specified time.</td>
</tr>
<tr>
<td>Abnormal termination [D], [E]</td>
<td>MRG10 error</td>
<td>1AH A write error has occurred.</td>
</tr>
<tr>
<td></td>
<td>MRG11 error</td>
<td>1BH</td>
</tr>
<tr>
<td></td>
<td>Write error</td>
<td>1CH</td>
</tr>
</tbody>
</table>
6.8.4 Flowchart

```
CHAPTER 6 UART COMMUNICATION MODE

6.8.4 Flowchart

Programming command processing

Wait from previous frame reception until next command transmission

Command frame transmission processing (Programming)

Status frame received?
  Yes
    Status = ACK?
      Yes
        Abnormal termination [B]
      No
        Normal completion [A]
    No
      Timed out?
        Yes
          Time-out error [C]
        No
          Status = ACK?
            Yes
              Abnormal termination [B]
            No
              Abnormal termination [E]

Data frame transmission processing (User program)

Wait from previous frame reception until next command transmission

Status frame received?
  Yes
    ST1 = ACK?
      Yes
        Abnormal termination [B]
      No
        ST2 = ACK?
          Yes
            Abnormal termination [D]
          No
            All data frames transmitted?
              Yes
                Abnormal termination [B]
              No
                Timed out?
                  Yes
                    Time-out error [C]
                  No
                    Status = ACK?
                      Yes
                        Abnormal termination [E]
                      No
                        Status = ACK?
                          Yes
                            Normal completion [A]
                          No
                            Time-out error [C]

TIM (MAX.)
```

× number of blocks
6.8.5 Sample program

The following shows a sample program for Programming command processing.

```c
#define fl_st2_ua (fl_ua_sfrm[OFS_STA_PLD+1])

u16 fl_ua_write(u32 top, u32 bottom)
{
    u16 rc;
    u32 send_head, send_size;
    bool is_end;
    u16 block_num;

    block_num = get_block_num(top, bottom); // get block num

    set_range_prm(fl_cmd_prm, top, bottom); // set SAH/SAM/SAL, EAH/EAM/EAL

    fl_wait(tCOM);    // wait before sending command
    put_cmd_ua(FL_COM_WRITE, 7, fl_cmd_prm);// send "Programming" command
    rc = get_sfrm_ua(fl_ua_sfrm, tWT3_MAX); // get status frame
    switch(rc) {
        case FLC_NO_ERR:    break; // continue
        // case FLC_DFTO_ERR: return rc; break; // case [C]
        default:   return rc;  break; // case [B]
    }

    send_head = top;
    while(1){
        // make send data frame
        if ((bottom - send_head) > 256){  // rest size > 256 ?
            is_end = false;   // yes, not is_end frame
            send_size  = 256;   // transmit size = 256 byte
            break;
        }
    }
}
```

else{
    is_end = true;
    send_size = bottom - send_head + 1; // transmit size = (bottom
- send_head)+1 byte
}

memcpysf(f1_txdastdata_frm, rom_buf+send_head, send_size); // set data frame
payload
send_head += send_size;

f1_wait(tFD3); // wait before sending data frame
put_dfrm_ua(send_size, f1_txdastdata_frm, is_end); // send user data

rc = get_sfrm_ua(f1_ua_sfrm, tWT4_MAX); // get status frame
switch(rc) {
    case FLC_NO_ERR: break; // continue
    case FLC_DFTO_ERR: return rc; break; // case [C]
    default: return rc; break; // case [B]
}
if (f1_st2_ua != FLST_ACK){ // ST2 = ACK ?
    rc = decode_status(f1_st2_ua); // No
    return rc; // case [D]
}
if (is_end)
    break;

/*******************
/* Check internally verify */
/
***************************/

rc = get_sfrm_ua(f1_ua_sfrm, tWT5_MAX*block_num); // get status frame again
switch(rc) {
    case FLC_NO_ERR: return rc; break; // case [A]
    case FLC_DFTO_ERR: return rc; break; // case [C]
    default: return rc; break; // case [E]
}

return rc;
}
6.9 Verify Command

6.9.1 Processing sequence chart

Verify command processing sequence

Programmer 78K0R/Kx3

1. Wait from previous frame reception until next command transmission

2. Verify command frame transmission

3. Time-out check for status frame reception

4. Status frame reception

5. Wait from previous frame reception until next data frame transmission

6. Data frame (user data for verify) transmission

7. Time-out check for status frame reception

8. Status frame reception (ST1/ST2)

- If Status frame received within specified time: Normal completion [A] (ACK)
- If Time-out occurs: Time-out error [C]

- If Reception status [ACK/other than ACK]:
  - Other than ACK: Abnormal termination [B]
  - ACK: Go to <5>

- If All data frames transmitted? [Yes/No]:
  - No: Go to <5>
  - Yes: Normal completion [A] (ACK)

- If Time-out error [C]:
  - Abnormal termination [B]

- If Reception status (ST1) [ACK/other than ACK]:
  - Other than ACK: Abnormal termination [B]
  - ACK: Go to <5>

- If Reception status (ST2) [ACK/other than ACK]:
  - Other than ACK: Abnormal termination [D]
  - ACK: Go to <5>
6.9.2 Description of processing sequence

<1> Waits from the previous frame reception until the next command transmission (wait time $t_{\text{COM}}$).
<2> The Verify command is transmitted by command frame transmission processing.
<3> A time-out check is performed from command transmission until status frame reception.
   If a time-out occurs, a time-out error [C] is returned (time-out time $t_{\text{WT6 (MAX.)}}$).
<4> The status code is checked.
   When ST1 = ACK: Proceeds to <5>.
   When ST1 $\neq$ ACK: Abnormal termination [B]
<5> Waits from the previous frame reception until the next data frame transmission (wait time $t_{\text{FD3}}$).
<6> User data for verifying is transmitted by data frame transmission processing.
<7> A time-out check is performed from user data transmission until status frame reception.
   If a time-out occurs, a time-out error [C] is returned (time-out time $t_{\text{WT7 (MAX.)}}$).
<8> The status code (ST1/ST2) is checked (also refer to the processing sequence chart and flowchart).
   When ST1 $\neq$ ACK: Abnormal termination [B]
   When ST1 = ACK: The following processing is performed according to the ST2 value.
   - When ST2 = ACK: If transmission of all data frames is completed, the processing ends normally [A].
     If there still remain data frames to be transmitted, the processing re-executes the sequence from <5>.
   - When ST2 $\neq$ ACK: Abnormal termination [D]

6.9.3 Status at processing completion

<table>
<thead>
<tr>
<th>Status at Processing Completion</th>
<th>Status Code</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Normal completion [A]</td>
<td>Normal acknowledgment (ACK)</td>
<td>06H</td>
</tr>
<tr>
<td>Abnormal termination [B]</td>
<td>Parameter error</td>
<td>05H</td>
</tr>
<tr>
<td></td>
<td>Checksum error</td>
<td>07H</td>
</tr>
<tr>
<td></td>
<td>Negative acknowledgment (NACK)</td>
<td>15H</td>
</tr>
<tr>
<td>Time-out error [C]</td>
<td>–</td>
<td>The status frame was not received within the specified time.</td>
</tr>
<tr>
<td>Abnormal termination [D]</td>
<td>Verify error</td>
<td>0FH (ST2)</td>
</tr>
</tbody>
</table>
6.9.4 Flowchart

Verify command processing

Wait from previous frame reception until next command transmission

Command frame transmission processing (Verify)

Status frame received? No

Wait from previous frame reception until next data frame transmission

Data frame transmission processing (User program)

Status frame received? No

Wait from previous frame reception until next data frame transmission

Data frame transmission processing (User program)

Status frame received? No

Wait from previous frame reception until next command transmission

Command frame transmission processing (Verify)

ST1 = ACK? Yes

Time-out? No

ST1 = ACK? Yes

Time-out error [C]

Status frame received? No

Wait from previous frame reception until next command transmission

Command frame transmission processing (Verify)

ST1 = ACK? Yes

All data frames transmitted? No

ST2 = ACK? Yes

Time-out error [C]

All data frames transmitted? No

ST2 = ACK? Yes

Normal completion [A]
6.9.5 Sample program

The following shows a sample program for Verify command processing.

```c
u16  fl_ua_verify(u32 top, u32 bottom, u8 *buf)
{
    u16  rc;
    u32  send_head, send_size;
    bool is_end;

    set_range_prm(fl_cmd_prm, top, bottom); // set SAH/SAM/SAL, EAH/EAM/EAL

    fl_wait(tCOM); // wait before sending command

    put_cmd_ua(FL_COM_VERIFY, 7, fl_cmd_prm); // send VERIFY command

    rc = get_sfrm_ua(fl_ua_sfrm, tWT6_MAX); // get status frame

    switch(rc) {
    case FLC_NO_ERR:    break; // continue
    // case FLC_DFTO_ERR: return rc;  break; // case [C]
    default:  return rc;  break; // case [B]
    }

    send_head = top;

    while(1){
        // make send data frame
        if ((bottom - send_head) > 256){ // rest size > 256 ?
            is_end = false; // yes, not is_end frame
            send_size = 256; // transmit size = 256 byte
        } else{
            is_end = true;
            send_size = bottom - send_head + 1; // transmit size = (bottom - send_head)+1 byte
```
} memcpy(fl_txdata_frm, buf+send_head, send_size);// set data frame payload
send_head += send_size;

fl_wait(tFD3);
put_dfrm_ua(send_size, fl_txdata_frm, is_end); // send user data

rc = get_sfrm_ua(fl_ua_sfrm, tWT7_MAX);  // get status frame
switch(rc) {
    case FLC_NO_ERR:   break; // continue

    case FLC_DFTO_ERR: return rc; break; // case [C]

    default:  return rc; break; // case [B]
}

if (fl_st2_ua != FLST_ACK){  // ST2 = ACK ?
    rc = decode_status(fl_st2_ua); // No
    return rc;    // case [D]
}

if (is_end)      // send all user data ?
    break;      // yes
//continue;

return FLC_NO_ERR;  // case [A]
6.10 Block Blank Check Command

6.10.1 Processing sequence chart

Block Blank Check command processing sequence

Programmer 78K0R/Kx3

1. Wait from previous frame reception until next command transmission

2. Block Blank Check command frame transmission

3. Time-out check for status frame reception

4. Status frame reception

Time-out occurs

Status frame received within specified time

Other than ACK

Abnormal termination [B]

ACK

Normal completion [A]

Reception status [ACK/other than ACK]

Time-out error [C]
6.10.2 Description of processing sequence

<1> Waits from the previous frame reception until the next command transmission (wait time \( t_{\text{com}} \)).

<2> The Block Blank Check command is transmitted by command frame transmission processing.

<3> A time-out check is performed from command transmission until status frame reception.
    If a time-out occurs, a time-out error [C] is returned (time-out time \( t_{\text{WT8}}(\text{MAX.}) \times \text{number of blocks} \)).

<4> The status code is checked.

When \( \text{ST1} = \text{ACK} \): Normal completion [A]
When \( \text{ST1} \neq \text{ACK} \): Abnormal termination [B]

6.10.3 Status at processing completion

<table>
<thead>
<tr>
<th>Status at Processing Completion</th>
<th>Status Code</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Normal completion [A]</td>
<td>Normal acknowledgment (ACK)</td>
<td>06H</td>
</tr>
<tr>
<td>Abnormal termination [B]</td>
<td>Parameter error</td>
<td>05H</td>
</tr>
<tr>
<td></td>
<td>Checksum error</td>
<td>07H</td>
</tr>
<tr>
<td></td>
<td>Negative acknowledgment (NACK)</td>
<td>15H</td>
</tr>
<tr>
<td></td>
<td>MRG11 error</td>
<td>1BH</td>
</tr>
<tr>
<td>Time-out error [C]</td>
<td>–</td>
<td>The status frame was not received within the specified time.</td>
</tr>
</tbody>
</table>
6.10.4 Flowchart

Block Blank Check command processing

Wait from previous frame reception until next command transmission

Command frame transmission processing (Block Blank Check)

Status frame received?

Yes

Timed out?

Yes

Time-out error [C]

No

$t_{\text{COM}}$ × number of blocks

No

Status = ACK?

Yes

Normal completion [A]

No

Abnormal termination [B]
6.10.5 Sample program

The following shows a sample program for Block Blank Check command processing.

```c
u16 fl_ua_blk_blank_chk(u32 top, u32 bottom, u8 whole)
{
    u16 rc;
    u16 block_num;

    set_range_prm(fl_cmd_prm, top, bottom); // set SAH/SAM/SAL, EAH/EAM/EAL
    block_num = get_block_num(top, bottom); // get block num
    fl_cmd_prm[6] = whole; // check only user area or not

    fl_wait(tCOM); // wait before sending command

    put_cmd_ua(FL_COM_BLOCK_BLANK_CHK, 7+1, fl_cmd_prm);

    rc = get_sfrm_ua(fl_ua_sfrm, tWT8_MAX * block_num); // get status frame
    switch(rc) {
        case FLC_NO_ERR:    return rc;  break; // case [A]
        case FLC_DFTO_ERR:  return rc;  break; // case [C]
        default: return rc;  break; // case [B]
    }
    return rc;
}
```
6.11 Silicon Signature Command

6.11.1 Processing sequence chart

Silicon Signature command processing sequence

Programmer 78K0R/Kx3

<1> Wait from previous frame reception until next command transmission
<2> Silicon Signature command frame transmission
<3> Time-out check for status frame reception
<4> Status frame reception
<5> Time-out check for data frame reception
<6> Data frame (silicon signature) reception

Time-out occurs

Status frame received within specified time

Reception status [ACK/other than ACK]

ACK

Other than ACK

Abnormal termination [B]

Time-out occurs

Data frame received within specified time

Time-out error [C]

Normal data frame? [Yes/No]

No

Data frame error [D]

Yes

Normal completion [A]
6.11.2 Description of processing sequence

<1> Waits from the previous frame reception until the next command transmission (wait time \( t_{\text{com}} \)).

<2> The Silicon Signature command is transmitted by command frame transmission processing.

<3> A time-out check is performed from command transmission until status frame reception.
   If a time-out occurs, a time-out error \([C]\) is returned (time-out time \( t_{\text{WT1}}(\text{MAX.}) \)).

<4> The status code is checked.
   
   When \( \text{ST1} = \text{ACK} \): Proceeds to <5>.
   When \( \text{ST1} \neq \text{ACK} \): Abnormal termination [B]

<5> A time-out check is performed until data frame (silicon signature data) reception.
   If a time-out occurs, a time-out error \([C]\) is returned (time-out time \( t_{\text{FD2}}(\text{MAX.}) \)).

<6> The received data frame (silicon signature data) is checked.
   
   If data frame is normal: Normal completion [A]
   If data frame is abnormal: Data frame error [D]

6.11.3 Status at processing completion

<table>
<thead>
<tr>
<th>Status at Processing Completion</th>
<th>Status Code</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Normal completion [A]</td>
<td>Normal acknowledgment (ACK)</td>
<td>06H</td>
</tr>
<tr>
<td>Abnormal termination [B]</td>
<td>Checksum error</td>
<td>07H</td>
</tr>
<tr>
<td>Abnormal termination [B]</td>
<td>Negative acknowledgment (NACK)</td>
<td>15H</td>
</tr>
<tr>
<td>Time-out error [C]</td>
<td>–</td>
<td>The status frame or data frame was not received within the specified time.</td>
</tr>
<tr>
<td>Data frame error [D]</td>
<td>–</td>
<td>The checksum of the data frame received as silicon signature data does not match.</td>
</tr>
</tbody>
</table>
6.11.4 Flowchart

Silicon Signature command processing

Wait from previous frame reception until next command transmission tCOM

Command frame transmission processing (Silicon Signature)

Status frame received?

Yes

No

Status = ACK?

Yes

Abnormal termination [B]

No

Timed out?

Yes

Time-out error [C]

No

Data frame (silicon signature) received?

Yes

Timed out?

No

No

Normal data frame?

Yes

Normal completion [A]

No

Data frame error [D]
6.11.5 Sample program

The following shows a sample program for Silicon Signature command processing.

```c
/*******************************************************/
/* */
/* Get silicon signature command */
/* */
/*******************************************************/
/* [i] u8 *sig ... pointer to signature save area */
/* [r] u16 ... error code */
/*******************************************************/
u16 fl_ua_getsig(u8 *sig)
{
    u16 rc;

    fl_wait(tCOM); // wait before sending command

    put_cmd_ua(FL_COM_GET_SIGNATURE, 1, fl_cmd_prm); // send GET SIGNATURE command

    rc = get_sfrm_ua(fl_ua_sfrm, tWT11_MAX); // get status frame
    switch(rc) {
        case FLC_NO_ERR:   break; // continue
        // case FLC_DFTO_ERR: return rc; break; // case [C]
        default:  return rc; break; // case [B]
    }

    rc = get_dfrm_ua(fl_rxdata_frm, tFD2_MAX); // get status frame
    if (rc){ // if error
        return rc; // case [D]
    }
    memcpy(sig, fl_rxdata_frm+OFS_STA_PLD, fl_rxdata_frm[OFS_LEN]); // copy Signature data
    return rc; // case [A]
}
```
6.12 Version Get Command

6.12.1 Processing sequence chart

Version Get command processing sequence

Programmer 78K0R/Kx3

1. Wait from previous frame reception until next command transmission

2. Version Get command frame transmission

3. Time-out check for status frame reception

4. Status frame reception

5. Time-out check for data frame reception

6. Data frame (version data) reception

- Normal data frame? [Yes/No]
  - Yes
    - Normal completion [A]
  - No
    - Data frame error [D]

- Time-out error [C]
  - Status frame received within specified time
    - Normal completion [A]
    - Time-out [C]
  - Time-out occurs
    - Other than ACK [B]
      - Abnormal termination [B]
      - Time-out [C]
    - ACK
      - Reception status [ACK/other than ACK]
        - Normal completion [A]
        - Time-out [C]

- tCOM (MAX.)
- tWT12 (MAX.)
- tFD2 (MAX.)
### 6.12.2 Description of processing sequence

<1> Waits from the previous frame reception until the next command transmission (wait time \( t_{\text{com}} \)).

<2> The Version Get command is transmitted by command frame transmission processing.

<3> A time-out check is performed from command transmission until status frame reception.
   If a time-out occurs, a time-out error [C] is returned (time-out time \( t_{\text{WT12}}(\text{MAX.}) \)).

<4> The status code is checked.

   When \( ST1 = \text{ACK} \): Proceeds to <5>.
   When \( ST1 \neq \text{ACK} \): Abnormal termination [B]

<5> A time-out check is performed until data frame (version data) reception.
   If a time-out occurs, a time-out error [C] is returned (time-out time \( t_{\text{FD2}}(\text{MAX.}) \)).

<6> The received data frame (version data) is checked.

   If data frame is normal: Normal completion [A]
   If data frame is abnormal: Data frame error [D]

### 6.12.3 Status at processing completion

<table>
<thead>
<tr>
<th>Status at Processing Completion</th>
<th>Status Code</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Normal completion [A]</td>
<td>Normal acknowledgment (ACK)</td>
<td>06H</td>
</tr>
<tr>
<td>Abnormal termination [B]</td>
<td>Checksum error</td>
<td>07H</td>
</tr>
<tr>
<td></td>
<td>Negative acknowledgment (NACK)</td>
<td>15H</td>
</tr>
<tr>
<td>Time-out error [C]</td>
<td>–</td>
<td>The status frame or data frame was not received within the specified time.</td>
</tr>
<tr>
<td>Data frame error [D]</td>
<td>–</td>
<td>The checksum of the data frame received as version data does not match.</td>
</tr>
</tbody>
</table>
6.12.4 Flowchart

1. **Version Get command processing**

2. **Wait from previous frame reception until next command transmission**

3. **Command frame transmission processing (Version Get)**

   - **Status frame received?**
     - Yes
       - **Status = ACK?**
         - Yes
           - Abnormal termination [B]
         - No
           - Data frame (version data) received?
             - No
               - Status = ACK?
                 - Yes
                   - Abnormal termination [B]
                 - No
                   - Timed out? (tCOM)
                     - Yes
                       - Time-out error [C]
                     - No
                       - Normal data frame?
                         - Yes
                           - Normal completion [A]
                         - No
                           - Timed out? (tFD2)
                             - Yes
                               - Time-out error [C]
                             - No
                               - Timed out? (tWT12)
                                 - Yes
                                   - Time-out error [C]
                                 - No
                                   - Normal completion [A]

   - No
     - Timed out? (tWT12)
       - Yes
         - Time-out error [C]
       - No
         - Normal completion [A]
6.12.5 Sample program

The following shows a sample program for Version Get command processing.

```c
u16 fl_ua_getver(u8 *buf)
{
    u16 rc;

    fl_wait(tCOM); // wait before sending command

    put_cmd_ua(FL_COM_GET_VERSION, 1, fl_cmd_prm); // send GET VERSION command

    rc = get_sfrm_ua(fl_ua_sfrm, tWT12_MAX); // get status frame
    switch(rc) {
        case FLC_NO_ERR:    break; // continue
        // case FLC_DFTO_ERR: return rc;  break; // case [C]
        default:  return rc;  break; // case [B]
    }

    rc = get_dfrm_ua(fl_rxdata_frm, tFD2_MAX); // get data frame
    if (rc){
        return rc; // case [D]
    }

    memcpy(buf, fl_rxdata_frm+OFS_STA_PLD, DFV_LEN); // copy version data
    return rc; // case [A]
}
```
6.13 Checksum Command

6.13.1 Processing sequence chart

Checksum command processing sequence

Programmer 78K0R/Kx3

<1> Wait from previous frame reception until next command transmission

<2> Checksum command frame transmission

<3> Time-out check for status frame reception

<4> Status frame reception

<5> Time-out check for data frame reception

<6> Data frame (checksum data) reception

Normal data frame? [Yes/No]

No

Data frame error [D]

Yes

Normal completion [A]

Reception status [ACK/other than ACK]

ACK

Other than ACK

Abnormal termination [B]

Time-out error [C]

Time-out occurs

Status frame received within specified time

<3> Time-out check for status frame reception

<5> Time-out check for data frame reception

<6> Data frame (checksum data) reception

<2> Checksum command frame transmission

<1> Wait from previous frame reception until next command transmission

Programmer 78K0R/Kx3
6.13.2 Description of processing sequence

<1> Waits from the previous frame reception until the next command transmission (wait time \( t_{\text{com}} \)).

<2> The Checksum command is transmitted by command frame transmission processing.

<3> A time-out check is performed from command transmission until status frame reception.
   If a time-out occurs, a time-out error [C] is returned (time-out time \( t_{\text{WT1}} \text{(MAX.)} \)).

<4> The status code is checked.

   When \( ST1 = \text{ACK} \): Proceeds to <5>.
   When \( ST1 \neq \text{ACK} \): Abnormal termination [B]

<5> A time-out check is performed until data frame (checksum data) reception.
   If a time-out occurs, a time-out error [C] is returned (time-out time \( t_{\text{FD1}} \text{(MAX.)} \)).

<6> The received data frame (checksum data) is checked.

   If data frame is normal: Normal completion [A]
   If data frame is abnormal: Data frame error [D]

6.13.3 Status at processing completion

<table>
<thead>
<tr>
<th>Status at Processing Completion</th>
<th>Status Code</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Normal completion [A]</td>
<td>06H</td>
<td>The command was executed normally and checksum data was acquired normally.</td>
</tr>
<tr>
<td>Abnormal termination [B]</td>
<td>05H</td>
<td>The specified start/end address is out of the flash memory range, or the start/end address is not the start/end address of the block.</td>
</tr>
<tr>
<td></td>
<td>07H</td>
<td>The checksum of the transmitted command frame does not match.</td>
</tr>
<tr>
<td></td>
<td>15H</td>
<td>Command frame data is abnormal (such as invalid data length (LEN) or no ETX).</td>
</tr>
<tr>
<td>Time-out error [C]</td>
<td>–</td>
<td>The status frame or data frame was not received within the specified time.</td>
</tr>
<tr>
<td>Data frame error [D]</td>
<td>–</td>
<td>The checksum of the data frame received as checksum data does not match.</td>
</tr>
</tbody>
</table>
6.13.4 Flowchart

Checksum command processing

Wait from previous frame reception until next command transmission

Command frame transmission processing (Checksum)

Status frame received?

Yes

Status = ACK?

Yes

Abnormal termination [B]

No

Data frame (checksum data) received?

Yes

Normal data frame?

Yes

Normal completion [A]

No

Data frame error [D]

No

No

Status = ACK?

Yes

Timed out?

No

Time-out error [C]

Yes

tWT16 (MAX.)

Abnormal termination [B]

Timed out?

No

Time-out error [C]

Yes

tFD1 (MAX.)

Timed out?

No

Data frame error [D]

No

Normal completion [A]
6.13.5 Sample program
The following shows a sample program for Checksum command processing.

```c
/* Get checksum command */
/*****************************/
/* [i] u16 *sum ... pointer to checksum save area */
/* [i] u32 top ... start address */
/* [i] u32 bottom ... end address */
/* [r] u16 ... error code */
/*****************************/
u16 fl_ua_getsum(u16 *sum, u32 top, u32 bottom)
{
    u16 rc;

    /*****************************/
    /* set params */
    /*****************************/
    set_range_prm(fl_cmd_prm, top, bottom); // set SAH/SAM/SAL, EAH/EAM/EAL

    /*****************************/
    /* send command */
    /*****************************/
    fl_wait(tCOM); // wait before sending command

    put_cmd_ua(FL_COM_GET_CHECK_SUM, 7, fl_cmd_prm); // send GET VERSION command

    rc = get_sfrm_ua(fl_rxdata_frm, tWT16_MAX); // get status frame
    switch(rc) {
        case FLC_NO_ERR: break; // continue
        // case FLC_DFTO_ERR: return rc; break; // case [C]
        default: return rc; break; // case [B]
    }

    /*****************************/
    /* get data frame (Checksum data) */
    /*****************************/
    rc = get_dfrm_ua(fl_rxdata_frm, tFD1_MAX); // get status frame
    if (rc){ // if no error,
        return rc; // case [D]
    }

    *sum = (fl_rxdata_frm[OFS_STA_PLD] << 8) + fl_rxdata_frm[OFS_STA_PLD+1]; // set SUM data
    return rc; // case [A]
}
```
6.14 Security Set Command

6.14.1 Processing sequence chart

Security Set command processing sequence

Programmer 78K0R/Kx3

<1> Wait from previous frame reception until next command transmission

<2> Security Set command frame transmission

<3> Time-out check for status frame reception

<4> Status frame reception

<5> Wait from previous frame reception until data frame transmission

<6> Data frame (security data) transmission

<7> Time-out check for status frame reception

<8> Status frame reception

<9> Time-out check for status frame reception

<10> Status frame reception

Abnormal termination [B]

Other than ACK

Time-out error [C]

Abnormal termination [D]

Other than ACK

Abnormal termination [E]

Normal completion [A]

Reception status [ACK/other than ACK]

Status frame received within specified time

Time-out occurs

Time-out occurs

Time-out occurs

Time-out occurs

Time-out occurs

Time-out occurs

Time-out occurs
6.14.2 Description of processing sequence

<1> Waits from the previous frame reception until the next command transmission (wait time \( t_{\text{com}} \)).

<2> The Security Set command is transmitted by command frame transmission processing.

<3> A time-out check is performed from command transmission until status frame reception.
   If a time-out occurs, a time-out error [C] is returned (time-out time \( t_{\text{WT13}}(\text{MAX.}) \)).

<4> The status code is checked.
   
   When ST1 = ACK: Proceeds to <5>.
   When ST1 ≠ ACK: Abnormal termination [B]

<5> Waits from the previous frame reception until the next data frame transmission (wait time \( t_{\text{FD3}} \)).

<6> The data frame (security setting data) is transmitted by data frame transmission processing.

<7> A time-out check is performed until status frame reception.
   If a time-out occurs, a time-out error [C] is returned (time-out time \( t_{\text{WT14}}(\text{MAX.}) \)).

<8> The status code is checked.
   
   When ST1 = ACK: Proceeds to <9>.
   When ST1 ≠ ACK: Abnormal termination [D]

<9> A time-out check is performed until status frame reception.
   If a time-out occurs, a time-out error [C] is returned (time-out time \( t_{\text{WT15}}(\text{MAX.}) \)).

<10> The status code is checked.
   
   When ST1 = ACK: Normal completion [A]
   When ST1 ≠ ACK: Abnormal termination [E]

6.14.3 Status at processing completion

<table>
<thead>
<tr>
<th>Status at Processing Completion</th>
<th>Status Code</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Normal completion [A]</td>
<td>Normal acknowledgment (ACK)</td>
<td>06H</td>
</tr>
<tr>
<td>Abnormal termination [B]</td>
<td>Parameter error</td>
<td>05H</td>
</tr>
<tr>
<td></td>
<td>Checksum error</td>
<td>07H</td>
</tr>
<tr>
<td></td>
<td>Protect error</td>
<td>10H</td>
</tr>
<tr>
<td></td>
<td>Negative acknowledgment (NACK)</td>
<td>15H</td>
</tr>
<tr>
<td>Time-out error [C]</td>
<td>–</td>
<td>The status frame or data frame was not received within the specified time.</td>
</tr>
<tr>
<td>Abnormal termination [D], [E]</td>
<td>MRG10 error</td>
<td>1AH</td>
</tr>
<tr>
<td></td>
<td>MRG11 error</td>
<td>1BH</td>
</tr>
<tr>
<td></td>
<td>Write error</td>
<td>1CH</td>
</tr>
</tbody>
</table>
6.14.4 Flowchart

Security Set command processing

Wait from previous frame reception until next command transmission

Command frame transmission processing (Security Set)

Status frame received?

Yes

Timed out?

No

Yes

Time-out error [C]

Status = ACK?

No

Yes

Abnormal termination [B]

Wait from previous frame reception until next data frame transmission

Data frame transmission processing (Security data)

Status frame received?

Yes

Timed out?

No

Yes

Time-out error [C]

Status = ACK?

No

Yes

Abnormal termination [D]

Status frame received?

No

Wait from previous frame reception until next data frame transmission

Normal completion [A]

No

Status = ACK?

Yes

Time-out error [C]

Yes

Time-out error [C]
6.14.5 Sample program
The following shows a sample program for Security Set command processing.

```c
//*************************************************************************/
/*               */
/* Set security flag command           */
/*               */
/****************************************************************************/
/* [i] u8 scf ... Security flag data          */
/* [r] u16 ... error code           */
/****************************************************************************/

u16  fl_ua_setscf(u8 scf, u8 bot, u8 fsws, u8 fswe)
{
    u16 rc;

    /***********************************************************************
     * set params
    *********************************************************************************/
    fl_cmd_prm[0] = 0x00;   // "BLK" (must be 0x00)
    fl_cmd_prm[1] = 0x00;   // "PAG" (must be 0x00)
    fl_txdata_frm[0] = scf|= 0b11101000; // "FLG" (bit 7,6,5,3 must be '1')
    fl_txdata_frm[1] = bot;   // "BOT"
    fl_txdata_frm[2] = 0x00;   // "FSWS High"
    fl_txdata_frm[3] = fsws;   // "FSWS Low"
    fl_txdata_frm[4] = 0x00;   // "FSWE High"
    fl_txdata_frm[5] = fswe;   // "FSWE Low"

    /*******************************************************************************/
    /* send command */
    /*******************************************************************************/
    fl_wait(tCOM);     // wait before sending command
    put_cmd_ua(FL_COM_SET_SECURITY, 3, fl_cmd_prm);
    rc = get_sfrm_ua(fl_ua_sfrm, tWT13_MAX); // get status frame
    switch(rc) {
        case FLC_NO_ERR:    break; // continue
        // case FLC_DFTO_ERR: return rc;  break; // case [C]
        default:  return rc;  break; // case [B]
    }

    /*******************************************************************************/
    /*    send data frame (security setting data)   */
    /*******************************************************************************/
    fl_wait(tFD4);
    put_dfrm_ua(6, fl_txdata_frm, true);  // send security setting data
    rc = get_sfrm_ua(fl_ua_sfrm, tWT14_MAX); // get status frame
    rc = get_sfrm_ua(fl_ua_sfrm, tWT14_MAX+100); // get status frame (+100us is overhead)
    switch(rc) {
        case FLC_NO_ERR: break; // continue
        // case FLC_DFTO_ERR: return rc; break; // case [C]
```
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    default: return rc; break; // case [B]

}  

/***********************************************************/  
/* Check internally verify */  
/***********************************************************/  
rc = get_sfrm_ua(fl ua_sfrm, tWT15_MAX);  // get status frame  
switch(rc) {
    //  
    //      case FLC_NO_ERR: return rc; break; // case [A]  
    //      case FLC_DFTO_ERR: return rc; break; // case [C]  
    //      default: return rc; break; // case [B]  
    // }
return rc;
}
CHAPTER 7  FLASH MEMORY PROGRAMMING PARAMETER CHARACTERISTICS

This chapter describes the parameter characteristics between the programmer and the 78K0R/Kx3 in the flash memory programming mode.
Be sure to refer to the user’s manual of the 78K0R/Kx3 for electrical specifications when designing a programmer.

(1) Flash memory parameter characteristics

(a) Flash memory programming mode setting time

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>MIN.</th>
<th>TYP.</th>
<th>MAX.</th>
</tr>
</thead>
<tbody>
<tr>
<td>VDD↑ to FLMD0↑</td>
<td>tDP</td>
<td>0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>FLMD0↑ to RESET↑</td>
<td>tPR</td>
<td>2 ms</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Ready start time from RESET↑</td>
<td>tR0</td>
<td>3 ms</td>
<td>100 ms</td>
<td></td>
</tr>
<tr>
<td>Low level data0 (Ready) width</td>
<td>tL0</td>
<td>892 μs</td>
<td>937.5 μs</td>
<td>987 μs</td>
</tr>
<tr>
<td>Wait for low level data1</td>
<td>tL0</td>
<td>120 μs</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Wait for low level data2</td>
<td>tL1</td>
<td>10 μs</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Wait for Read command</td>
<td>tL2</td>
<td>300 μs</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Low level data1/data2 width</td>
<td>tL1, tL2</td>
<td>937.5 μs</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Note** The low-level width is the same as the 00H data width at 9,600 bps. (It includes the start bit and is therefore “0” data of 9 bits.)
tL0 is the low-level width of the data transmitted from the 78K0R/Kx3 firmware. tL1 and tL2 are the low-level widths of the data transmitted from the flash programmer.
(b) Programming characteristics

<table>
<thead>
<tr>
<th>Wait</th>
<th>Condition</th>
<th>Symbol</th>
<th>MIN.</th>
<th>MAX.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Between data frame transmissions</td>
<td>Data frame reception</td>
<td>tDR</td>
<td>8.0 µs</td>
<td></td>
</tr>
<tr>
<td>Data frame transmission</td>
<td></td>
<td>tDT</td>
<td></td>
<td>Note</td>
</tr>
<tr>
<td>From status frame transmission until data frame</td>
<td>–</td>
<td>tFD1</td>
<td></td>
<td>Note</td>
</tr>
<tr>
<td>transmission</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>From status frame transmission until data frame</td>
<td>Program command</td>
<td>tFD2</td>
<td>8.7 µs</td>
<td></td>
</tr>
<tr>
<td>reception (1)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>From status frame transmission until data frame</td>
<td>Verify command</td>
<td>tFD3</td>
<td>145 µs</td>
<td></td>
</tr>
<tr>
<td>reception (2)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>From status frame transmission until data frame</td>
<td>Security setting command</td>
<td>tFD4</td>
<td>120 µs</td>
<td></td>
</tr>
<tr>
<td>reception (3)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>From status frame transmission until command</td>
<td>–</td>
<td>tCOM</td>
<td>595 µs</td>
<td></td>
</tr>
<tr>
<td>frame reception</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Note** Enable successive reception for the programmer. Also, set the time-out time for the programmer to 3 seconds or more.

**Remark** The waits are defined as follows.

<\text{tDR}, \text{tFD2}, \text{tFD3}, \text{tFD4}, \text{tCOM}>

The 78K0R/Kx3 is readied for the next communication after the MIN. time has elapsed after completion of the previous communication.

<\text{tDT}, \text{tFD1}>

The 78K0R/Kx3 is readied for the next communication after the MIN. time has elapsed after completion of the previous communication.
### Command characteristics

<table>
<thead>
<tr>
<th>Command</th>
<th>Symbol</th>
<th>Condition</th>
<th>MIN.</th>
<th>MAX.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Reset</td>
<td>$t_{WT0}$</td>
<td>–</td>
<td>Note 1</td>
<td></td>
</tr>
<tr>
<td>Chip Erase</td>
<td>$t_{WT1}$</td>
<td>Product group A$^{\text{Note }2}$ $(60.6 + 5.7 \times \text{total number of blocks})$ ms</td>
<td>$(1112 + 140.9 \times \text{total number of blocks})$ ms</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Product group B$^{\text{Note }3}$ $(812.9 + 5.7 \times (\text{total number of blocks} - 128))$ ms</td>
<td>$(19403.5 + 140.9 \times (\text{total number of blocks} - 128))$ ms</td>
<td></td>
</tr>
<tr>
<td>Block Erase</td>
<td>$t_{WT2}$ $^{\text{Note }4}$</td>
<td>–</td>
<td>17.5 ms</td>
<td>$(1.1 + 275.5 \times \text{execution count of simultaneous selection and erasure} + 137.9 \times \text{number of blocks to be erased})$ ms</td>
</tr>
<tr>
<td>Programming</td>
<td>$t_{WT3}$</td>
<td>–</td>
<td>Note 1</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$t_{WT4}$ $^{\text{Note }5}$</td>
<td>–</td>
<td>2.8 ms</td>
<td>47.2 ms</td>
</tr>
<tr>
<td></td>
<td>$t_{WT5}$ $^{\text{Note }6}$</td>
<td>Block 0</td>
<td>13.3 ms</td>
<td>860.0 ms</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Other than block 0</td>
<td>13.3 ms</td>
<td>16.3 ms</td>
</tr>
<tr>
<td>Verify</td>
<td>$t_{WT6}$</td>
<td>–</td>
<td>Note 1</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$t_{WT7}$ $^{\text{Note }8}$</td>
<td>–</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Block Blank Check</td>
<td>$t_{WT8}$ $^{\text{Note }10}$</td>
<td>–</td>
<td>5.7 ms</td>
<td>7.7 ms</td>
</tr>
<tr>
<td>Baud Rate Set</td>
<td>$t_{WT9}$</td>
<td>–</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Silicon Signature</td>
<td>$t_{WT10}$</td>
<td>–</td>
<td>66.0 μs</td>
<td></td>
</tr>
<tr>
<td>Version Get</td>
<td>$t_{WT11}$</td>
<td>–</td>
<td>Note 1</td>
<td></td>
</tr>
<tr>
<td>Security Set</td>
<td>$t_{WT12}$</td>
<td>–</td>
<td>Note 1</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$t_{WT13}$</td>
<td>–</td>
<td>Note 1</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$t_{WT14}$</td>
<td>–</td>
<td>Note 1</td>
<td>20.0 μs</td>
</tr>
<tr>
<td></td>
<td>$t_{WT15}$</td>
<td>–</td>
<td>Note 8</td>
<td>843.7 ms</td>
</tr>
<tr>
<td>Checksum</td>
<td>$t_{WT16}$</td>
<td>–</td>
<td>Note 1</td>
<td></td>
</tr>
</tbody>
</table>

**Notes**

1. Reception must be enabled for the programmer before command frame transmission. Also, set the time-out time for the programmer to 3 seconds or more.
2. Product group A: Flash size ≤ 256 KB (number of blocks ≤ 128)
3. Product group B: Flash size > 256 KB (number of blocks > 128)
4. See (2) Simultaneous selection and erasure performed by Block Erase command for the calculation method of the execution count of simultaneous selection and erasure.
5. Time for 256-byte data transmission
6. Time for one block transmission
7. Reception must be enabled for the programmer before data frame transmission. Also, set the time-out time for the programmer to 3 seconds or more.
8. Enable successive reception for the programmer. Also, set the time-out time for the programmer to 3 seconds or more.

(A Remark is on the next page.)
Remark  The waits are defined as follows.

\(<t_{WT0} \text{ to } t_{WT8}, \ t_{WT11} \text{ to } t_{WT16}>\)

The 78K0R/Kx3 completes command processing between the MIN. and MAX. times and transmits a status frame.

For commands with a specified MAX. time, the programmer must wait for the start bit of the reception frame until the MAX. time has elapsed and then perform time-out processing.

See the corresponding note for commands without a specified MAX. time.

\(<t_{WT10}>\)

The 78K0R/Kx3 can perform the next communication after MIN., after the communication immediately before has been completed.

The programmer must transmit the next data after the MIN. time elapses, after the communication immediately before has been completed.
(2) **Simultaneous selection and erasure performed by Block Erase command**

The Block Erase command of the 78K0R/Kx3 is executed by repeating "simultaneous selection and erasure", which erases multiple blocks simultaneously.

The wait time inserted during Block Erase command execution is therefore equal to the total execution time of "simultaneous selection and erasure".

To calculate the "total execution time of simultaneous selection and erasure", the execution count (M) of the simultaneous selection and erasure must first be calculated.

"M" is calculated by obtaining the number of blocks to be erased simultaneously (number of blocks to be selected and erased simultaneously).

The following describes the method for calculating the number of blocks to be selected and erased simultaneously and the execution count (M).

(a) **Calculation of number of blocks to be selected and erased simultaneously**

The number of blocks to be selected and erased simultaneously should be 1, 2, 4, 8, 16, 32, 64, or 128, depending on which satisfies all of the following conditions.

- **[Condition 1]**
  
  \[(\text{Number of blocks to be erased}) \geq (\text{Number of blocks to be selected and erased simultaneously})\]

- **[Condition 2]**
  
  \[(\text{Start block number}) \div (\text{Number of blocks to be selected and erased simultaneously}) = \text{Remainder is 0}\]

- **[Condition 3]**
  
  The maximum value among the values that satisfy both Conditions 1 and 2
(b) Calculation of the execution count (M) of simultaneous selection and erasure

Calculation of the execution count (M) is illustrated in the following flowchart.

**Start**

\[ \text{ER_BKNUM} \leftarrow \text{END_BKNO} - \text{ST_BKNO} + 1 \]

\[ \text{M} \leftarrow 0 \]

\[ \text{SSER_BKNUM} \leftarrow 128 \]

- **Condition 1**: ER_BKNUM ≥ SSER_BKNUM?
- **Condition 2**: ST_BKNO = SSER_BKNUM = Remainder is 0?

**Note** Based on the maximum value of SSER_BKNUM (128), obtain the value that satisfies Conditions 1 and 2 by executing SSER_BKNUM ÷ 2; Condition 3 is then satisfied.
Example 1  Erasing blocks 1 to 127 (N (number of blocks to be erased) = 127)

<1> The first start block number is 1 and the number of blocks to be erased is 127; the values that satisfy Condition 1 are therefore 1, 2, 4, 8, 16, 32, 64, and 128. Moreover, the value that satisfies Condition 2 is 1 and the value that satisfies Condition 3 is 1, so the number of blocks to be selected and erased simultaneously is 1; only block 1 is then erased.

<2> After block 1 is erased, the next start block number is 2 and the number of blocks to be erased is 126; the values that satisfy Condition 1 are therefore 1, 2, 4, 8, 16, 32, and 64. Moreover, the values that satisfy Condition 2 are 1 and 2, the value that satisfies Condition 3 is 2, so the number of blocks to be selected and erased simultaneously is 2; blocks 2 and 3 are then erased.

<3> After blocks 2 and 3 are erased, the next start block number is 4 and the number of blocks to be erased is 124; the values that satisfy Condition 1 are therefore 1, 2, 4, 8, 16, 32, and 64. Moreover, the values that satisfy Condition 2 are 1, 2, and 4, the value that satisfies Condition 3 is 4, so the number of blocks to be selected and erased simultaneously is 4; blocks 4 to 7 are then erased.

<4> After blocks 4 to 7 are erased, the next start block number is 8 and the number of blocks to be erased is 120; the values that satisfy Condition 1 are therefore 1, 2, 4, 8, 16, 32, and 64. Moreover, the values that satisfy Condition 2 are 1, 2, 4, and 8, the value that satisfies Condition 3 is 8, so the number of blocks to be selected and erased simultaneously is 8; blocks 8 to 15 are then erased.

<5> After blocks 8 to 15 are erased, the next start block number is 16 and the number of blocks to be erased is 112; the values that satisfy Condition 1 are therefore 1, 2, 4, 8, 16, 32, and 64. Moreover, the values that satisfy Condition 2 are 1, 2, 4, 8, 16, and 32, the value that satisfies Condition 3 is 16, so the number of blocks to be selected and erased simultaneously is 16; blocks 16 to 31 are then erased.

<6> After blocks 16 to 31 are erased, the next start block number is 32 and the number of blocks to be erased is 96; the values that satisfy Condition 1 are therefore 1, 2, 4, 8, 16, 32, and 64. Moreover, the values that satisfy Condition 2 are 1, 2, 4, 8, 16, and 32, the value that satisfies Condition 3 is 32, so the number of blocks to be selected and erased simultaneously is 32; blocks 32 to 63 are then erased.

<7> After blocks 32 to 63 are erased, the next start block number is 64 and the number of blocks to be erased is 64; the values that satisfy Condition 1 are therefore 1, 2, 4, 8, 16, 32, and 64. Moreover, the values that satisfy Condition 2 are 1, 2, 4, 8, 16, 32, and 64, the value that satisfies Condition 3 is 64, so the number of blocks to be selected and erased simultaneously is 64; blocks 64 to 127 are then erased.

Therefore, simultaneous selection and erasure is executed seven times (1, 2 and 3, 4 to 7, 8 to 15, 16 to 31, 32 to 63, and 64 to 127) to erase blocks 1 to 127, so M = 7 is obtained.
Block configuration when executing simultaneous selection and erasure (when erasing blocks 1 to 127)

<Range of blocks that can be selected and erased simultaneously>
Example 2  Erasing blocks 5 to 10 (N (number of blocks to be erased) = 6)

<1> The first start block number is 5 and the number of blocks to be erased is 6; the values that satisfy Condition 1 are therefore 1, 2, and 4.
Moreover, the value that satisfies Condition 2 is 1 and the value that satisfies Condition 3 is 1, so the number of blocks to be selected and erased simultaneously is 1; only block 5 is the erased.

<2> After block 5 is erased, the next start block number is 6 and the number of blocks to be erased is 5; the values that satisfy Condition 1 are therefore 1, 2, and 4.
Moreover, the values that satisfy Condition 2 are 1 and 2, the value that satisfies Condition 3 is 2, so the number of blocks to be selected and erased simultaneously is 2; blocks 6 and 7 are then erased.

<3> After blocks 6 and 7 are erased, the next start block number is 8 and the number of blocks to be erased is 3; the values that satisfy Condition 1 are therefore 1 and 2.
Moreover, the values that satisfy Condition 2 are 1 and 2, the value that satisfies Condition 3 is 2, so the number of blocks to be selected and erased simultaneously is 2; blocks 8 and 9 are then erased.

<4> After blocks 8 and 9 are erased, the next start block number is 10 and the number of blocks to be erased is 1; the value that satisfies Condition 1 is therefore 1. This also satisfies Conditions 2 and 3, so the number of blocks to be selected and erased simultaneously is 1; block 10 is then erased.

Therefore, simultaneous selection and erasure is executed four times (5, 6 and 7, 8 and 9, and 10) to erase blocks 5 to 10, so \( M = 4 \) is obtained.
Block configuration when executing simultaneous selection and erasure (when erasing blocks 5 to 10)

User area

<Range of blocks that can be selected and erased simultaneously>
Example 3  Erasing blocks 25 to 73 (N (number of blocks to be erased) = 49)

<1> The first start block number is 25 and the number of blocks to be erased is 49; the values that satisfy Condition 1 are therefore 1, 2, 4, 8, 16, and 32. Moreover, the value that satisfies Condition 2 is 1 and the value that satisfies Condition 3 is 1, so the number of blocks to be selected and erased simultaneously is 1; only block 25 is then erased.

<2> After block 25 is erased, the next start block number is 26 and the number of blocks to be erased is 48; the values that satisfy Condition 1 are therefore 1, 2, 4, 8, 16, and 32. Moreover, the values that satisfy Condition 2 are 1 and 2, the value that satisfies Condition 3 is 2, so the number of blocks to be selected and erased simultaneously is 2; blocks 26 and 27 are then erased.

<3> After blocks 26 and 27 are erased, the next start block number is 28 and the number of blocks to be erased is 46; the values that satisfy Condition 1 are therefore 1, 2, 4, 8, 16, and 32. Moreover, the values that satisfy Condition 2 are 1, 2, and 4, the value that satisfies Condition 3 is 4, so the number of blocks to be selected and erased simultaneously is 4; blocks 28 to 31 are then erased.

<4> After blocks 28 to 31 are erased, the next start block number is 32 and the number of blocks to be erased is 42; the values that satisfy Condition 1 are therefore 1, 2, 4, 8, 16, and 32. Moreover, the values that satisfy Condition 2 are 1, 2, 4, 8, and 32, the value that satisfies Condition 3 is 32, so the number of blocks to be selected and erased simultaneously is 32; blocks 32 to 63 are then erased.

<5> After blocks 32 to 63 are erased, the next start block number is 64, and the number of blocks to be erased is 10; the values that satisfy Condition 1 are therefore 1, 2, 4, and 8. Moreover, the values that satisfy Condition 2 are 1, 2, 4, and 8, the value that satisfies Condition 3 is 8, so the number of blocks to be selected and erased simultaneously is 8; blocks 64 to 71 are then erased.

<6> After blocks 64 to 71 are erased, the next start block number is 72, and the number of blocks to be erased is 2; the values that satisfy Condition 1 are therefore 1 and 2. Moreover, the values that satisfy Condition 2 are 1 and 2, the value that satisfies Condition 3 is 2, so the number of blocks to be selected and erased simultaneously is 2; blocks 72 and 73 are then erased.

Therefore, simultaneous selection and erasure is executed six times (25, 26 and 27, 28 to 31, 32 to 63, 64 to 71, and 72 and 73) to erase blocks 25 to 73, so M = 6 is obtained.
Block configuration when executing simultaneous selection and erasure (when erasing blocks 25 to 73)
(3) UART communication mode

(a) Data frame

Remark In the above figure, TOOL0 is illustrated as two separate lines for the sake of description, but it is actually a single line. The VDD level of TOOL0 can be achieved by using a pull-up resistor (the pin is Hi-Z).

(b) Programming mode setting/Reset command

Remark In the above figure, TOOL0 is illustrated as two separate lines for the sake of description, but it is actually a single line. The VDD level of TOOL0 can be achieved by using a pull-up resistor (the pin is Hi-Z).

(c) Chip Erase command/Block Erase command/Block Blank Check command/Oscillating Frequency Set command

Remark The descriptions in parentheses indicate operations of the 78K0R/Kx3.
(d) **Baud Rate Set command**

**Command frame**
- **(Reception)**
- **(Transmission)**

**Remark** The descriptions in parentheses indicate operations of the 78K0R/Kx3.

(e) **Silicon Signature command/Version Get command**

**Command frame**
- **(Reception)**
- **(Transmission)**

**Data frame**
- **(Transmission)**

**Remark** The descriptions in parentheses indicate operations of the 78K0R/Kx3.

(f) **Checksum command**

**Command frame**
- **(Reception)**
- **(Transmission)**

**Data frame**
- **(Transmission)**

**Remark** The descriptions in parentheses indicate operations of the 78K0R/Kx3.

(g) **Programming command**

**Command frame**
- **(Reception)**

**Status frame**
- **(Transmission)**
- **(Reception)**

**Data frame**
- **(Transmission)**
- **(Transmission)**
- **(Transmission)**

**Remark** The descriptions in parentheses indicate operations of the 78K0R/Kx3.
(h) Verify command

Remark  The descriptions in parentheses indicate operations of the 78K0R/Kx3.

(i) Security Set command

Remark  The descriptions in parentheses indicate operations of the 78K0R/Kx3.

(j) Wait before command frame transmission

Remark  The descriptions in parentheses indicate operations of the 78K0R/Kx3.
[MEMO]
APPENDIX A CIRCUIT DIAGRAMS (REFERENCE)

Figures A-1 and A-2 show circuit diagrams of the programmer and the 78K0R/Kx3, for reference.
Figure A-1. Reference Circuit Diagram of Programmer and 78K0R/Kx3 (Main Board)
78K0R/Kx3 Flash programmer sample application - TARGET BOARD

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