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RENESAS

Application Note

78K0/Kx2-L

Sample Program (Operational Amplifier)

Amplifying Analog Voltages in Single-Amplifier Mode

This document describes an operation overview of the sample program and how to use it, as well as how to set up and use the operational amplifier. In the sample program, a non-inverting amplifier is set up by using operational amplifier 0 in the single-amplifier mode, the amplified analog voltage is A/D converted using the A/D converter, and then the conversion results and the average of four conversion results are saved in the RAM area.

Target devices
78K0/KY2-L microcontroller
78K0/KA2-L microcontroller
78K0/KB2-L microcontroller
78K0/KC2-L microcontroller

CONTENTS

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CHAPTER 1 OVERVIEW

An example of using the operational amplifier is presented in this sample program. A non-inverting amplifier is set up by using operational amplifier 0 in the single-amplifier mode, the amplified analog voltage is A/D converted using the A/D converter, and then the conversion results and the average of four conversion results are saved in the RAM area.

1.1 Primary Initial Settings

The primary initial settings are as follows:

<Option byte settings>

- Allowing the internal low-speed oscillator to be programmed to stop
- Disabling the watchdog timer
- Setting the internal high-speed oscillation clock frequency to 8 MHz
- Disabling LVI from being started by default

<Settings during initialization immediately after a reset ends>

- Specifying the ROM and RAM sizes
- Setting up I/O ports
  - Specifying the P20/AMP0-, P21/AMP0OUT, and P22/AMP0+ pins as analog input pins
- Checking whether V_{DD} is 2.7 V or more by using the low-voltage detector[Note 1]
- Specifying that the CPU clock and peripheral hardware clock run on the internal high-speed oscillation clock (8 MHz)
- Stopping the internal low-speed oscillator
- Disabling peripheral hardware not to be used
- Specifying single-amplifier mode for operational amplifier 0
- Setting up the A/D converter[Note 1]
  - Specifying the standard mode as the operating mode and 264/f_{PRS} (about 33 μs) as the conversion time
  - Specifying ANI1[Note 2] as the analog input channel
  - Enabling the INTAD interrupt for exiting the HALT mode during A/D conversion

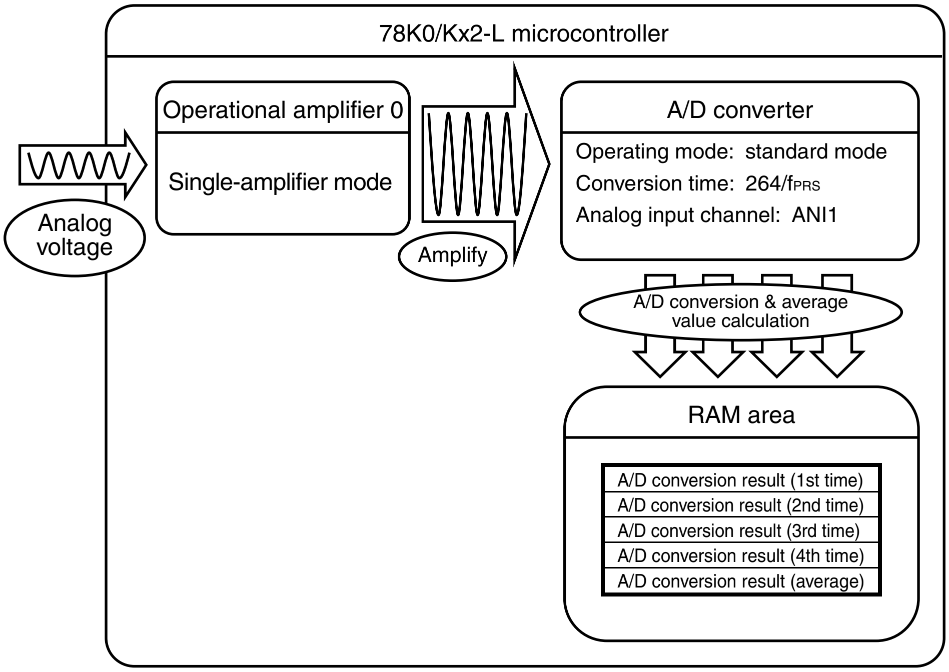
Notes 1. For details about the low-voltage detector and A/D converter, refer to the 78K0/Kx2-L User's Manual.

2. Analog input pin ANI1 of the A/D converter is alternately used as the AMP0OUT pin of operational amplifier 0. By specifying ANI1 as the analog input channel of the A/D converter, the analog voltage amplified by using operational amplifier 0 in the single-amplifier mode can be input to the A/D converter.

1.2 Processing After Main Loop

After the initial settings have been specified, A/D conversion starts, the amplified analog voltage from the AMP0+ pin is input to ANI1 and A/D converted four times, the correction value for the input offset voltage of operational amplifier 0 is added to the conversion results, and then the results are saved in the RAM area. After the four conversion results are saved, A/D conversion is stopped. After A/D conversion is stopped, the average of four A/D conversion results is calculated and saved in the RAM area.

[Operation overview]

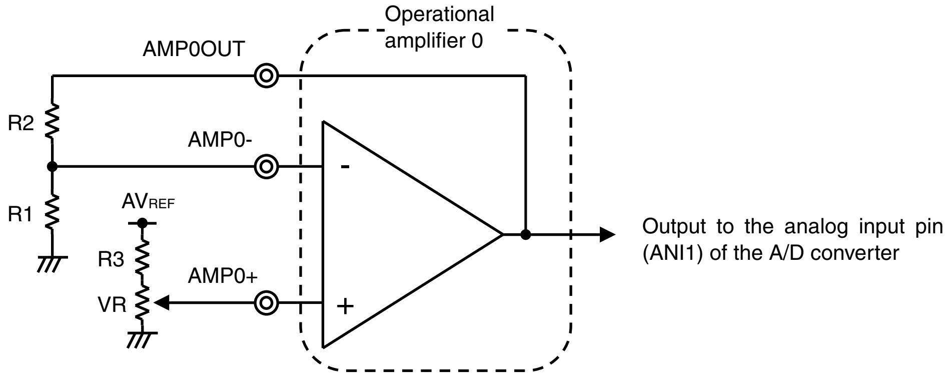

78K0/Kx2-L microcontroller
Operational amplifier 0
Single-amplifier mode
Analog voltage
Amplify
A/D converter
Operating mode: standard mode
Conversion time: 264/fPRS
Analog input channel: ANI1
A/D conversion & average value calculation
RAM area
A/D conversion result (1st time)
A/D conversion result (2nd time)
A/D conversion result (3rd time)
A/D conversion result (4th time)
A/D conversion result (average)

1.3 Single-Amplifier Mode

(1) Example of using the single-amplifier mode

By using operational amplifier 0 in the single-amplifier mode, two input pins (the AMP0- and AMP0+ pins) and one output pin (the AMP0OUT pin) can be used to enable operational amplifier 0 to be used as a single-power-supply amplifier that can be connected externally. Because the AMP0OUT pin is alternately used as the analog input pin of the A/D converter (ANI1), the amplified voltage can be input to the A/D converter.

An example of using the single-amplifier mode is shown below.



In the figure above, the analog voltage from the variable resistor (VR) connected to the AMP0+ pin is amplified by ((R2 + R1)/R1) and then output to the analog input pin (ANI1) of the A/D converter. To use operational amplifier 0 in the single-amplifier mode, specify the resistance of R1 and R2 in accordance with the target gain. In this sample program, R1 is 1 kΩ and R2 is 9.1 kΩ, so the gain is about tenfold.

Caution In this sample program, a voltage greater than AV_{REF}/10 does not need to be input to the AMP0+ pin because the gain is assumed to be about tenfold. Therefore, by connecting R3 (9.1 kΩ) between VR (1 kΩ) and AV_{REF}, the analog voltage input to the AMP0+ pin is set to be in the range from V_{SS} to AV_{REF}/10.

(2) Input offset voltage

An input offset voltage of up to ±10 mV is generated for operational amplifier 0. Therefore, the target output voltage (the analog voltage input to the AMP0+ pin × gain) differs from the actual output voltage. Therefore, when performing A/D conversion on the output of operational amplifier 0, the A/D conversion results must be corrected in accordance with the input offset voltage.

In this sample program, a correction value of –5[Note] is added to the A/D conversion results to handle the effects of the input offset voltage.

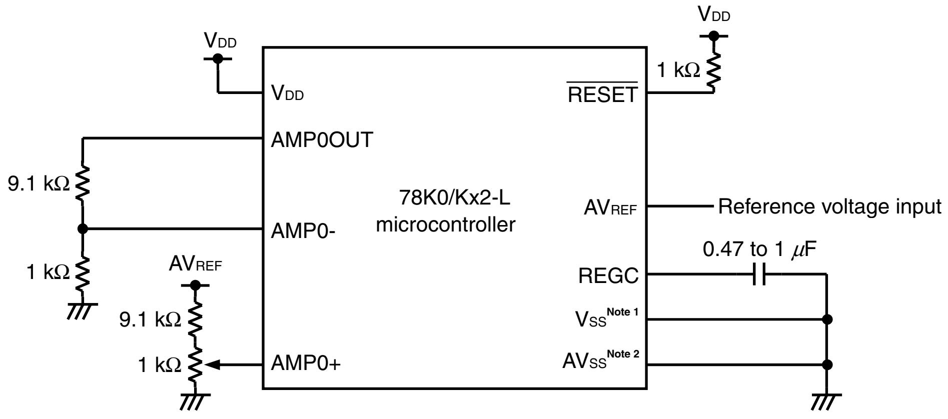
Note The input offset voltage varies depending on the device used and the operating environment. When adding a correction value to the A/D conversion results, adjust the correction value in accordance with the input offset voltage.

CHAPTER 2 CIRCUIT DIAGRAM

This chapter provides a circuit diagram used in this sample program.

2.1 Circuit Diagram

A circuit diagram is shown below.



Notes 1. This is shared with AVSS in the 78K0/KY2-L and 78K0/KA2-L.

2. This is provided only in the 78K0/KB2-L and 78K0/KC2-L.

Cautions 1. Use the microcontroller at a voltage in the range of 2.94 V ≤ VDD ≤ 5.5 V.

2. Connect REGC to VSS via a capacitor (0.47 to 1 μF).

3. For the 78K0/KY2-L and 78K0/KA2-L, VSS is also used as the ground potential for the A/D converter. Be sure to connect VSS to a stable GND.

4. Make the AVSS pin have the same potential as VSS and connect it directly to GND (only for the 78K0/KB2-L and 78K0/KC2-L microcontrollers).

5. Make sure that the AVREF voltage is 2.7 V or more, 5.5 V or less, and VDD or less.

6. Handle unused pins that are not shown in the circuit diagram as follows:

- **I/O ports: Set them to output mode and leave them open (unconnected).**
- **Input ports: Connect them independently to VDD or VSS via a resistor.**

7. In this sample program, the P121/X1/TOOLC0 and P122/X2/EXCLK/TOOLD0 pins are used for on-chip debugging.

8. For details about the resistance of the resistors to connect to the AMP0+, AMP0-, and AMP0OUT pins, refer to 1.3 Single-Amplifier Mode.

CHAPTER 3 SOFTWARE

This chapter describes the files included in the compressed file to be downloaded, internal peripheral functions of the microcontroller to be used, and initial settings and provides an operation overview of the sample program and the flow charts.

3.1 Included Files

The following table shows the files included in the compressed file to be downloaded.

File Name	Description	Compressed (*.zip) File Included	
		ZIP	PM 32
main.asm (Assembly language version) main.c (C language version)	Source file for hardware initialization processing and main processing of microcontroller	●[Note]	●[Note]
op.asm	Assembler source file for setting the option byte (This file is used for setting up the watchdog timer and internal low-speed oscillator and selecting the internal high-speed oscillation clock frequency.)	●	●
Kx2-L_AMP.prw	Work space file for integrated development environment PM+		●
Kx2-L_AMP.prj	Project file for integrated development environment PM+		●

Note "main.asm" is included with the assembly language version, and "main.c" with the C language version.

Remark ZIP : Only the source file is included.

PM 32 : The files to be used with integrated development environment PM+ are included.

3.2 Internal Peripheral Functions to Be Used

The following internal peripheral functions of the microcontroller are used in this sample program.

(1) Peripheral hardware

- Operational amplifier 0: Used to amplify the analog voltage.
- A/D converter: Performs 10-bit resolution A/D conversion.
- Low-voltage detector: Used to check that V_{DD} is 2.7 V or more.

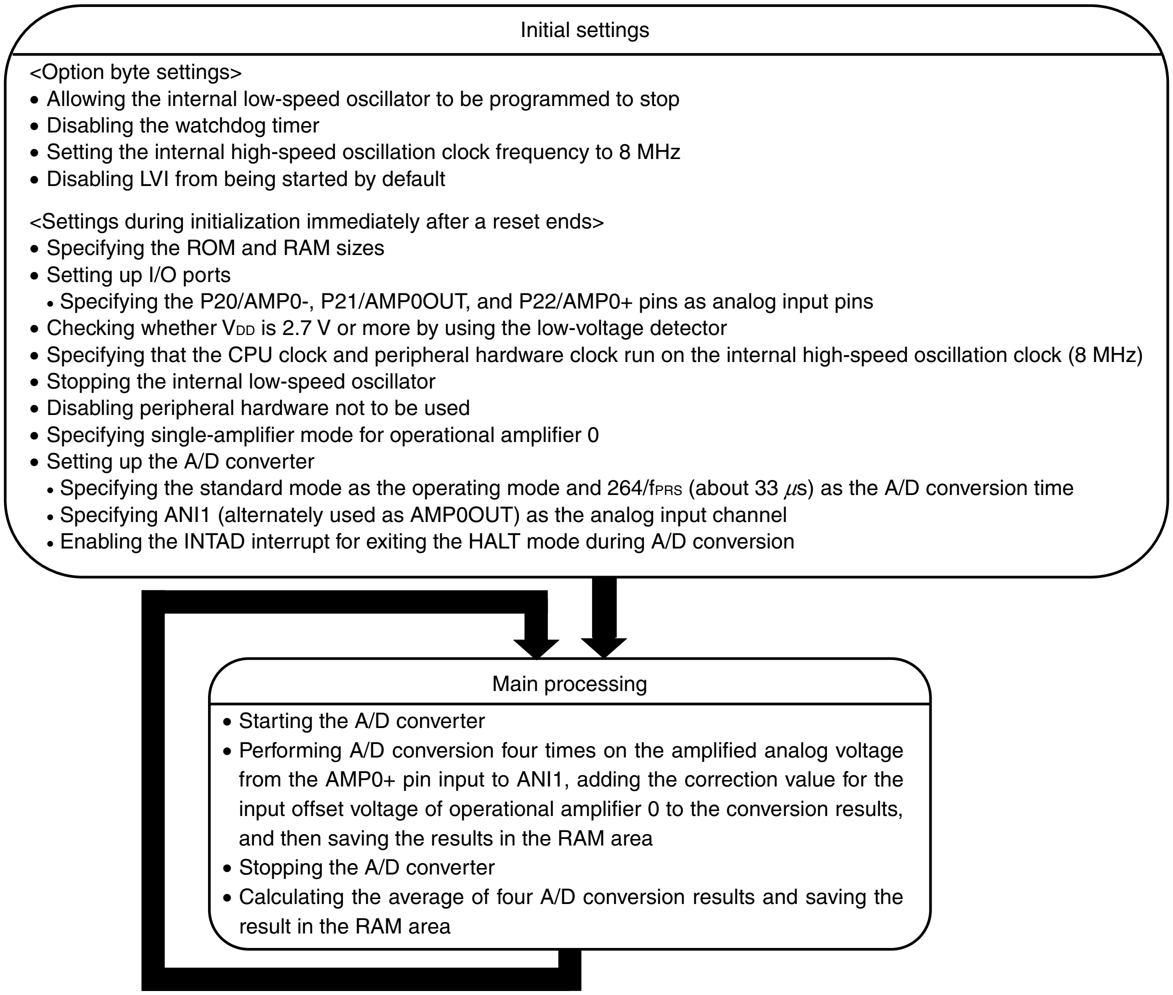
(2) Pins

- P20/AMP0-: Used as the inverted input of operational amplifier 0.
- P21/AMP0OUT: Used as the output of operational amplifier 0.
- P22/AMP0+: Used as the non-inverted input of operational amplifier 0.

3.3 Initial Settings and Operation Overview

In this sample program, initial settings including the selection of the clock frequency, setting of the I/O ports, and setting of operational amplifier 0 are performed. After the initial settings have been specified, A/D conversion starts, the amplified analog voltage from the AMP0+ pin is input to ANI1 and A/D converted four times, the correction value for the input offset voltage of operational amplifier 0 is added to the conversion results, and then the results are saved in the RAM area. After the four conversion results are saved, A/D conversion is stopped. After A/D conversion is stopped, the average of four A/D conversion results is calculated and saved in the RAM area.

The details are described in the status transition diagram shown below.



Initial settings

<Option byte settings>

- Allowing the internal low-speed oscillator to be programmed to stop
- Disabling the watchdog timer
- Setting the internal high-speed oscillation clock frequency to 8 MHz
- Disabling LVI from being started by default

<Settings during initialization immediately after a reset ends>

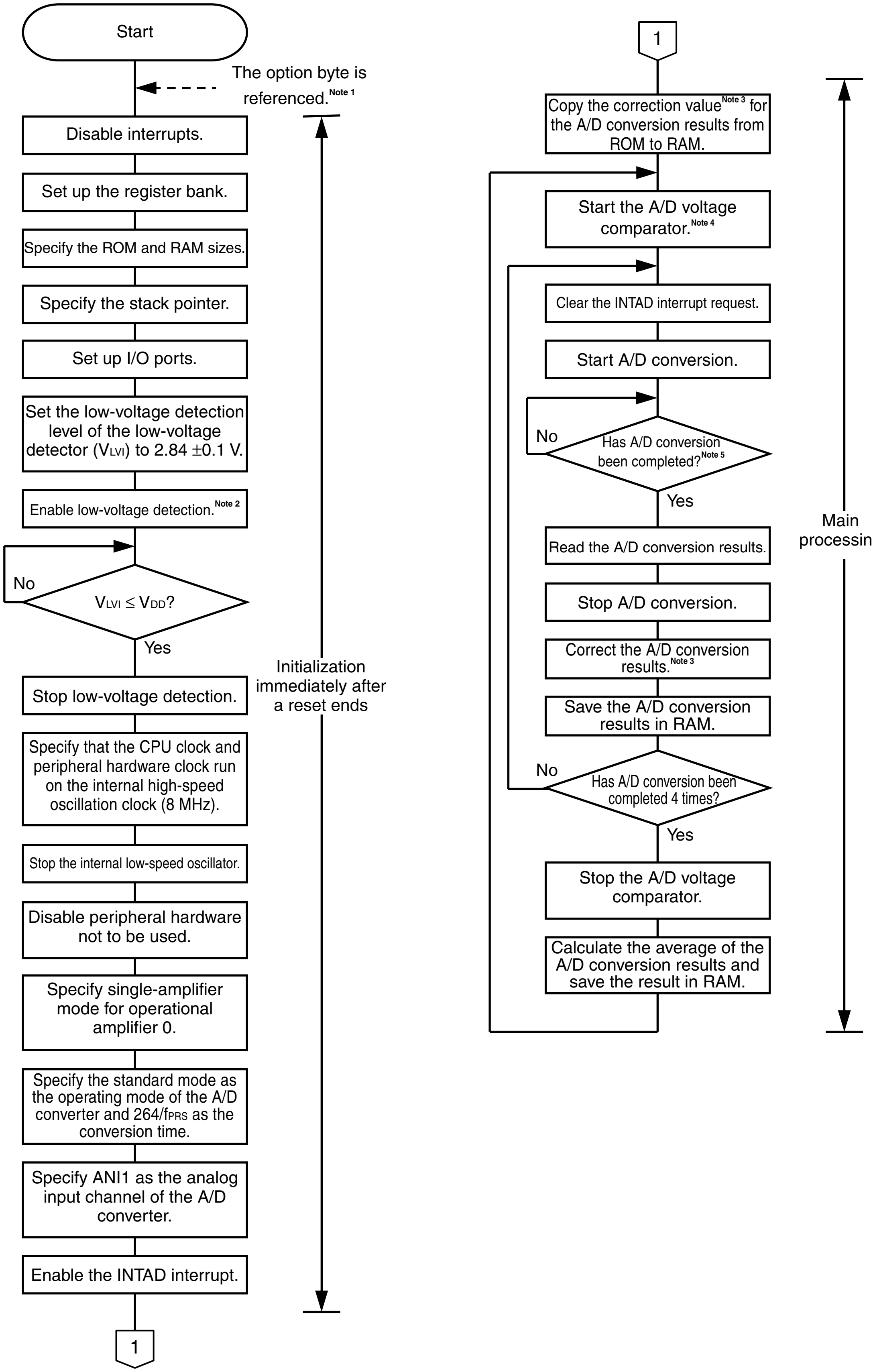
- Specifying the ROM and RAM sizes
- Setting up I/O ports
  - Specifying the P20/AMP0-, P21/AMP0OUT, and P22/AMP0+ pins as analog input pins
- Checking whether V_{DD} is 2.7 V or more by using the low-voltage detector
- Specifying that the CPU clock and peripheral hardware clock run on the internal high-speed oscillation clock (8 MHz)
- Stopping the internal low-speed oscillator
- Disabling peripheral hardware not to be used
- Specifying single-amplifier mode for operational amplifier 0
- Setting up the A/D converter
  - Specifying the standard mode as the operating mode and $264/f_{PRS}$ (about 33 μs) as the A/D conversion time
  - Specifying ANI1 (alternately used as AMP0OUT) as the analog input channel
  - Enabling the INTAD interrupt for exiting the HALT mode during A/D conversion

Main processing

- Starting the A/D converter
- Performing A/D conversion four times on the amplified analog voltage from the AMP0+ pin input to ANI1, adding the correction value for the input offset voltage of operational amplifier 0 to the conversion results, and then saving the results in the RAM area
- Stopping the A/D converter
- Calculating the average of four A/D conversion results and saving the result in the RAM area

3.4 Flow Charts

The flow charts for the sample program are shown below.


Start
The option byte is referenced.Note 1
Disable interrupts.
Set up the register bank.
Specify the ROM and RAM sizes.
Specify the stack pointer.
Set up I/O ports.
Set the low-voltage detection level of the low-voltage detector (V_{LVI}) to 2.84 ±0.1 V.
Enable low-voltage detection.Note 2
No
$V_{LVI} \leq V_{DD}$?
Yes
Stop low-voltage detection.
Specify that the CPU clock and peripheral hardware clock run on the internal high-speed oscillation clock (8 MHz).
Stop the internal low-speed oscillator.
Disable peripheral hardware not to be used.
Specify single-amplifier mode for operational amplifier 0.
Specify the standard mode as the operating mode of the A/D converter and 264/f_{PRS} as the conversion time.
Specify ANI1 as the analog input channel of the A/D converter.
Enable the INTAD interrupt.
1
Initialization immediately after a reset ends
1
Copy the correction valueNote 3 for the A/D conversion results from ROM to RAM.
Start the A/D voltage comparator.Note 4
Clear the INTAD interrupt request.
Start A/D conversion.
No
Has A/D conversion been completed?Note 5
Yes
Read the A/D conversion results.
Stop A/D conversion.
Correct the A/D conversion results.Note 3
Save the A/D conversion results in RAM.
No
Has A/D conversion been completed 4 times?
Yes
Stop the A/D voltage comparator.
Calculate the average of the A/D conversion results and save the result in RAM.
Main processing

Notes 1. The option byte is automatically referenced by the microcontroller immediately after a reset ends. In this sample program, the following settings are specified using the option byte:

- Allowing the internal low-speed oscillator to be programmed to stop
- Disabling the watchdog timer
- Setting the internal high-speed oscillation clock frequency to 8 MHz
- Disabling LVI from being started by default

2. The low-voltage detector is enabled, and then the system is made to wait at least 10 μs until the low-voltage detector stabilizes.

3. A correction value of –5 is added to the A/D conversion results to handle the effects of the input offset voltage of operational amplifier 0.

4. A/D conversion starts after the system waits for 1 μs until operation stabilizes after the A/D voltage comparator is started.

5. To reduce the effects of noise, the HALT mode is entered until A/D conversion ends.

CHAPTER 4 SETTING METHODS

This chapter describes how to set up operational amplifier 0 and provides software coding examples.

For details about the A/D converter settings, refer to the 78K0/Kx2-L Sample Program (A/D Converter) Successive A/D Conversion & Average Value Calculation Application Note.

For other initial settings, refer to the 78K0/Kx2-L Sample Program (Initial Settings) LED Lighting Switch Control Application Note.

For how to set registers, refer to the 78K0/Kx2-L User's Manual.

For assembler instructions, refer to the 78K/0 Series Instructions User's Manual.

4.1 Setting up Operational Amplifier 0

Operational amplifier 0 uses the following registers:

- Operational amplifier 0 control register (AMP0M)
- A/D port configuration register 0 (ADPC0)
- Port mode register 2 (PM2)

[Example of the setup procedure when outputting the analog voltage amplified in single-amplifier mode to the A/D converter]

<1> Use the ADPC0 register to specify the pins to be used in the single-amplifier mode (AMP0-, AMP0+, and AMP0OUT) as analog input pins.

<2> Use the PM2 register to specify the pins to be used in the single-amplifier mode (AMP0-, AMP0+, and AMP0OUT) as input pins.

<3> Set the OPAMP0E bit of the AMP0M register to 1 to enable operation in single-amplifier mode.

<4> Use the ADS register of the A/D converter to specify ANI1 (alternately used as AMP0OUT) as the analog input channel.

(1) Operational amplifier 0 control register (AMP0M)

This register controls the operation of operational amplifier 0.

Figure 4-1. Format of Operational Amplifier 0 Control Register (AMP0M)

OPAMP0E	PGAEN	0	0	0	0	AMP0VG1	AMP0VG0

AMP0VG1	AMP0VG0	PGA mode of operational amplifier 0 gain selection
0	0	×4
0	1	×8
1	0	×16
1	1	×32

OPAMP0E	PGAEN	Operational amplifier 0 operation control
0	0	Stops operational amplifier 0 operation
0	1	Enables operational amplifier 0 (PGA mode only) operation
1	0	Enables operational amplifier 0 (single-amplifier mode only) operation
1	1	Enables operational amplifier 0 (simultaneous operation in the PGA and single-amplifier modes) operation

Cautions

1. **When using the PGA mode, use the ADPC0 register to select the PGAIN/AMP0OUT/ANI1/P21 pin as an analog input.**
2. **When using the single-amplifier mode, use the ADPC0 register to select the AMP0OUT/PGAIN/ANI1/P21, AMP0-/ANI0/P20, and AMP0+/ANI2/P22 pins as analog inputs.**
3. **When using as digital inputs the pins of port 2, which are not used with operational amplifier 0, when operational amplifier 0 is used, make sure that the input levels are fixed.**
4. **Be sure to clear bits 5 to 2 to “0”.**

Remark The values written in red in the above figure are specified in this sample program.

(2) A/D port configuration register 0 (ADPC0)

ADPC0 switches the P20/AMP0-/ANI0 to P27/ANI7 pins to digital I/O or analog input of port. Each bit of ADPC0 corresponds to a pin of port 2 and can be specified in 1-bit units.

Specify the pins to be used in the PGA mode or single-amplifier mode as analog input pins by using ADPC0.

Figure 4-2. Format of A/D Port Configuration Register 0 (ADPC0)

ADPCS7[Note 1]	ADPCS6[Note 1]	ADPCS5[Note 2]	ADPCS4[Note 2]	ADPCS3	ADPCS2	ADPCS1	ADPCS0

ADPCSn	Digital I/O or analog input selection (n = 0 to 2)
0	Analog input
1	Digital I/O

ADPCSn	Digital I/O or analog input selection (n = 3 to 7)
0	Analog input
1	Digital I/O

Notes 1. This bit can be set only in the 78K0/KC2-L. Be sure to clear this bit to 0 in the 78K0/KY2-L, 78K0/KA2-L, and 78K0/KB2-L.

2. This bit can be set only in the 78K0/KA2-L and 78K0/KC2-L. Be sure to clear this bit to 0 in the 78K0/KY2-L and 78K0/KB2-L.

Cautions 1. Set the pin set to analog input to the input mode by using port mode register 2 (PM2).

2. If data is written to ADPC0, a wait cycle is generated. Do not write data to ADPC0 when the peripheral hardware clock (f_{PRS}) is stopped.

Remark The values written in red in the above figure are specified in this sample program.

(3) Port mode register 2 (PM2)

When using the AMP0-/ANI0/P20, AMP0OUT/PGAIN/ANI1/P21, and AMP0+/ANI2/P22 for operational amplifier 0, set PM20 to PM22 to 1.

The output latches of P20 to P22 at this time may be 0 or 1.

If PM20 to PM22 are set to 0, they cannot be used as the operational amplifier 0 pins.

Figure 4-3. Format of Port Mode Register 2 (PM2)

PM27[Note 1]	PM26[Note 1]	PM25[Note 2]	PM24[Note 2]	PM23	PM22	PM21	PM20

P2n pin I/O mode selection (n = 0 to 2)

0	Output mode (output buffer on)
1	Input mode (output buffer off)

P2n pin I/O mode selection (n = 3 to 7)

0	Output mode (output buffer on)
1	Input mode (output buffer off)

Notes 1. This bit can be set only in the 78K0/KC2-L. Be sure to set this bit to 1 in the 78K0/KY2-L, 78K0/KA2-L, and 78K0/KB2-L.

2. This bit can be set only in the 78K0/KA2-L and 78K0/KC2-L. Be sure to set this bit to 1 in the 78K0/KY2-L and 78K0/KB2-L.

Remark The values written in red in the above figure are specified in this sample program.

(4) Analog input channel specification register (ADS)

This register specifies the analog input channel of the A/D converter. The analog voltage amplified by using operational amplifier 0 in the single-amplifier mode can be input to the A/D converter by specifying analog input pin ANI1 as the analog input channel of the A/D converter, because the AMP0OUT pin of operational amplifier 0 is alternately used as ANI1 of the A/D converter.

Figure 4-4. Format of Analog Input Channel Specification Register (ADS)

0	ADOAS	0	0	ADS3	ADS2	ADS1	ADS0

ADOAS	ADS3	ADS2	ADS1	ADS0	Analog input channel	Input source
0	0	0	0	0	ANI0	P20/ANI0 pin
0	**0**	**0**	**0**	**1**	ANI1	P21/ANI1 pin
0	0	0	1	0	ANI2	P22/ANI2 pin
0	0	0	1	1	ANI3	P23/ANI3 pin
0	0	1	0	0	ANI4	P24/ANI4 pin
0	0	1	0	1	ANI5	P25/ANI5 pin
0	0	1	1	0	ANI6	P26/ANI6 pin
0	0	1	1	1	ANI7	P27/ANI7 pin
0	1	0	0	0	ANI8	P10/ANI8 pin
0	1	0	0	1	ANI9	P11/ANI9 pin
0	1	0	1	0	ANI10	P12/ANI10 pin
1	x	x	x	x	PGAIN	PGA output signal
Other than the above					Setting prohibited	

Cautions 1. Be sure to clear bits 7, 5, and 4 to "0".

2. Set a channel to be used for A/D conversion in the input mode by using port mode register 2 (PM2).

3. Set ADS after PGA operation setting when selecting the PGA output signal as analog input.

4. If data is written to ADS, a wait cycle is generated. Do not write data to ADS when the peripheral hardware clock (f_{PRS}) is stopped.

Remarks 1. A/D converter analog input pins differ depending on products.

- 78K0/KY2-L: ANI0 to ANI3
- 78K0/KA2-L: ANI0 to ANI5
- 78K0/KB2-L: ANI0 to ANI3, ANI8 to ANI10
- 78K0/KC2-L: ANI0 to ANI10

2. The values written in red in the above figure are specified in this sample program.

3. x: don't care

4.2 Software Coding Example

The settings to be specified for operational amplifier 0 in the 78K0/KC2-L source program are shown below as a software coding example.

For details about the registers used for the A/D converter (ADCE, ADCS, and ADCR), refer to the 78K0/Kx2-L Sample Program (A/D Converter) Successive A/D Conversion & Average Value Calculation Application Note.

(1) Assembly language

```
XMAIN   CSEG    UNIT
IRESET:
 • • • (Omitted) • • •

        MOV     ADPC0,  #11111000B       ; Specify P20 to P22 as analog input pins
 • • • (Omitted) • • •

        MOV     PM2,    #00000111B       ; Specify P20 to P22 as input ports
 • • • (Omitted) • • •

        MOV     AMP0M,  #10000000B       ; Operational amplifier 0 control register
 • • • (Omitted) • • •

        MOV     ADS,    #00000001B       ; Specify ANI1 (AMP0OUT) as the analog input channel
 • • • (Omitted) • • •

        SET1    ADCE                     ; Start the A/D voltage comparator
 • • • (Omitted) • • •
        CLR1    ADIF                     ; Clear the INTAD interrupt request
        SET1    ADCS                     ; Start A/D conversion

        ; Make the system wait until A/D conversion ends
        HALT                             ;  Enter  the  HALT  mode  (Exit  the  HALT  mode  by
generating an INTAD interrupt)

        MOVW    AX,     ADCR             ; Read the A/D conversion results
        CLR1    ADCS                     ; Stop A/D conversion

 • • • (Omitted) • • •
        CLR1    ADCE                     ; Stop the A/D voltage comparator
```

Specify the P20/AMP0-, P21/AMP0OUT, and P22/AMP0+ pins as analog input pins.

Specify P20 to P22 as input ports.

Specify single-amplifier mode for operational amplifier 0.

Specify ANI1 as the analog input channel.

Start the A/D voltage comparator.

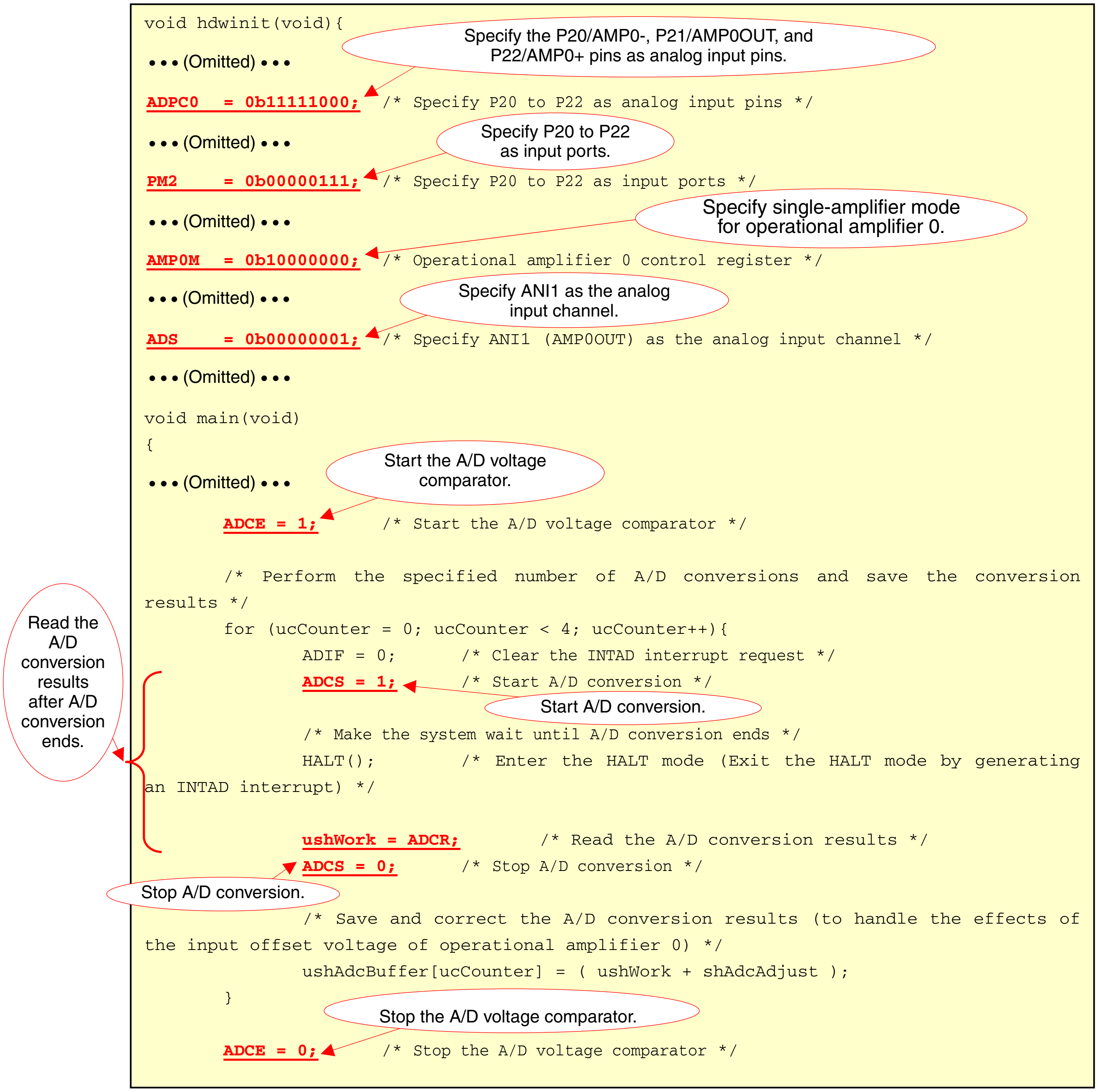
Start A/D conversion.

Read the A/D conversion results after A/D conversion ends.

Stop A/D conversion.

Stop the A/D voltage comparator.

(2) C language


Specify the P20/AMP0-, P21/AMP0OUT, and P22/AMP0+ pins as analog input pins.
Specify P20 to P22 as input ports.
Specify single-amplifier mode for operational amplifier 0.
Specify ANI1 as the analog input channel.
Start the A/D voltage comparator.
Read the A/D conversion results after A/D conversion ends.
Start A/D conversion.
Stop A/D conversion.
Stop the A/D voltage comparator.

```
void hdwinit(void){

••• (Omitted) •••

ADPC0   = 0b11111000;  /* Specify P20 to P22 as analog input pins */

••• (Omitted) •••

PM2     = 0b00000111;  /* Specify P20 to P22 as input ports */

••• (Omitted) •••

AMP0M   = 0b10000000;  /* Operational amplifier 0 control register */

••• (Omitted) •••

ADS     = 0b00000001;  /* Specify ANI1 (AMP0OUT) as the analog input channel */

••• (Omitted) •••

void main(void)
{

••• (Omitted) •••

        ADCE = 1;      /* Start the A/D voltage comparator */

        /* Perform the specified number of A/D conversions and save the conversion
results */
        for (ucCounter = 0; ucCounter < 4; ucCounter++){
                ADIF = 0;       /* Clear the INTAD interrupt request */
                ADCS = 1;       /* Start A/D conversion */

                /* Make the system wait until A/D conversion ends */
                HALT();         /* Enter the HALT mode (Exit the HALT mode by generating
an INTAD interrupt) */

                ushWork = ADCR;         /* Read the A/D conversion results */
                ADCS = 0;       /* Stop A/D conversion */

                /* Save and correct the A/D conversion results (to handle the effects of
the input offset voltage of operational amplifier 0) */
                ushAdcBuffer[ucCounter] = ( ushWork + shAdcAdjust );
        }

        ADCE = 0;      /* Stop the A/D voltage comparator */
```

CHAPTER 5 RELATED DOCUMENTS

The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

Document Name		English
78K0/Kx2-L User's Manual		PDF
78K/0 Series Instructions User's Manual		PDF
RA78K0 Assembler Package User's Manual	Language	PDF
	Operation	PDF
CC78K0 C Compiler User's Manual	Language	PDF
	Operation	PDF
PM+ Project Manager User's Manual		PDF
78K0/Kx2-L Application Note	Sample Program (Initial Settings) LED Lighting Switch Control	PDF
	Sample Program (A/D Converter) Successive A/D Conversion & Average Value Calculation	PDF

APPENDIX A PROGRAM LIST

As a program list example, the 78K0/KC2-L microcontroller source program is shown below.

● main.asm (assembly language version)

```
  ;******************************************************************************
  ;
  ;    NEC Electronics     78K0/KC2-L Series
  ;
  ;******************************************************************************
  ;    78K0/KC2-L Series   Sample Program (Operational Amplifier)
  ;******************************************************************************
  ;    Amplifying Analog Voltages in Single-Amplifier Mode
  ;******************************************************************************
  ;<<History>>
  ;    2009.1.--    Release
  ;******************************************************************************
  ;
  ;<<Overview>>
  ;
  ; This sample program presents an example of using the operational amplifier.
  ; A non-inverting amplifier is set up by using operational amplifier 0 in the
  ; single-amplifier mode, the amplified analog voltage is A/D converted using
  ; the A/D converter, and then the conversion results and the average of four
  ; conversion results are saved in the RAM area.
  ;
  ;
  ; <Primary initial settings>
  ;
  ; (Option byte settings)
  ; - Allowing the internal low-speed oscillator to be programmed to stop
  ; - Disabling the watchdog timer
  ; - Setting the internal high-speed oscillation clock frequency to 8 MHz
  ; - Disabling LVI from being started by default
  ; (Settings during initialization immediately after a reset ends)
  ; - Specifying the ROM and RAM sizes
  ; - Setting up I/O ports
  ;   → Specifying the P20/AMP0-, P21/AMP0OUT, and P22/AMP0+ pins as analog input pins
  ; - Checking whether VDD is 2.7 V or more by using the low-voltage detector
  ; - Specifying that the CPU clock and peripheral hardware clock run on the internal
  ;   high-speed oscillation clock (8 MHz)
  ; - Stopping the internal low-speed oscillator
  ; - Disabling peripheral hardware not to be used
  ; - Specifying single-amplifier mode for operational amplifier 0
  ; - Setting up the A/D converter
  ;    → Specifying the standard mode as the operating mode and 264/fPRS (about 33 us) as
the conversion time
```

```
;   → Specifying ANI1 as the analog input channel
;   → Enabling the INTAD interrupt
;   → Enabling the INTAD interrupt for exiting the HALT mode during A/D conversion
;
;
; <Area in which to save the A/D conversion results>
;
; +---------------------------------------------------------+
; | Data Type                           | Variable Name     |
; |---------------------------------------------------------|
; | A/D conversion result (1st time)    | RADCBUF + 0       |
; | A/D conversion result (2nd time)    | RADCBUF + 2       |
; | A/D conversion result (3rd time)    | RADCBUF + 4       |
; | A/D conversion result (4th time)    | RADCBUF + 6       |
; | A/D conversion result (average)     | RADCAVR           |
; +---------------------------------------------------------+
;
;
; <I/O port settings>
;  Input: P20 to P22
;  * Set all unused ports that can be specified as output ports as output ports.
;
;******************************************************************************


;==============================================================================
;
;    Vector table
;
;==============================================================================
XVECT1          CSEG    AT      0000H
     DW     RESET_START         ;0000H RESET input, POC, LVI, WDT
XVECT2          CSEG    AT      0004H
     DW     IINIT               ;0004H INTLVI
     DW     IINIT               ;0006H INTP0
     DW     IINIT               ;0008H INTP1
     DW     IINIT               ;000AH INTP2
     DW     IINIT               ;000CH INTP3
     DW     IINIT               ;000EH INTP4
     DW     IINIT               ;0010H INTP5
     DW     IINIT               ;0012H INTSRE6
     DW     IINIT               ;0014H INTSR6
     DW     IINIT               ;0016H INTST6
     DW     IINIT               ;0018H INTCSI10
     DW     IINIT               ;001AH INTTMH1
     DW     IINIT               ;001CH INTTMH0
     DW     IINIT               ;001EH INTTM50
     DW     IINIT               ;0020H INTTM000
```

```
       DW     IINIT               ;0022H INTTM010
       DW     IINIT               ;0024H INTAD
       DW     IINIT               ;0026H INTP6
       DW     IINIT               ;0028H INTRTCI
       DW     IINIT               ;002AH INTTM51
       DW     IINIT               ;002CH INTKR
       DW     IINIT               ;002EH INTRTC
       DW     IINIT               ;0030H INTP7
       DW     IINIT               ;0032H INTP8
       DW     IINIT               ;0034H INTIICA0
       DW     IINIT               ;0036H INTCSI11
       DW     IINIT               ;0038H INTP9
       DW     IINIT               ;003AH INTP10
       DW     IINIT               ;003CH INTP11
       DW     IINIT               ;003EH BRK

  ;================================================================================
  ;
  ;    Define the ROM data table
  ;
  ;================================================================================
  XTBL CSEG   AT    0200H
  TADCADJ:    DW    0005H         ; A/D conversion result correction value −5
                                  ; *For handling the effects of the input offset voltage
of operational amplifier 0

  ;================================================================================
  ;
  ;    Define the RAM data table
  ;
  ;================================================================================
  DRAM DSEG   SADDRP
  RADCBUF:    DS    8             ; Area in which to save the A/D conversion results
  RADCAVR:    DS    2             ; Average A/D conversion result
  RADCADJ:    DS    2             ; Corrected A/D conversion result

  ;================================================================================
  ;
  ;    Define the memory stack area
  ;
  ;================================================================================
  DSTK DSEG   IHRAM
  STACKEND:
              DS    20H           ; Memory stack area = 32 bytes
  STACKTOP:                       ; Start address of the memory stack area


  ;********************************************************************************
  ;
  ;    Servicing interrupts by using unnecessary interrupt sources
  ;
  ;*******************************************************************************
  XMAIN      CSEG   UNIT
  IINIT:
  ;    If an unnecessary interrupt occurred, the processing branches to this line.
  ;    The processing then returns to the initial original processing because no
processing is performed here.

       RETI

  ;*******************************************************************************
  ;
  ;    Initialization after RESET
  ;
  ;*******************************************************************************
  RESET_START:

  ;-------------------------------------------------------------------------------
  ;    Disable interrupts
  ;-------------------------------------------------------------------------------
       DI                        ; Disable interrupts

  ;-------------------------------------------------------------------------------
  ;    Set up the register bank
  ;-------------------------------------------------------------------------------
       SEL    RB0                ; Set up the register bank

  ;-------------------------------------------------------------------------------
  ;    Specify the ROM and RAM sizes
  ;-------------------------------------------------------------------------------
  ;    Note that the values to specify vary depending on the model.
  ;    Enable the settings for the model to use. (The uPD78F0588 is the default model.)
  ;-------------------------------------------------------------------------------
       ; Setting when using uPD78F0586
       ;MOV   IMS,   #042H       ; Specify the ROM and RAM sizes

       ; Setting when using uPD78F0587
       ;MOV   IMS,   #004H       ; Specify the ROM and RAM sizes

       ; Setting when using uPD78F0588
       MOV    IMS,   #0C8H       ; Specify the ROM and RAM sizes

  ;-------------------------------------------------------------------------------
  ;    Initialize the stack pointer
  ;-------------------------------------------------------------------------------
       MOVW   SP,    #STACKTOP   ; Initialize the stack pointer
```

```
;-------------------------------------------------------------------------------
;    Initialize port 0
;-------------------------------------------------------------------------------
     MOV    P0,   #00000000B    ; Set the P00 to P02 output latches to low level
     MOV    PM0,  #11111000B    ; Specify P00 to P02 as output ports
                                ; P00 to P02: Unused

;-------------------------------------------------------------------------------
;    Initialize port 1
;-------------------------------------------------------------------------------
     MOV    ADPC1,#00000111B    ; Specify P10 to P12 as digital I/O ports
     MOV    P1,   #00000000B    ; Set the P10 to P17 output latches to low level
     MOV    PM1,  #00000000B    ; Specify P10 to P17 as output ports
                                ; P10 to P17: Unused

;-------------------------------------------------------------------------------
;    Initialize port 2
;-------------------------------------------------------------------------------
     MOV    ADPC0,#11111000B    ; Specify P20 to P22 as analog input pins
                                ; Specify P23 to P27 as digital I/O pins
     MOV    P2,   #00000000B    ; Set the P20 to P27 output latches to low level
     MOV    PM2,  #00000111B    ; Specify P20 to P22 as input ports
                                ; Specify P23 to P27 as output ports
                                ; P20: Use as AMP0-
                                ; P21: Use as AMP0OUT
                                ; P22: Use as AMP0+
                                ; P23 to P27: Unused

;-------------------------------------------------------------------------------
;    Initialize port 3
;-------------------------------------------------------------------------------
     MOV    P3,   #00000000B    ; Set the P30 to P33 output latches to low level
     MOV    PM3,  #11110000B    ; Specify P30 to P33 as output ports
                                ; P30 to P33: Unused

;-------------------------------------------------------------------------------
;    Initialize port 4
;-------------------------------------------------------------------------------
     MOV    P4,   #00000000B    ; Set the P40 to P42 output latches to low level
     MOV    PM4,  #11111000B    ; Specify P40 to P42 as output ports
                                ; P40 to P42: Unused

;-------------------------------------------------------------------------------
;    Initialize port 6
;-------------------------------------------------------------------------------
     MOV    P6,   #00000000B    ; Set the P60 to P63 output latches to low level
     MOV    PM6,  #11110000B    ; Specify P60 to P63 as output ports
```

```
                                  ; P60 to P63: Unused

  ;-------------------------------------------------------------------------------
  ;    Initialize port 7
  ;-------------------------------------------------------------------------------
       MOV    P7,    #00000000B   ; Set the P70 to P75 output latches to low level
       MOV    PM7,   #11000000B   ; Specify P70 to P75 as output ports
                                  ; P70 to P75: Unused

  ;-------------------------------------------------------------------------------
  ;    Initialize port 12
  ;-------------------------------------------------------------------------------
       MOV    P12,   #00000000B   ; Set the P120 output latch to low level
       MOV    PM12,  #11111110B   ; Specify P120 as an output port
                                  ; P120 to P125: Unused

  ;-------------------------------------------------------------------------------
  ;    Low-voltage detection
  ;-------------------------------------------------------------------------------
  ;    The low-voltage detector is used to check whether VDD is 2.7 V or more.
  ;-------------------------------------------------------------------------------
       ; Set up the low-voltage detector
       SET1   LVIMK               ; Disable the INTLVI interrupt
       CLR1   LVISEL              ; Specify VDD as the detection voltage
       MOV    LVIS,  #00001001B   ; Set the low-voltage detection level (VLVI) to 2.84
±0.1 V
       CLR1   LVIMD               ; Specify that an interrupt signal is generated when a
low voltage is detected
       SET1   LVION               ; Enable low-voltage detection

       ; Make the system wait until the low-voltage detector stabilizes (10 us or more)
       MOV    B,     #5           ; Specify the number of counts
  HINI100:
       NOP
       DBNZ   B,     $HINI100     ; Has the wait period ended? No,

       ; Make the system wait until VLVI is less than or equal to VDD
  HINI110:
       NOP
       BT     LVIF,  $HINI110     ; VDD < VLVI? Yes,
       CLR1   LVION               ; Stop the low-voltage detector

  ;-------------------------------------------------------------------------------
  ;    Specify the clock frequency
  ;-------------------------------------------------------------------------------
  ;    Specify the clock frequency so that the device can run on the internal high-speed
oscillation clock.
  ;-------------------------------------------------------------------------------
```

```
      MOV    OSCCTL,#00000000B   ; Clock operation mode
  ;                   ||||+||+------- Be sure to clear this bit to 0
  ;                   |||| ++-------- RSWOSC/AMPHXT
  ;                   ||||          [XT1 oscillator oscillation mode selection]
  ;                   ||||           00: Low power consumption oscillation
  ;                   ||||           01: Normal oscillation
  ;                   ||||           1x: Ultra-low power consumption oscillation
  ;                   ||++----------- EXCLKS/OSCSELS
  ;                   ||            [Subsystem clock pin operation setting]
  ;                   ||            (P123/XT1,P124/XT2/EXCLKS)
  ;                   ||             Specify the use of the pin as an I/O port pin by
specifying 000 by also using XTSTART
  ;                   ++------------- EXCLK/OSCSEL
  ;                                 [High-speed system clock pin operation setting]
  ;                                 (P121/X1,P122/X2/EXCLK)
  ;                                  00: Input port
  ;                                  01: X1 oscillation mode
  ;                                  10: Input port
  ;                                  11: External clock input mode

      MOV    PCC,   #00000000B   ; Select the CPU clock (fCPU)
  ;                  |||+|+++------- CSS/PCC2/PCC1/PCC0
  ;                  ||| |          [CPU clock (fCPU) selection]
  ;                  ||| |           0000:fXP
  ;                  ||| |           0001:fXP/2
  ;                  ||| |           0010:fXP/2^2
  ;                  ||| |           0011:fXP/2^3
  ;                  ||| |           0100:fXP/2^4
  ;                  ||| |           1000:fSUB/2
  ;                  ||| |           1001:fSUB/2
  ;                  ||| |           1010:fSUB/2
  ;                  ||| |           1011:fSUB/2
  ;                  ||| |           1100:fSUB/2
  ;                  ||| |           (Other than the above: Setting prohibited)
  ;                  ||| +---------- Be sure to clear this bit to 0
  ;                  ||+------------ CLS
  ;                  ||             [CPU clock status]
  ;                  |+------------- XTSTART
  ;                  |              [Subsystem clock pin operation setting]
  ;                  |               Specify the use of the pin by also using EXCLKS and
OSCSELS
  ;                  +-------------- Be sure to clear this bit to 0

      MOV    RCM,   #00000010B   ; Select the operating mode of the internal oscillator
  ;                  |||||||+------- RSTOP
  ;                  |||||||        [Internal high-speed oscillator oscillating/stopped]
  ;                  |||||||         0: Internal high-speed oscillator oscillating
  ;                  |||||||         1: Internal high-speed oscillator stopped
  ;                  ||||||+-------- LSRSTOP
  ;                  ||||||         [Internal low-speed oscillator oscillating/stopped]
  ;                  ||||||          0: Internal low-speed oscillator oscillating
  ;                  ||||||          1: Internal low-speed oscillator stopped
  ;                  |+++++--------- Be sure to clear this bit to 0
  ;                  +-------------- RSTS
  ;                                 [Status of internal high-speed oscillator]

       MOV    MOC,  #10000000B    ;  Select  the  operating  mode  of  the  high-speed  system
clock
  ;                  |++++++-------- Be sure to clear this bit to 0
  ;                  +-------------- MSTOP
  ;                                 [Control of high-speed system clock operation]
  ;                                  0: X1 oscillator operating/external clock from
  ;                                     EXCLK pin is enabled
  ;                                  1: X1 oscillator stopped/external clock from
  ;                                     EXCLK pin is disabled

       MOV    MCM,  #00000000B    ; Select the clock to supply
  ;                  |||||+|+------- XSEL/MCM0:
  ;                  ||||| |        [Clock supplied to main system and
  ;                  ||||| |         peripheral hardware]
  ;                  ||||| |         00: Main system clock (fXP)
  ;                  ||||| |              = internal high-speed oscillation clock (fIH)
  ;                  ||||| |             Peripheral hardware clock (fPRS)
  ;                  ||||| |              = internal high-speed oscillation clock (fIH)
  ;                  ||||| |         01: Main system clock (fXP)
  ;                  ||||| |              = internal high-speed oscillation clock (fIH)
  ;                  ||||| |             Peripheral hardware clock (fPRS)
  ;                  ||||| |              = internal high-speed oscillation clock (fIH)
  ;                  ||||| |         10: Main system clock (fXP)
  ;                  ||||| |              = internal high-speed oscillation clock (fIH)
  ;                  ||||| |             Peripheral hardware clock (fPRS)
  ;                  ||||| |              = high-speed system clock (fIH)
  ;                  ||||| |         11: Main system clock (fXP)
  ;                  ||||| |              = high-speed system clock (fIH)
  ;                  ||||| |             Peripheral hardware clock (fPRS)
  ;                  ||||| |              = high-speed system clock (fIH)
  ;                  ||||| +-------- MCS
  ;                  |||||          [Main system clock status]
  ;                  +++++---------- Be sure to clear this bit to 0

       MOV    PER0, #00000000B    ; Control the real-time counter control clock
  ;                  |++++++-------- Be sure to clear this bit to 0
  ;                  +-------------- RTCEN:
  ;                                 [Real-time counter control clock]
  ;                                  0: Stop supply of control clock
  ;                                  1: Supply control clock
```

```
;-------------------------------------------------------------------------------
;    Disable peripheral hardware not to be used
;-------------------------------------------------------------------------------
     ; 16-bit timer/event counter 00
     MOV    TMC00, #00000000B   ; Disable the counter

     ; 8-bit timer/event counters 50 and 51
     MOV    TMC50, #00000000B   ; Disable timer 50
     MOV    TMC51, #00000000B   ; Disable timer 51

     ; 8-bit timers H0 and H1
     MOV    TMHMD0,      #00000000B   ; Stop timer H0
     MOV    TMHMD1,      #00000000B   ; Stop timer H1

     ; Real-time counter
     MOV    RTCC0, #00000000B   ; Stop the counter

     ; Clock output controller
     MOV    CKS,   #00000000B   ; Stop the clock frequency divider

     ; Operational amplifier
     MOV    AMP1M, #00000000B   ; Stop operational amplifier 1

     ; Serial interface UART6
     MOV    ASIM6, #00000001B   ; Disable the interface

     ; Serial interface IICA
     MOV    IICACTL0,#00000000B ; Disable the interface

     ; Serial interfaces CSI10 and CSI11
     MOV    CSIM10,      #00000000B   ; Disable CSI10
     MOV    CSIM11,      #00000000B   ; Disable CSI11

     ; Interrupts
     MOVW   MK0,   #0FFFFH      ; Disable all interrupts
     MOVW   MK1,   #0FFFFH      ;
     MOV    EGPCTL0,#00000000B  ; Disable the detection of all external interrupts
     MOV    EGPCTL1,#00000000B  ;

     ; Key interrupts
     MOV    KRM,   #00000000B   ; Disable all key interrupts

;-------------------------------------------------------------------------------
;    Set up operational amplifier 0
;-------------------------------------------------------------------------------
     MOV    AMP0M, #10000000B   ; Operational amplifier 0 control register
;                  ||||||++------- AMP0VG1/0
```

```
  ;                  ||||||        [PGA mode of operational amplifier 0 gain selection]
  ;                  ||||||         00: x4
  ;                  ||||||         01: x8
  ;                  ||||||         10: x16
  ;                  ||||||         11: x32
  ;                  ||++++--------- Be sure to clear this bit to 0
  ;                  ++------------- OPAMP0E/PGAEN
  ;                                [Operational amplifier 0 operation control]
  ;                                 00: Stop operational amplifier 0 operation
  ;                                 01: Enable operational amplifier 0 (PGA mode only)
operation
  ;                                 10: Enable operational amplifier 0 (single-amplifier
  ;                                     mode only) operation
  ;                                 11: Enable operational amplifier 0 (simultaneous
  ;                                     operation in the PGA and single-amplifier modes)
operation

  ;-------------------------------------------------------------------------------
  ;    Set up the A/D converter
  ;-------------------------------------------------------------------------------
       MOV   ADM0,  #00000000B   ; Specify the standard mode as the operating mode and
264/fPRS as the conversion time
       MOV   ADS,   #00000001B   ; Specify ANI1 (AMP0OUT) as the analog input channel
       CLR1  ADIF                ; Clear the INTAD interrupt request
       CLR1  ADMK                ; Enable the INTAD interrupt

       BR    MMAIN_LOOP          ; Go to the main loop


  ;*******************************************************************************
  ;
  ;    Main loop
  ;
  ;*******************************************************************************
  MMAIN_LOOP:

       ; Read the corrected A/D conversion results
       MOVW  AX,    !TADCADJ     ; Read the corrected values
       MOVW  RADCADJ,AX          ; Store the corrected values in RAM

  LMAIN010:
  ;-------------------------------------------------------------------------------
  ;    A/D conversion
  ;-------------------------------------------------------------------------------
       SET1  ADCE                ; Start the A/D voltage comparator

       MOVW  DE,    #RADCBUF     ; Specify the address of the area in which to save the
A/D conversion results
```

```
       MOV    B,     #4            ; Specify the number of A/D conversions
       MOVW   HL,    #RADCADJ      ; Specify the address of the corrected A/D conversion
results
  LMAIN100:
       CLR1   ADIF                 ; Clear the INTAD interrupt request
       SET1   ADCS                 ; Start A/D conversion

       ; Make the system wait until A/D conversion ends
       HALT                        ; Enter the HALT mode (Exit the HALT mode by generating
an INTAD interrupt)

       MOVW   AX,    ADCR          ; Read the A/D conversion results
       CLR1   ADCS                 ; Stop A/D conversion

       ; Save and correct the A/D conversion results (to handle the effects of the input
offset voltage of operational amplifier 0)
       XCH    A,     X             ; Exchange the higher and lower bytes
       SUB    A,     [HL]          ; Correct the lower byte
       MOV    [DE],  A             ; Save the lower byte
       XCH    A,     X             ; Exchange the higher and lower bytes
       INCW   DE                   ; Go to the higher save area
       SUBC   A,     [HL+1]        ; Correct the higher byte
       MOV    [DE],  A             ; Save the higher byte
       INCW   DE                   ; Go to the next save area
       DBNZ   B,     $LMAIN100     ; Have the specified number of A/D conversions been
completed? No,

       CLR1   ADCE                 ; Stop the A/D voltage comparator

  ;-------------------------------------------------------------------------------
  ;    Average-value calculation of A/D conversion results
  ;-------------------------------------------------------------------------------
       MOVW   HL,    #RADCBUF      ; Specify the address of the area in which to save the
A/D conversion results
       MOV    B,     #4            ; Specify the number of A/D conversions used to
calculate the average
       MOVW   AX,    #0000H        ; Clear the AX register
  LMAIN400:
       XCH    A,     X             ; Exchange the higher and lower bytes
       ADD    A,     [HL]          ; Add the lower byte
       XCH    A,     X             ; Exchange the higher and lower bytes
       INCW   HL                   ; Go to the higher save area
       ADDC   A,     [HL]          ; Add the higher byte (including the carry of the lower
byte)
       INCW   HL                   ; Go to the next data
       DBNZ   B,     $LMAIN400     ; Has the total value been calculated? No,

       MOV    C,     #4            ; Specify the divisor
```

```
        DIVUW  C                    ; Calculate the average value (AX ← (AX/C))
        MOVW   RADCAVR,AX           ; Save the average value

        BR     LMAIN010             ; Go to the next A/D conversion
   end
```

● main.c (C language version)

```
/********************************************************************************

  NEC Electronics     78K0/KC2-L Series

*********************************************************************************
  78K0/KC2-L Series   Sample Program (Operational Amplifier)
*********************************************************************************
  Amplifying Analog Voltages in Single-Amplifier Mode
*********************************************************************************
<<History>>
  2009.1.-- Release
*********************************************************************************

<<Overview>>

This sample program presents an example of using the operational amplifier.
A non-inverting amplifier is set up by using operational amplifier 0 in the
single-amplifier mode, the amplified analog voltage is A/D converted using
the A/D converter, and then the conversion results and the average of four
conversion results are saved in the RAM area.


 <Primary initial settings>

 (Option byte settings)
 - Allowing the internal low-speed oscillator to be programmed to stop
 - Disabling the watchdog timer
 - Setting the internal high-speed oscillation clock frequency to 8 MHz
 - Disabling LVI from being started by default
 (Settings during initialization immediately after a reset ends)
 - Specifying the ROM and RAM sizes
 - Setting up I/O ports
  → Specifying the P20/AMP0-, P21/AMP0OUT, and P22/AMP0+ pins as analog input pins
 - Checking whether VDD is 2.7 V or more by using the low-voltage detector
 - Specifying that the CPU clock and peripheral hardware clock run on the internal
   high-speed oscillation clock (8 MHz)
 - Stopping the internal low-speed oscillator
 - Disabling peripheral hardware not to be used
 - Specifying single-amplifier mode for operational amplifier 0
 - Setting up the A/D converter
   → Specifying the standard mode as the operating mode and 264/fPRS (about 33 us) as
the conversion time
   → Specifying ANI1 as the analog input channel
   → Enabling the INTAD interrupt for exiting the HALT mode during A/D conversion


 <Area in which to save the A/D conversion results>
 +---------------------------------------------------------+
 | Data Type                          | Variable Name      |
 |---------------------------------------------------------|
 | A/D conversion result (1st time)   | ushAdcBuffer[0]    |
 | A/D conversion result (2nd time)   | ushAdcBuffer[1]    |
 | A/D conversion result (3rd time)   | ushAdcBuffer[2]    |
 | A/D conversion result (4th time)   | ushAdcBuffer[3]    |
 | A/D conversion result (average)    | ushAdcAverage      |
 +---------------------------------------------------------+


 <I/O port settings>
  Input: P20 to P22
  * Set all unused ports that can be specified as output ports as output ports.

*******************************************************************************/



/*==============================================================================

  Preprocessing directive (#pragma)

==============================================================================*/
#pragma SFR              /* SFR names can be described at the C source level   */
#pragma DI               /* DI instructions can be described at the C source level */
#pragma EI               /* EI instructions can be described at the C source level */
#pragma NOP              /* NOP instructions can be described at the C source level */
#pragma HALT             /* HALT instructions can be described at the C source level */

/*******************************************************************************

  Initialization after RESET

*******************************************************************************/
void hdwinit( void )
{
  unsigned char ucCounter;   /* Count variable */

/*------------------------------------------------------------------------------
  Disable interrupts
------------------------------------------------------------------------------*/
  DI();               /* Disable interrupts */

/*------------------------------------------------------------------------------
  Specify the ROM and RAM sizes
--------------------------------------------------------------------------------
  Note that the values to specify vary depending on the model.
  Enable the settings for the model to use. (The uPD78F0588 is the default model.)
------------------------------------------------------------------------------*/
  /* Setting when using uPD78F0586 */
  /*IMS =   0x42;*/          /* Specify the ROM and RAM sizes */

  /* Setting when using uPD78F0587 */
  /*IMS =   0x04;*/          /* Specify the ROM and RAM sizes */

  /* Setting when using uPD78F0588 */
  IMS =  0xC8;               /* Specify the ROM and RAM sizes */

/*------------------------------------------------------------------------------
  Initialize port 0
------------------------------------------------------------------------------*/
  P0     = 0b00000000; /* Set the P00 to P02 output latches to low level */
  PM0    = 0b11111000; /* Specify P00 to P02 as output ports */
                       /* P00 to P02: Unused */

/*------------------------------------------------------------------------------
  Initialize port 1
------------------------------------------------------------------------------*/
  ADPC1  = 0b00000111; /* Specify P10 to P12 as digital I/O ports */
  P1     = 0b00000000; /* Set the P10 to P17 output latches to low level */
  PM1    = 0b00000000; /* Specify P10 to P17 as output ports */
                       /* P10 to P17: Unused */

/*------------------------------------------------------------------------------
  Initialize port 2
------------------------------------------------------------------------------*/
  ADPC0  = 0b11111000; /* Specify P20 to P22 as analog input pins */
                       /* Specify P23 to P27 as digital I/O pins */
  P2     = 0b00000000; /* Set the P20 to P27 output latches to low level */
  PM2    = 0b00000111; /* Specify P20 to P22 as input ports */
                       /* Specify P23 to P27 as output ports */
                       /* P20: Use as AMP0- */
                       /* P21: Use as AMP0OUT */
                       /* P22: Use as AMP0+ */
                       /* P23 to P27: Unused */

/*------------------------------------------------------------------------------
  Initialize port 3
------------------------------------------------------------------------------*/
  P3     = 0b00000000; /* Set the P30 to P33 output latches to low level */
  PM3    = 0b11110000; /* Specify P30 to P33 as output ports */
                       /* P30 to P33: Unused */

/*------------------------------------------------------------------------------
  Initialize port 4
  ------------------------------------------------------------------------------*/
   P4     = 0b00000000; /* Set the P40 to P42 output latches to low level */
   PM4    = 0b11111000; /* Specify P40 to P42 as output ports */
                        /* P40 to P42: Unused */

  /*------------------------------------------------------------------------------
   Initialize port 6
  ------------------------------------------------------------------------------*/
   P6     = 0b00000000; /* Set the P60 to P63 output latches to low level */
   PM6    = 0b11110000; /* Specify P60 to P63 as output ports */
                        /* P60 to P63: Unused */

  /*------------------------------------------------------------------------------
   Initialize port 7
  ------------------------------------------------------------------------------*/
   P7     = 0b00000000; /* Set the P70 to P75 output latches to low level */
   PM7    = 0b11000000; /* Specify P70 to P75 as output ports */
                        /* P70 to P75: Unused */

  /*------------------------------------------------------------------------------
   Initialize port 12
  ------------------------------------------------------------------------------*/
   P12    = 0b00000000; /* Set the P120 output latch to low level */
   PM12   = 0b11111110; /* Specify P120 as an output port */
                        /* P120 to P125: Unused */

  /*------------------------------------------------------------------------------
   Low-voltage detection
  --------------------------------------------------------------------------------
   The low-voltage detector is used to check whether VDD is 2.7 V or more.
  ------------------------------------------------------------------------------*/
   /* Set up the low-voltage detector */
   LVIMK  = 1;          /* Disable the INTLVI interrupt */
   LVISEL = 0;          /* Specify VDD as the detection voltage */
   LVIS   = 0b00001001; /* Set the low-voltage detection level (VLVI) to 2.84 ±0.1 V */
   LVIMD  = 0;          /* Specify that an interrupt signal is generated when a low
voltage is detected */
   LVION  = 1;          /* Enable low-voltage detection */

   /* Make the system wait until the low-voltage detector stabilizes (10 us or more) */
   for( ucCounter = 0; ucCounter < 2; ucCounter++ ){
      NOP();
   }

   /* Make the system wait until VLVI is less than or equal to VDD */
   while(LVIF){
      NOP();
   }
```

```
    LVION  = 0;         /* Stop the low-voltage detector */

  /*------------------------------------------------------------------------------
    Specify the clock frequency
  --------------------------------------------------------------------------------
    Specify the clock frequency so that the device can run on the internal high-speed
oscillation clock.
  ------------------------------------------------------------------------------*/
    OSCCTL = 0b00000000; /* Clock operation mode */
    /*         ||||+||+---- Be sure to clear this bit to 0 */
    /*         |||| ++----- RSWOSC/AMPHXT */
    /*         ||||       [XT1 oscillator oscillation mode selection] */
    /*         ||||        00: Low power consumption oscillation */
    /*         ||||        01: Normal oscillation */
    /*         ||||        1x: Ultra-low power consumption oscillation */
    /*         ||++-------- EXCLKS/OSCSELS */
    /*         ||         [Subsystem clock pin operation setting] */
    /*         ||         (P123/XT1,P124/XT2/EXCLKS) */
    /*         ||          Specify the use of the pin as an I/O port pin by specifying 000
by also using XTSTART */
    /*         ++---------- EXCLK/OSCSEL */
    /*                    [High-speed system clock pin operation setting] */
    /*                     (P121/X1,P122/X2/EXCLK) */
    /*                     00: Input port */
    /*                     01: X1 oscillation mode */
    /*                     10: Input port */
    /*                     11: External clock input mode */

    PCC    = 0b00000000; /* Select the CPU clock (fCPU) */
    /*         |||+|+++---- CSS/PCC2/PCC1/PCC0 */
    /*         ||| |      [CPU clock (fCPU) selection] */
    /*         ||| |       0000:fXP */
    /*         ||| |       0001:fXP/2 */
    /*         ||| |       0010:fXP/2^2 */
    /*         ||| |       0011:fXP/2^3 */
    /*         ||| |       0100:fXP/2^4 */
    /*         ||| |       1000:fSUB/2 */
    /*         ||| |       1001:fSUB/2 */
    /*         ||| |       1010:fSUB/2 */
    /*         ||| |       1011:fSUB/2 */
    /*         ||| |       1100:fSUB/2 */
    /*         ||| |       (Other than the above: Setting prohibited) */
    /*         ||| +------- Be sure to clear this bit to 0 */
    /*         ||+--------- CLS */
    /*         ||         [CPU clock status] */
    /*         |+---------- XTSTART */
    /*         |          [Subsystem clock pin operation setting] */
    /*         |           Specify the use of the pin by also using EXCLKS and OSCSELS */
```

```
   /*        +----------- Be sure to clear this bit to 0 */

   RCM   = 0b00000010; /* Select the operating mode of the internal oscillator */
   /*        |||||||+---- RSTOP */
   /*        |||||||     [Internal high-speed oscillator oscillating/stopped] */
   /*        |||||||      0: Internal high-speed oscillator oscillating */
   /*        |||||||      1: Internal high-speed oscillator stopped */
   /*        ||||||+----- LSRSTOP */
   /*        ||||||      [Internal low-speed oscillator oscillating/stopped] */
   /*        ||||||       0: Internal low-speed oscillator oscillating */
   /*        ||||||       1: Internal low-speed oscillator stopped */
   /*        |+++++------ Be sure to clear this bit to 0 */
   /*        +----------- RSTS */
   /*                    [Status of internal high-speed oscillator] */

   MOC   = 0b10000000; /* Select the operating mode of the high-speed system clock */
   /*        |+++++++---- Be sure to clear this bit to 0 */
   /*        +----------- MSTOP */
   /*                    [Control of high-speed system clock operation] */
   /*                     0:  X1  oscillator  operating/external  clock  from  EXCLK  pin  is
enabled */
   /*                     1:  X1  oscillator  stopped/external  clock  from  EXCLK  pin  is
disabled */

   MCM   = 0b00000000; /* Select the clock to supply */
   /*        |||||+|+---- XSEL/MCM0 */
   /*        ||||| |        [Clock supplied to main system and peripheral hardware] */
   /*        ||||| |         00: Main system clock (fXP) */
   /*        ||||| |              = internal high-speed oscillation clock (fIH) */
   /*        ||||| |             Peripheral hardware clock (fPRS) */
   /*        ||||| |              = internal high-speed oscillation clock (fIH) */
   /*        ||||| |         01: Main system clock (fXP) */
   /*        ||||| |              = internal high-speed oscillation clock (fIH) */
   /*        ||||| |             Peripheral hardware clock (fPRS) */
   /*        ||||| |              = internal high-speed oscillation clock (fIH) */
   /*        ||||| |         10: Main system clock (fXP) */
   /*        ||||| |              = internal high-speed oscillation clock (fIH) */
   /*        ||||| |             Peripheral hardware clock (fPRS) */
   /*        ||||| |              = high-speed system clock (fIH) */
   /*        ||||| |         11: Main system clock (fXP) */
   /*        ||||| |              = high-speed system clock (fIH) */
   /*        ||||| |             Peripheral hardware clock (fPRS) */
   /*        ||||| |              = high-speed system clock (fIH) */
   /*        ||||| +----- MCS */
   /*        |||||       [Main system clock status] */
   /*        +++++------- Be sure to clear this bit to 0 */

   PER0  = 0b00000000; /* Control the real-time counter control clock */
```

```
  /*         |+++++++---- Be sure to clear this bit to 0 */
  /*         +----------- RTCEN: */
  /*                     [Real-time counter control clock] */
  /*                      0: Stop supply of control clock */
  /*                      1: Supply control clock */

/*------------------------------------------------------------------------------
  Disable peripheral hardware not to be used
------------------------------------------------------------------------------*/
  /* 16-bit timer/event counter 00 */
  TMC00  = 0b00000000; /* Disable the counter */

  /* 8-bit timer/event counters 50 and 51 */
  TMC50  = 0b00000000; /* Disable timer 50 */
  TMC51  = 0b00000000; /* Disable timer 51 */

  /* 8-bit timers H0 and H1 */
  TMHMD0 = 0b00000000; /* Stop timer H0 */
  TMHMD1 = 0b00000000; /* Stop timer H1 */

  /* Real-time counter */
  RTCC0  = 0b00000000; /* Stop the counter */

  /* Clock output controller */
  CKS    = 0b00000000; /* Stop the clock frequency divider */

  /* Operational amplifier */
  AMP1M  = 0b00000000; /* Stop operational amplifier 1 */

  /* Serial interface UART6 */
  ASIM6  = 0b00000001; /* Disable the interface */

  /* Serial interface IICA */
  IICACTL0 = 0b00000000;  /* Disable the interface */

  /* Serial interfaces CSI10 and CSI11 */
  CSIM10 = 0b00000000; /* Disable CSI10 */
  CSIM11 = 0b00000000; /* Disable CSI11 */

  /* Interrupts */
  MK0    = 0xFFFF;        /* Disable all interrupts */
  MK1    = 0xFFFF;
  EGPCTL0   = 0b00000000; /* Disable the detection of all external interrupts */
  EGPCTL1   = 0b00000000;

  /* Key interrupts */
  KRM    = 0b00000000; /* Disable all key interrupts */
  /*------------------------------------------------------------------------------
    Set up operational amplifier 0
  ------------------------------------------------------------------------------*/
    AMP0M  = 0b10000000;/* Operational amplifier 0 control register */
    /*        ||||||++---  AMP0VG1/0                                            */
    /*        ||||||    [PGA mode of operational amplifier 0 gain selection]   */
    /*        ||||||     00: x4                                                 */
    /*        ||||||     01: x8                                                 */
    /*        ||||||     10: x16                                                */
    /*        ||||||     11: x32                                                */
    /*        ||++++-----  Be sure to clear this bit to 0                       */
    /*        ++---------  OPAMP0E/PGAEN                                        */
    /*                  [Operational amplifier 0 operation control]             */
    /*                   00: Stop operational amplifier 0 operation             */
    /*                   01: Enable operational amplifier 0 (PGA mode only) operation  */
    /*                   10: Enable operational amplifier 0 (single-amplifier   */
    /*                       mode only) operation                               */
    /*                   11: Enable operational amplifier 0 (simultaneous operation */
    /*                       in the PGA and single-amplifier modes) operation   */

  /*------------------------------------------------------------------------------
    Set up the A/D converter
  ------------------------------------------------------------------------------*/
    ADM0   = 0b00000000;/* Specify the standard mode as the operating mode and 264/fPRS as
the conversion time */
    ADS    = 0b00000001;/* Specify ANI1 (AMP0OUT) as the analog input channel */
    ADIF   = 0;         /* Clear the INTAD interrupt request */
    ADMK   = 0;         /* Enable the INTAD interrupt */

  }



  /******************************************************************************

    Main loop

  ******************************************************************************/
  void main(void)
  {
    unsigned short ushAdcBuffer[4];   /* A/D conversion results (1st to 4th) */
```

```
   unsigned short ushAdcAverage; /* Average A/D conversion result */
   signed short shAdcAdjust;     /* Corrected A/D conversion result */
   unsigned char ucCounter;   /* Count variable */
   unsigned short ushWork;    /* Work variable */

   /* Corrected A/D conversion result (to handle the effects of the input offset voltage
of operational amplifier 0) */
   const signed short aAdcAdjust = ( -5 ); /* Corrected value -5 */



   shAdcAdjust = aAdcAdjust;  /* Read the corrected A/D conversion results */

   while (1){
  /*-----------------------------------------------------------------------------
   A/D conversion
  -----------------------------------------------------------------------------*/
       ADCE = 1; /* Start the A/D voltage comparator */

       /* Perform the specified number of A/D conversions and save the conversion results
*/
       for (ucCounter = 0; ucCounter < 4; ucCounter++){
          ADIF = 0; /* Clear the INTAD interrupt request */
          ADCS = 1; /* Start A/D conversion */

          /* Make the system wait until A/D conversion ends */
          HALT();   /* Enter the HALT mode (Exit the HALT mode by generating an INTAD
interrupt) */

          ushWork = ADCR;  /* Read the A/D conversion results */
          ADCS = 0;        /* Stop A/D conversion */

          /* Save and correct the A/D conversion results (to handle the effects of the
input offset voltage of operational amplifier 0) */
          ushAdcBuffer[ucCounter] = ( ushWork + shAdcAdjust );
       }

       ADCE = 0; /* Stop the A/D voltage comparator */

  /*-----------------------------------------------------------------------------
   Average-value calculation of A/D conversion results
  -------------------------------------------------------------------------------*/
       ushWork = 0;                      /* Clear the work variable */
       for (ucCounter = 0; ucCounter < 4; ucCounter++){
          ushWork += ushAdcBuffer[ucCounter];  /* Add up the four A/D conversion results
*/
       }
       ushAdcAverage = (ushWork / 4);          /* Calculate and then save the average
value */
    }
  }
```

APPENDIX B USING 78K0/KC2-L 44-PIN PRODUCTS

All 78K0/KC2-L sample programs are intended for 48-pin products. To use a 78K0/KC2-L sample program for a 44-pin product, specify the following settings:

(1) Initial settings of ports

- Setting up port 0
  Change the value of bit 2 of port mode register 0 (PM0) from “0” to “1”.

- Setting up port 4
  Change the value of bit 2 of port mode register 4 (PM4) from “0” to “1”.

- Setting up port 7
  Change the values of bits 5 and 4 of port mode register 7 (PM7) from “00” to “11”.

(2) Disabling unused peripheral hardware

Delete the instruction used to set up the clock output selection register (CKS).

APPENDIX C REVISION HISTORY

Edition	Date Published	Page	Revision
1st edition	September 2009	–	–

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