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April 1st, 2010
Renesas Electronics Corporation

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7560 Group

List of Registers

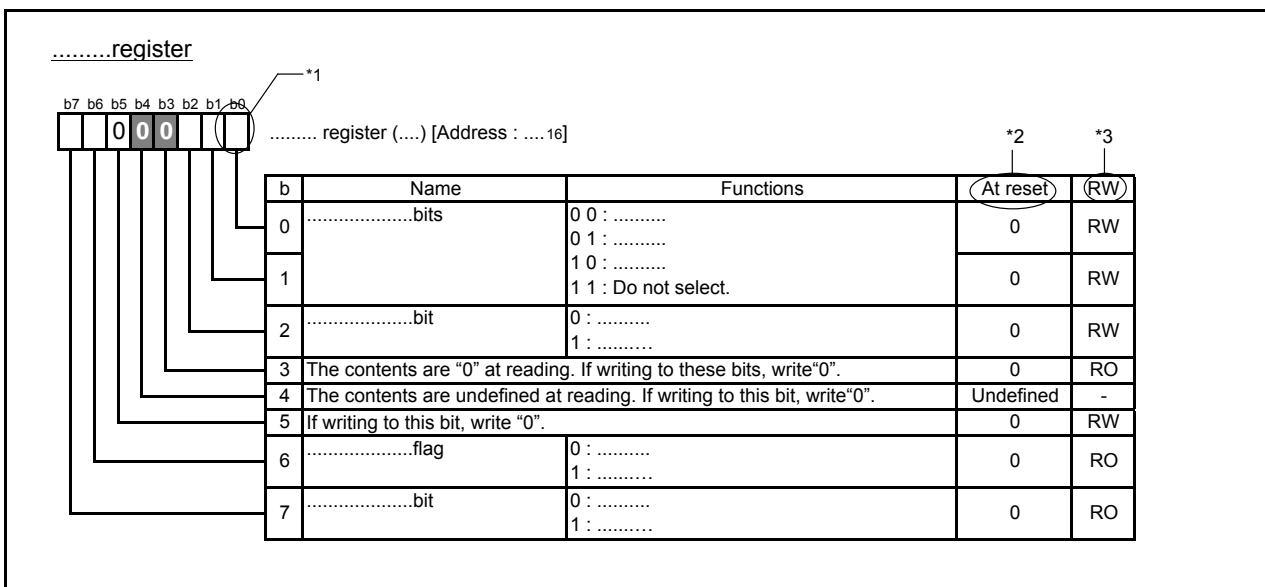
1. Abstract

The following article describes the control registers of the 7560 Group.

2. Introduction

The explanation of this issue is applied to the following condition:
 Applicable MCU: 7560 Group

3. Structure of Register



- *1
 Blank : Set "1" or "0" to this bit as usage.
 0 : If writing to this bit, write "0".
 1 : If writing to this bit, write "1".
 x : This bit is not used in the specific mode or state.
 ■ : Nothing is arranged for this bit.
- *2
 0 : "0" at reset release
 1 : "1" at reset release
 Undefined : Undefined at reset release
- *3
 RW : Read enabled. Write enabled.
 RO : Read enabled. This value depends on each bit at writing.
 WO : Write enabled. Undefined at reading.
 - : Undefined at reading. This value depends on each bit at writing.

4. List of Registers

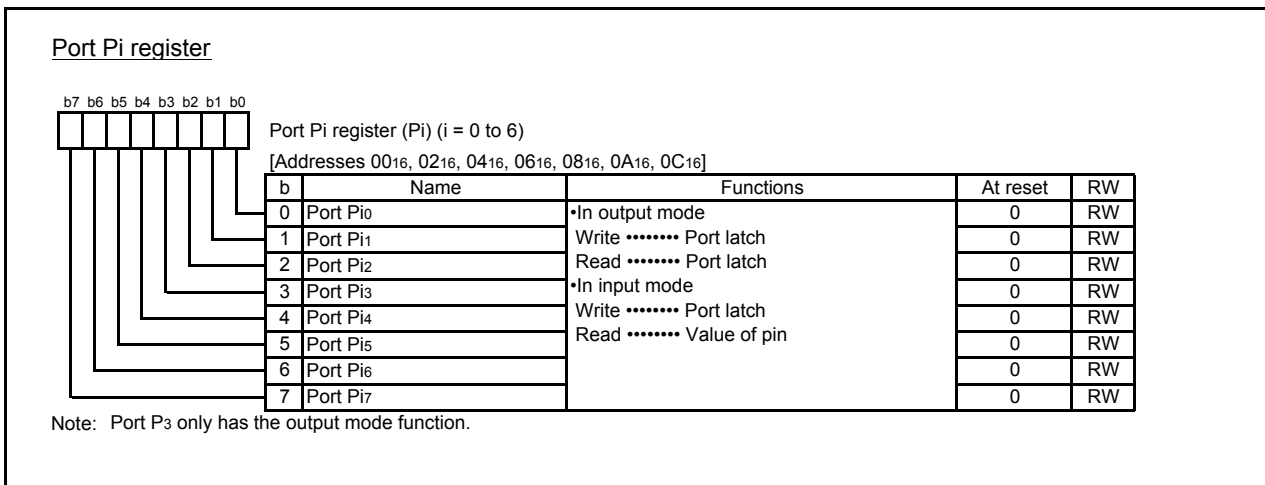


Fig. 4.1 Structure of Port Pi register (i = 0–6)

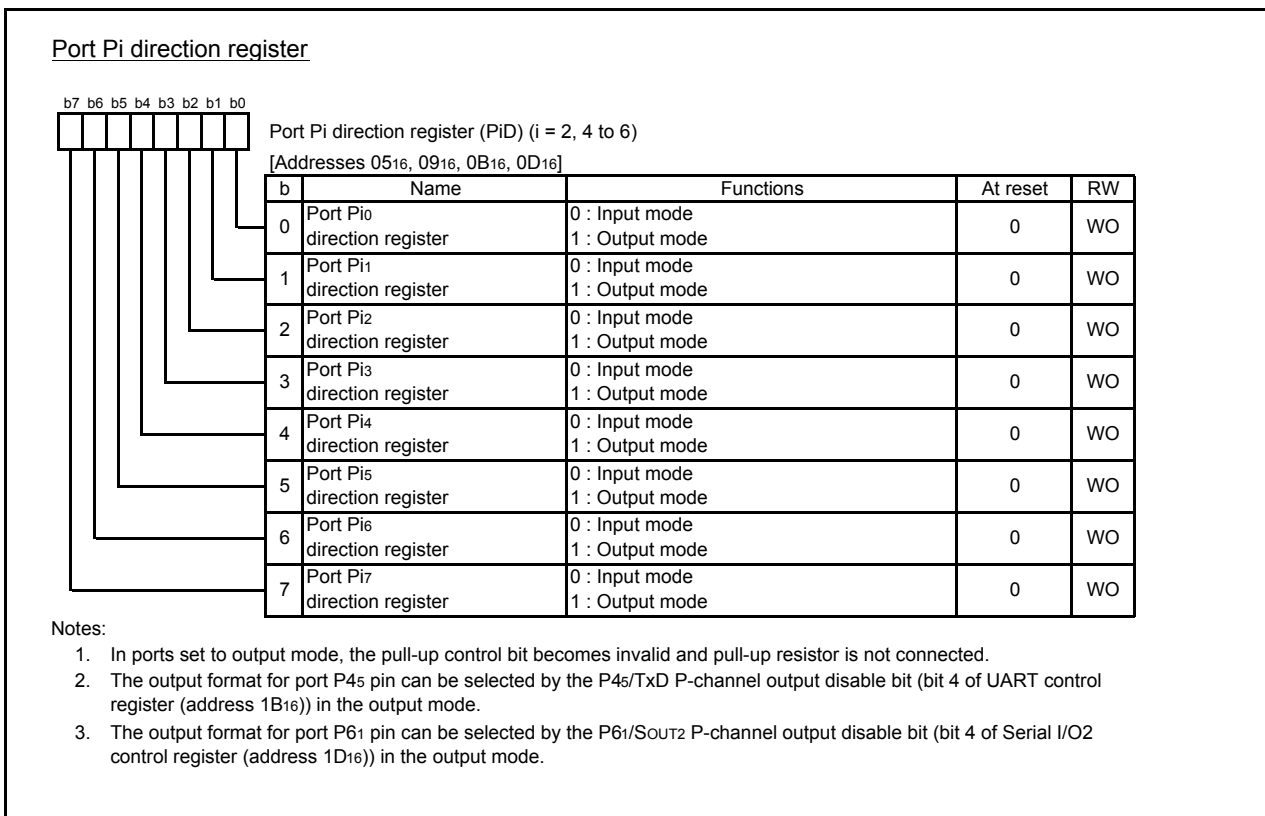
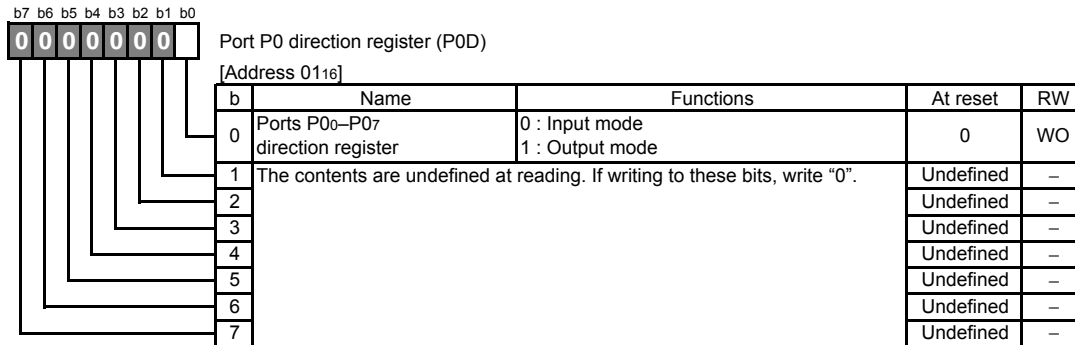


Fig. 4.2 Structure of Port Pi direction register (i = 2, 4–6)

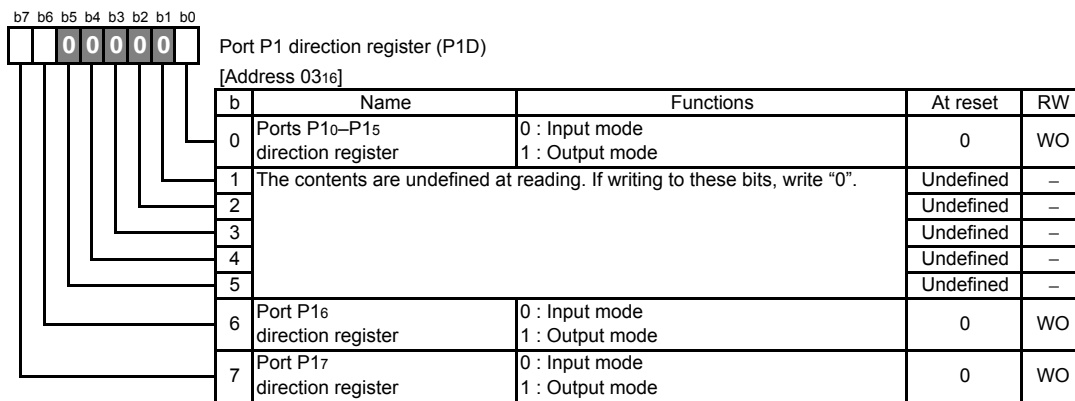
Port P0 direction register



Note: In ports set to output mode, the pull-up control bit becomes invalid and pull-up resistor is not connected.

Fig. 4.3 Structure of Port P0 register

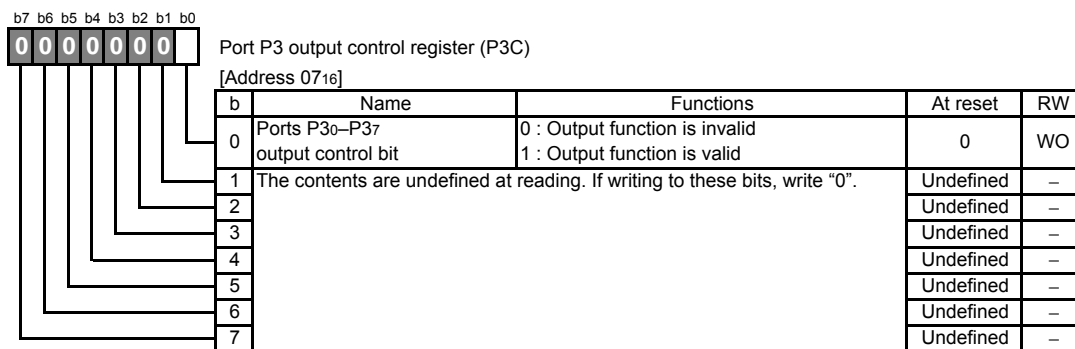
Port P1 direction register



Note: In ports set to output mode, the pull-up control bit becomes invalid and pull-up resistor is not connected.

Fig. 4.4 Structure of Port P1 direction register

Port P3 output control register



Note: In pins set to segment output by segment output enable bits 0,1 (bits 0, 1 of segment output enable register (address 3816)), this bit becomes invalid and pull-up resistor is not connected.

Fig. 4.5 Structure of Port P3 output control register

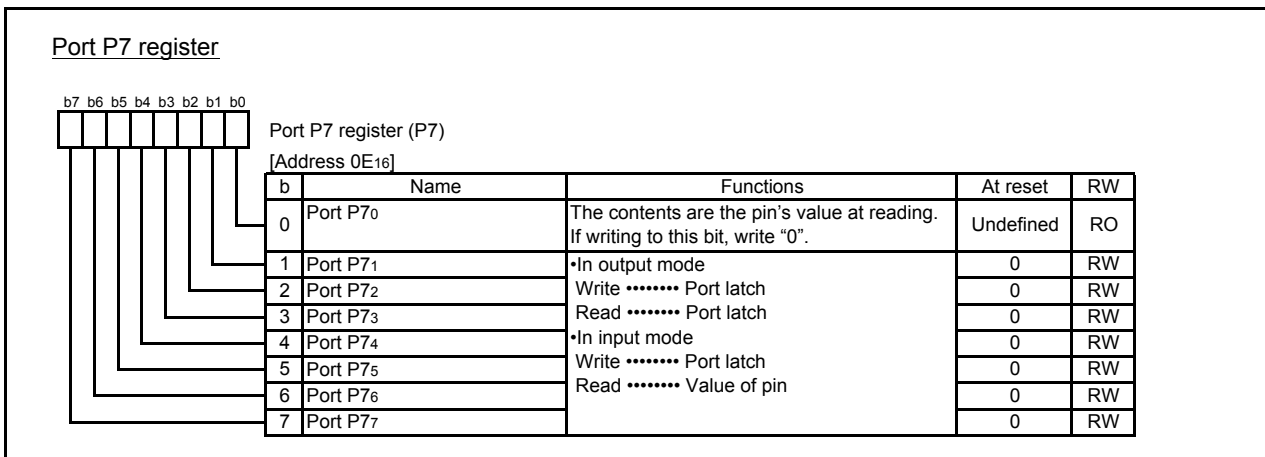


Fig. 4.6 Structure of Port P7 register

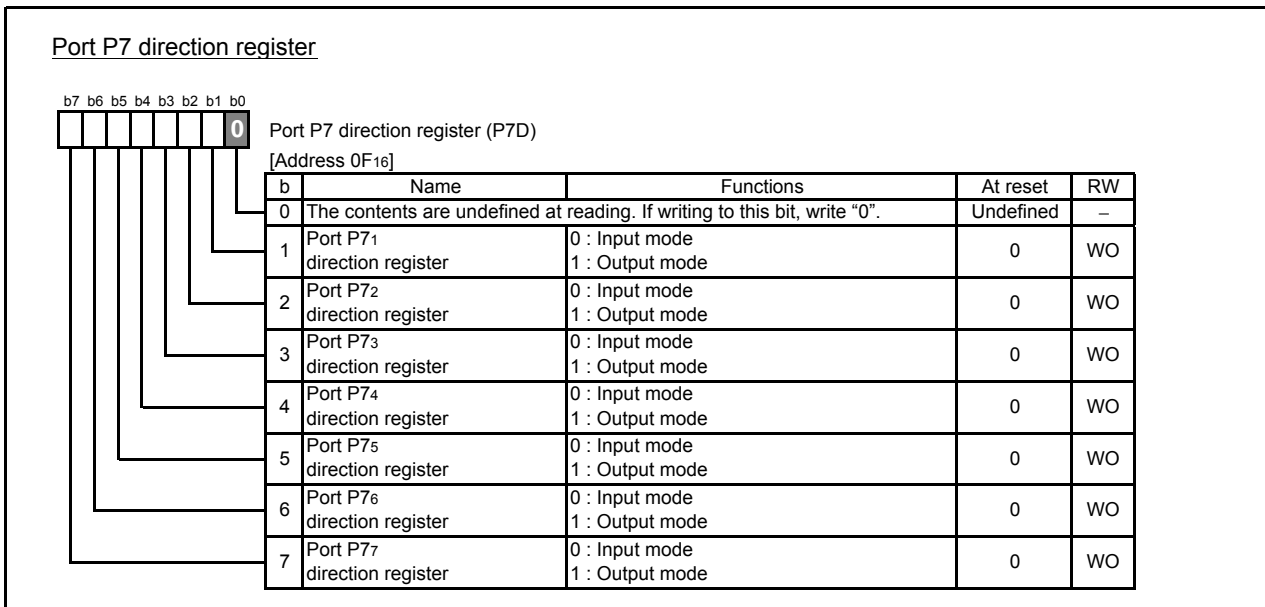


Fig. 4.7 Structure of Port P7 direction register

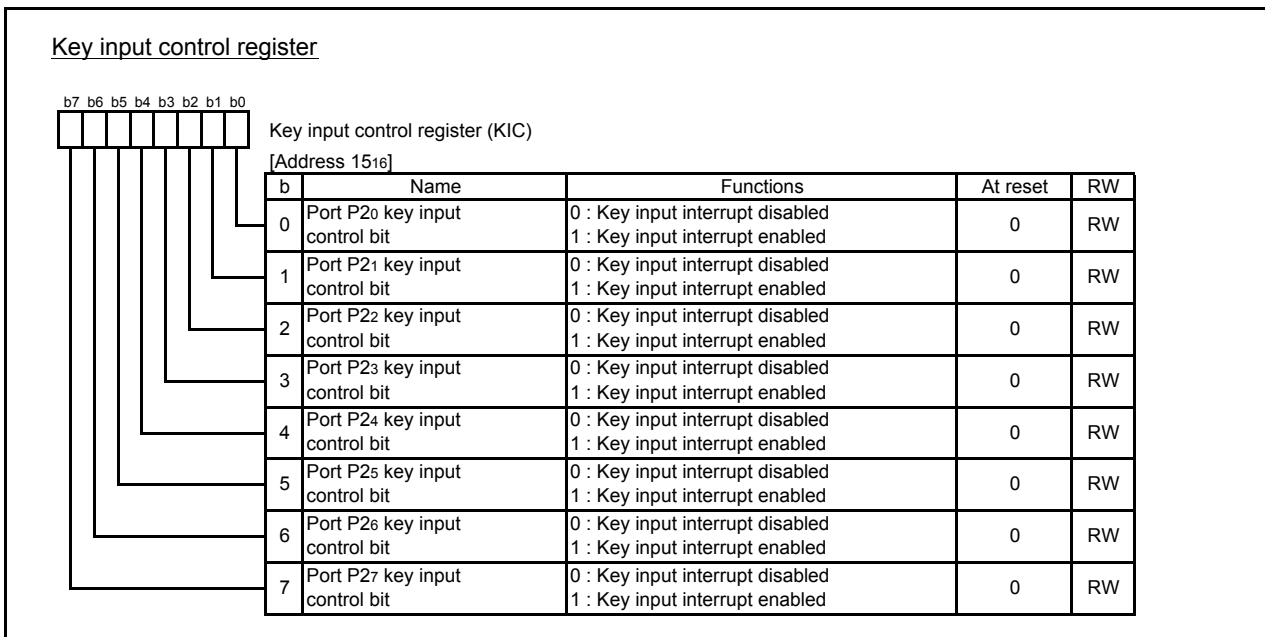
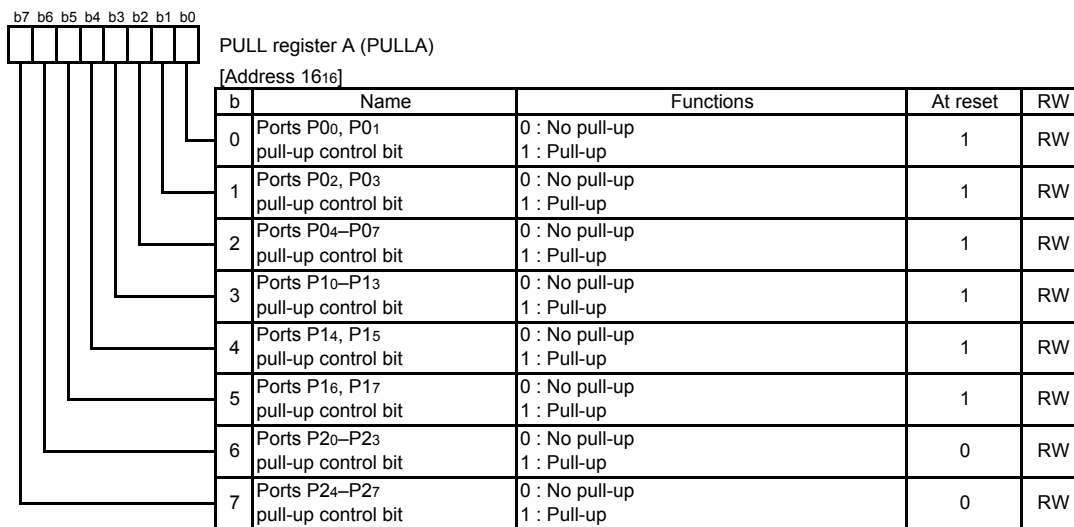


Fig. 4.8 Structure of Key input control register

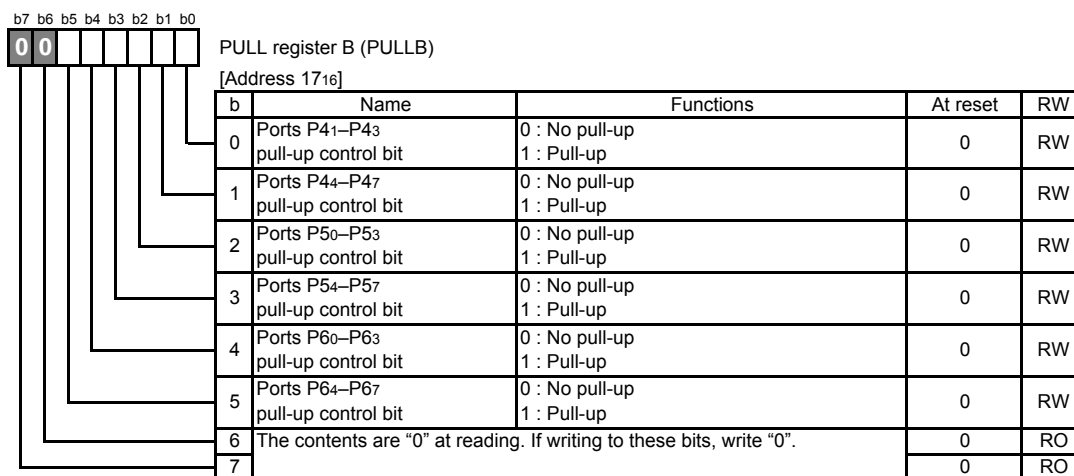
PULL register A



Note: In ports set to output mode, this bit becomes invalid and pull-up resistor is not connected.
The pin set to segment output by segment output enable bits 2 to 5 (bits 2 to 5 of segment output enable register (address 38₁₆)) becomes invalid and pull-up resistor is not connected.

Fig. 4.9 Structure of PULL register A

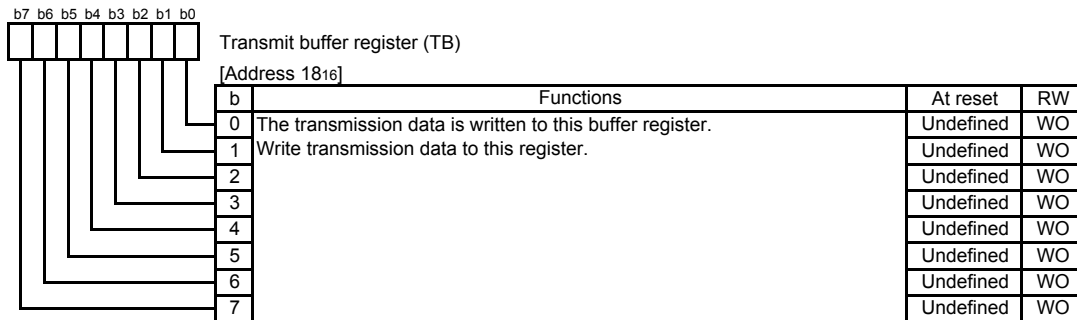
PULL register B



Note: In ports set to output mode, this bit becomes invalid and pull-up resistor is not connected.

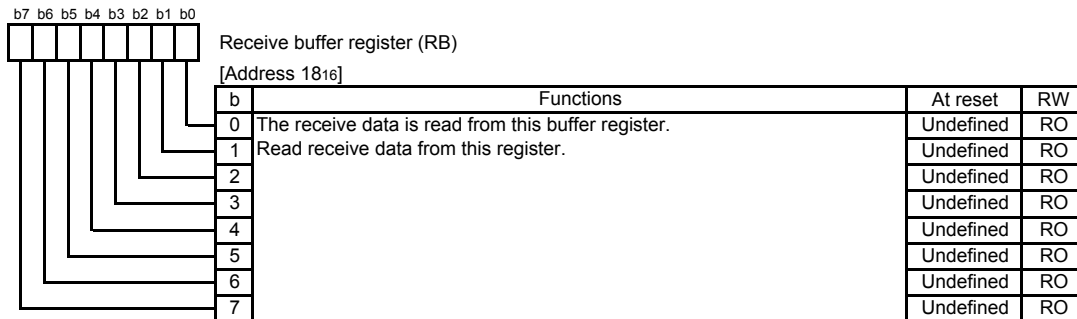
Fig. 4.10 Structure of PULL register B

Transmit buffer register



Note: This register is assigned to the same address as the receive buffer register. This register cannot be read.

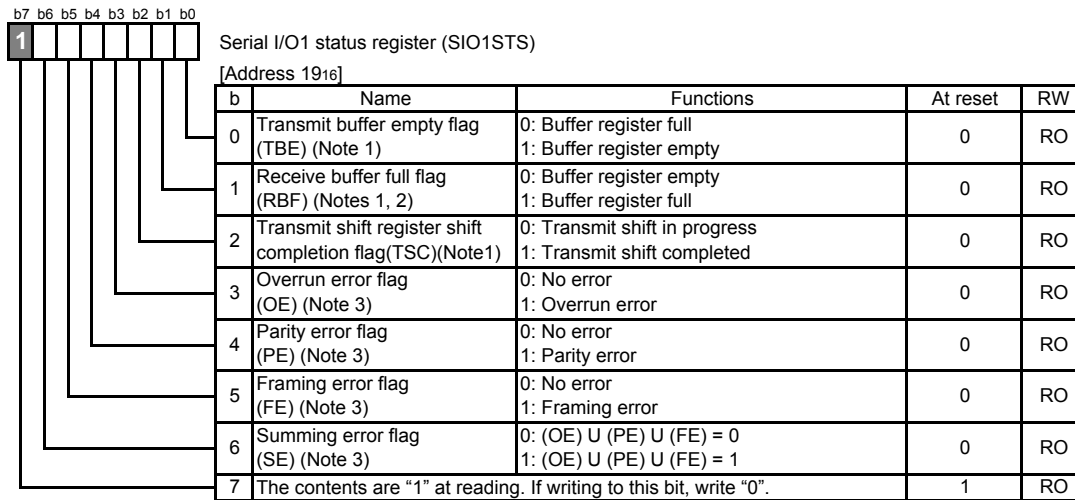
Receive buffer register



Note: This register is assigned to the same address as the transmit buffer register. This register cannot be written to.

Fig. 4.11 Structure of Transmit buffer register/Receive buffer register

Serial I/O1 status register



Notes:

1. Write "0" to this bit at writing.
2. This bit becomes "0" when the receive buffer register is read.
3. This bit becomes "0" when written to this register. If writing to this bit, write "0".

Fig. 4.12 Structure of Serial I/O1 status register

Serial I/O1 control register

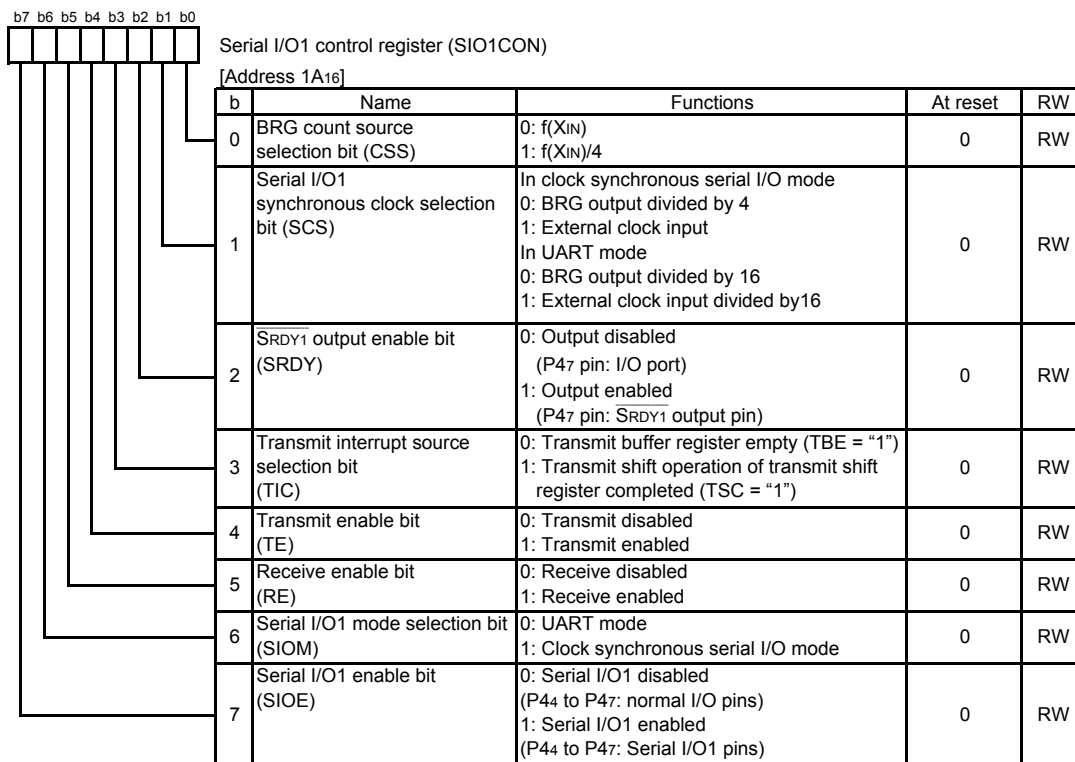


Fig. 4.13 Structure of Serial I/O1 control register

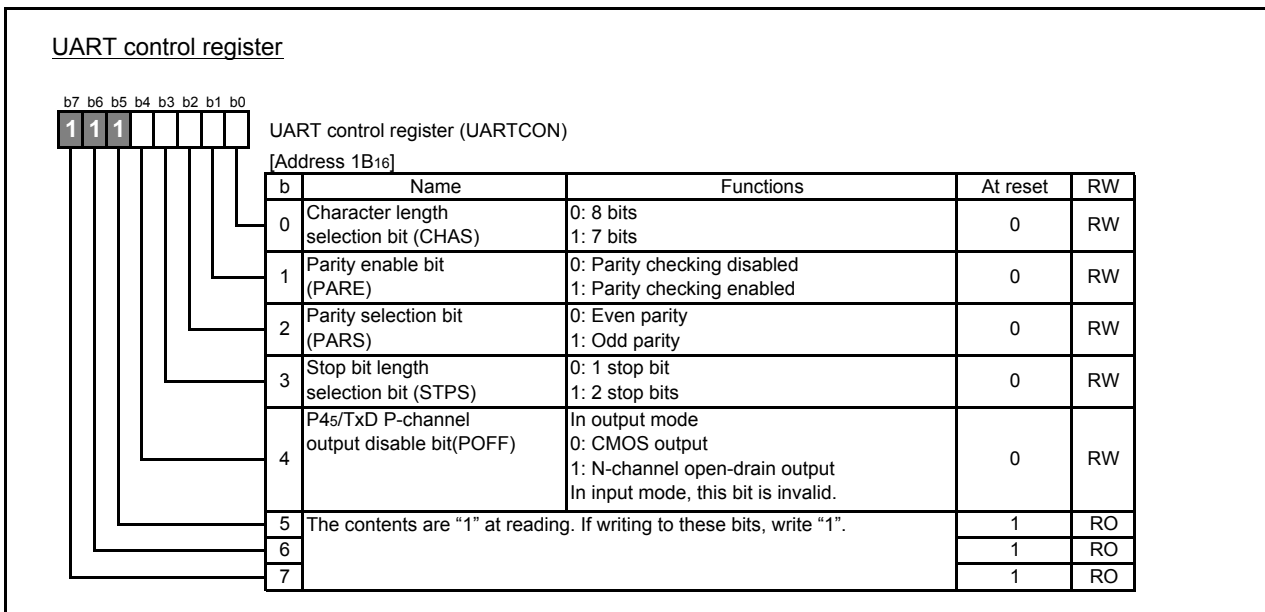


Fig. 4.14 Structure of UART control register

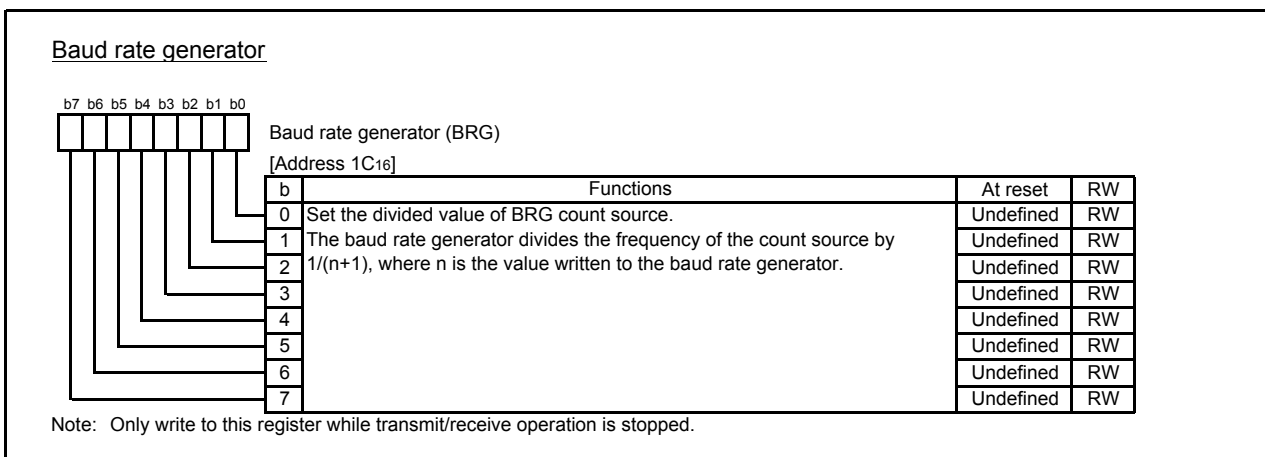


Fig. 4.15 Structure of Baud rate generator

Serial I/O2 control register

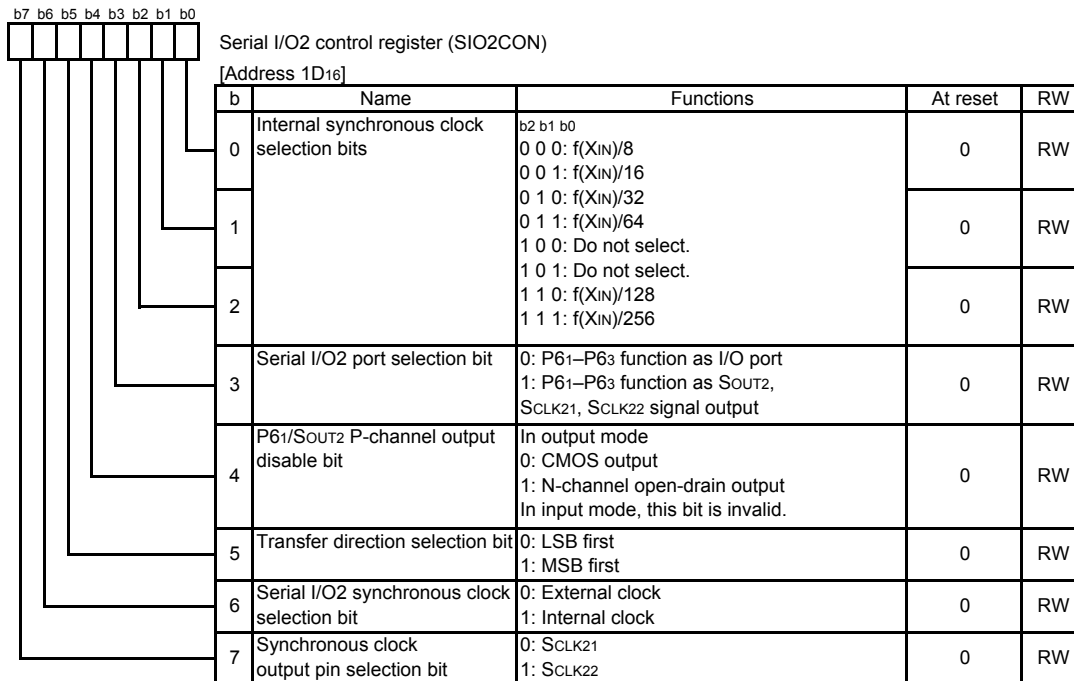


Fig. 4.16 Structure of Serial I/O2 control register

Serial I/O2 register

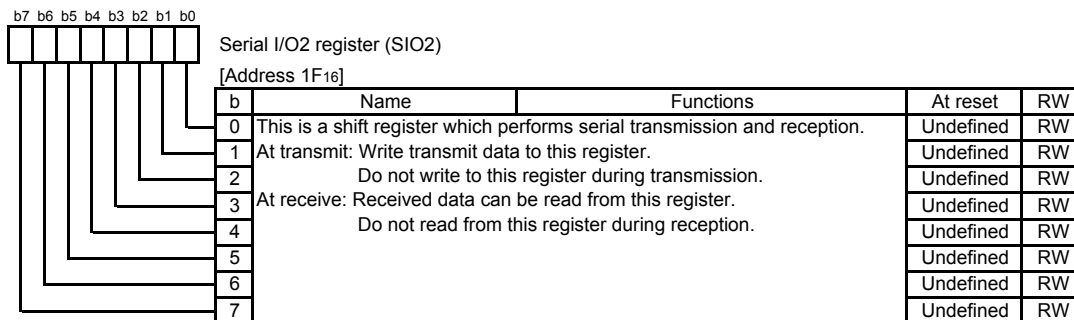


Fig. 4.17 Structure of Serial I/O2 register

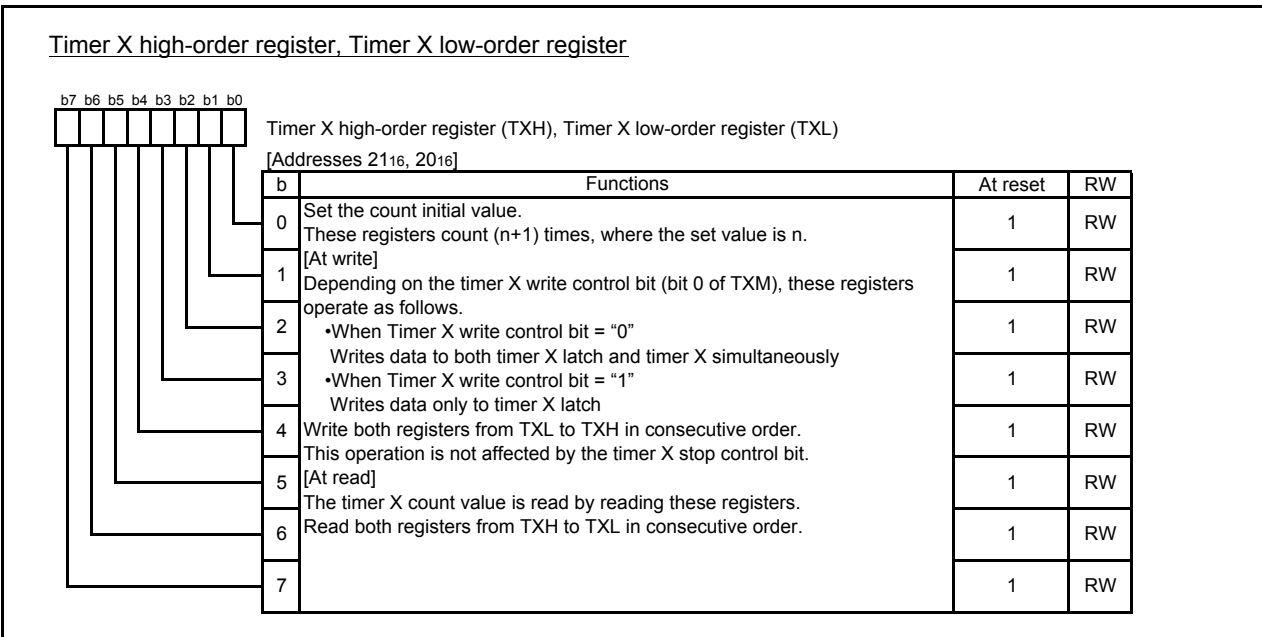


Fig. 4.18 Structure of Timer X high-order register, Timer X low-order register

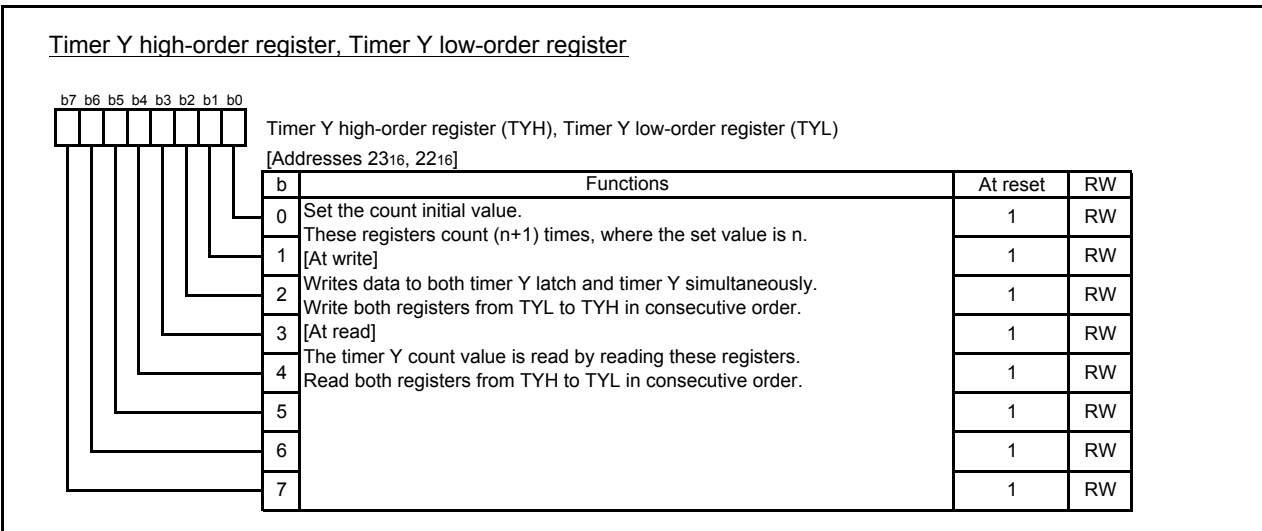


Fig. 4.19 Structure of Timer Y high-order register, Timer Y low-order register

Timer 1 register

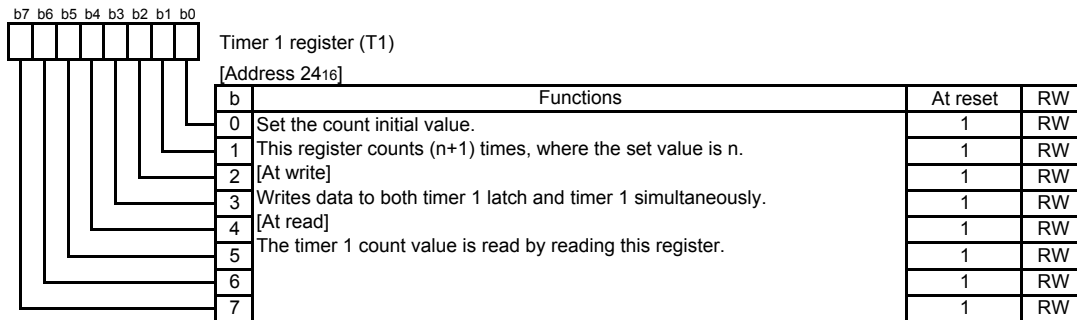


Fig. 4.20 Structure of Timer 1 register

Timer 2 register

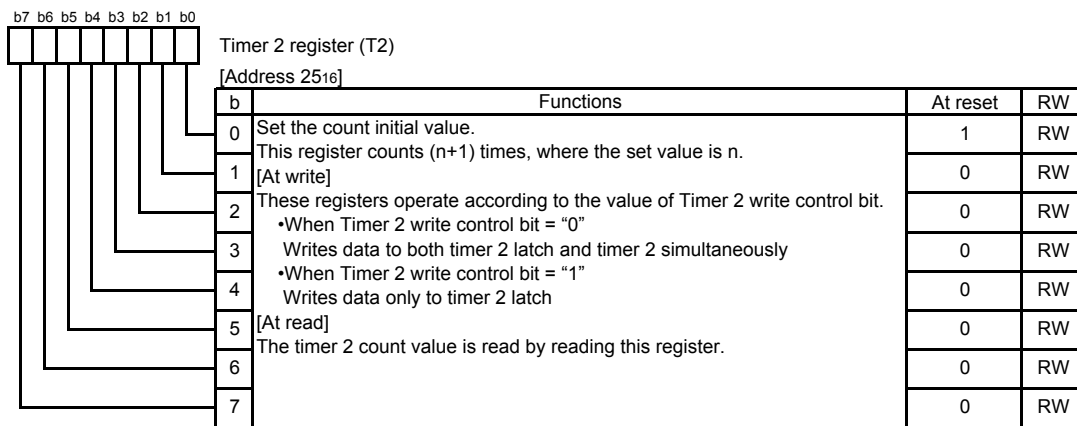


Fig. 4.21 Structure of Timer 2 register

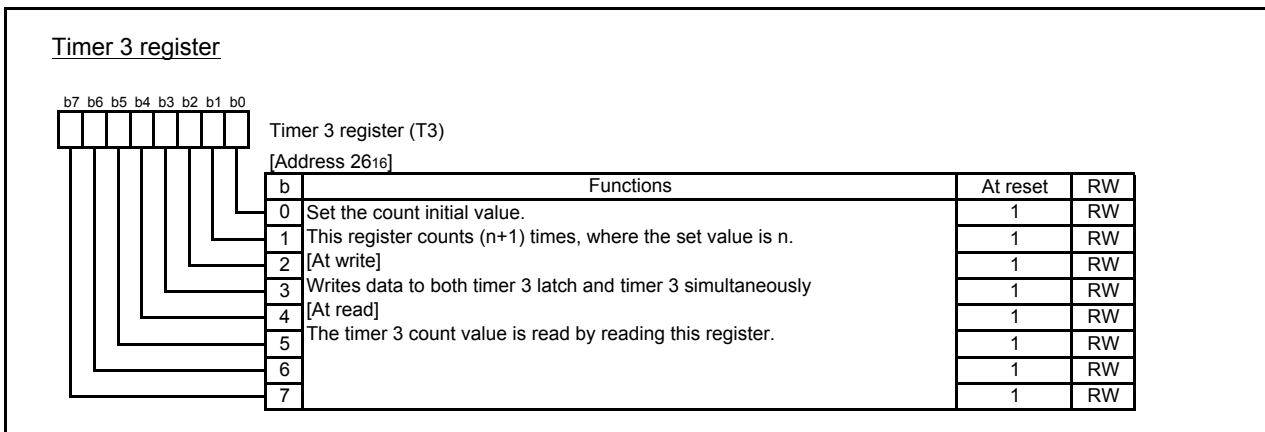


Fig. 4.22 Structure of Timer 3 register

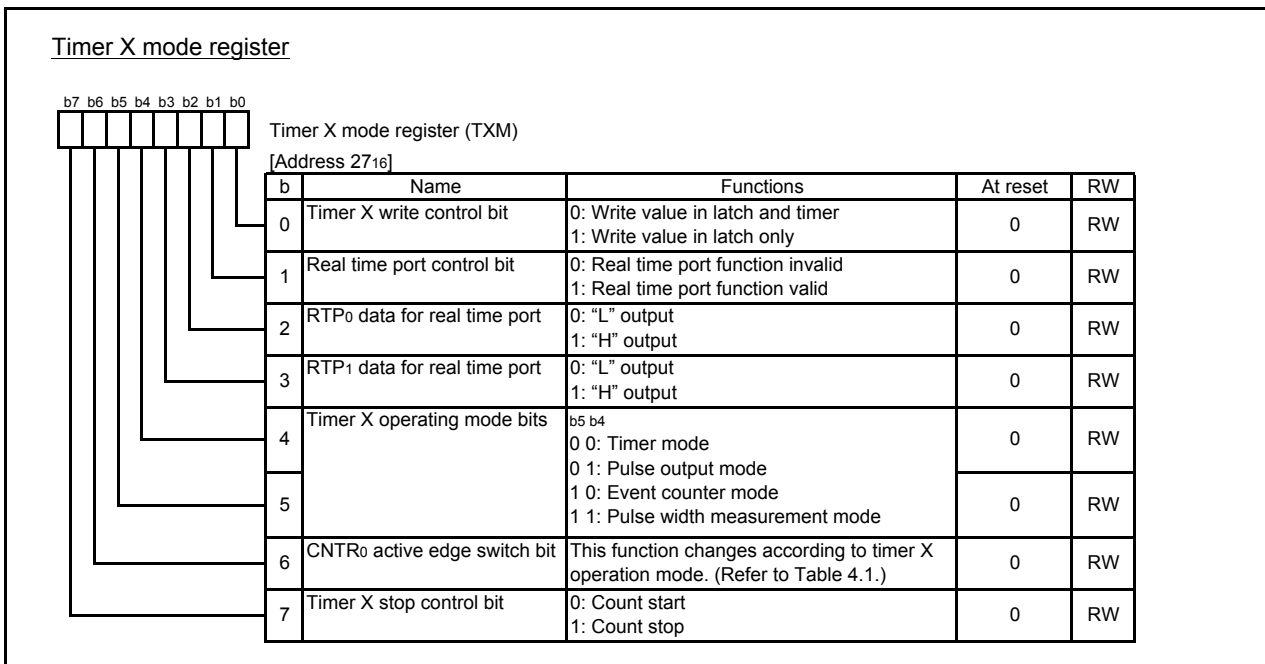


Fig. 4.23 Structure of Timer X mode register

Table 4.1 CNTR0 active edge switch bit function

Timer X operation mode	Set value	Timer function selection	CNTR0 interrupt request occurrence source
Timer mode	"0"	—	CNTR0 input signal falling edge (No influence to timer count)
	"1"	—	CNTR0 input signal rising edge (No influence to timer count)
Pulse output mode	"0"	Pulse output start from "H"	Output signal falling edge
	"1"	Pulse output start from "L"	Output signal rising edge
Event counter mode	"0"	Count at rising edge	Input signal falling edge
	"1"	Count at falling edge	Input signal rising edge
Pulse width measurement mode	"0"	Measure "H" pulse width	Input signal falling edge
	"1"	Measure "L" pulse width	Input signal rising edge

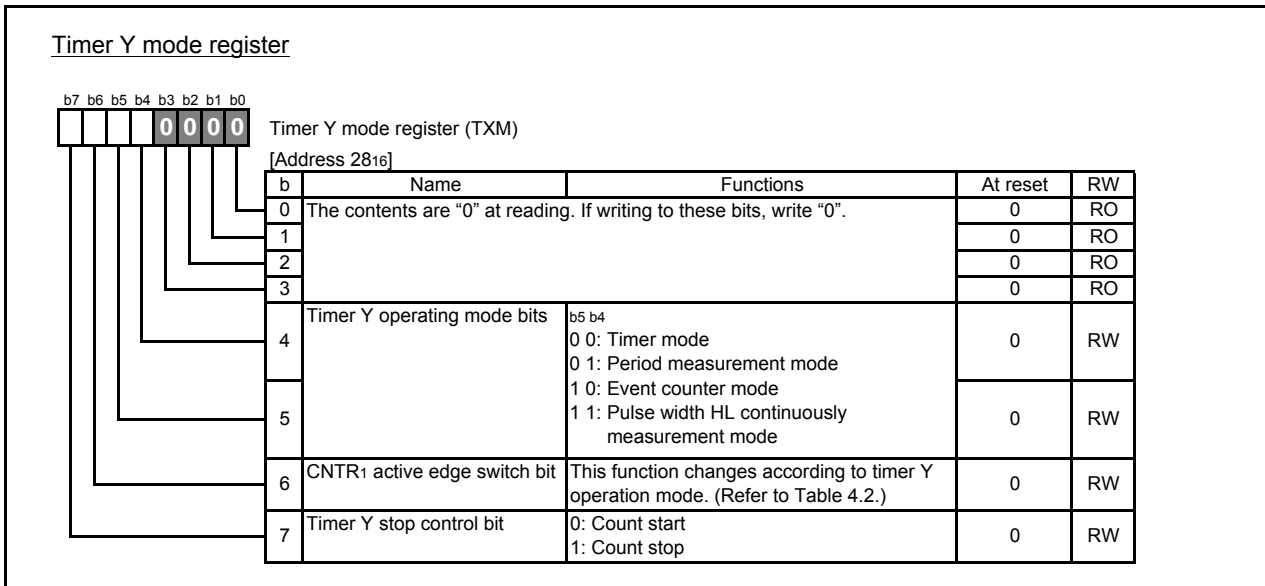


Fig. 4.24 Structure of Timer Y mode register

Table 4.2 CNTR1 active edge switch bit function

Timer Y operation mode	Set value	Timer function selection	CNTR1 interrupt request occurrence source
Timer mode	"0"	—	CNTR1 input signal falling edge (No influence to timer count)
	"1"	—	CNTR1 input signal rising edge (No influence to timer count)
Period measurement mode	"0"	Measures the falling edge to falling edge	Input signal falling edge
	"1"	Measures the rising edge to rising edge	Input signal rising edge
Event counter mode	"0"	Count at rising edge	Input signal falling edge
	"1"	Count at falling edge	Input signal rising edge
Pulse width HL continuously measurement mode	"0"	Measures "H" and "L" pulse widths	Input signal falling and rising edges
	"1"		

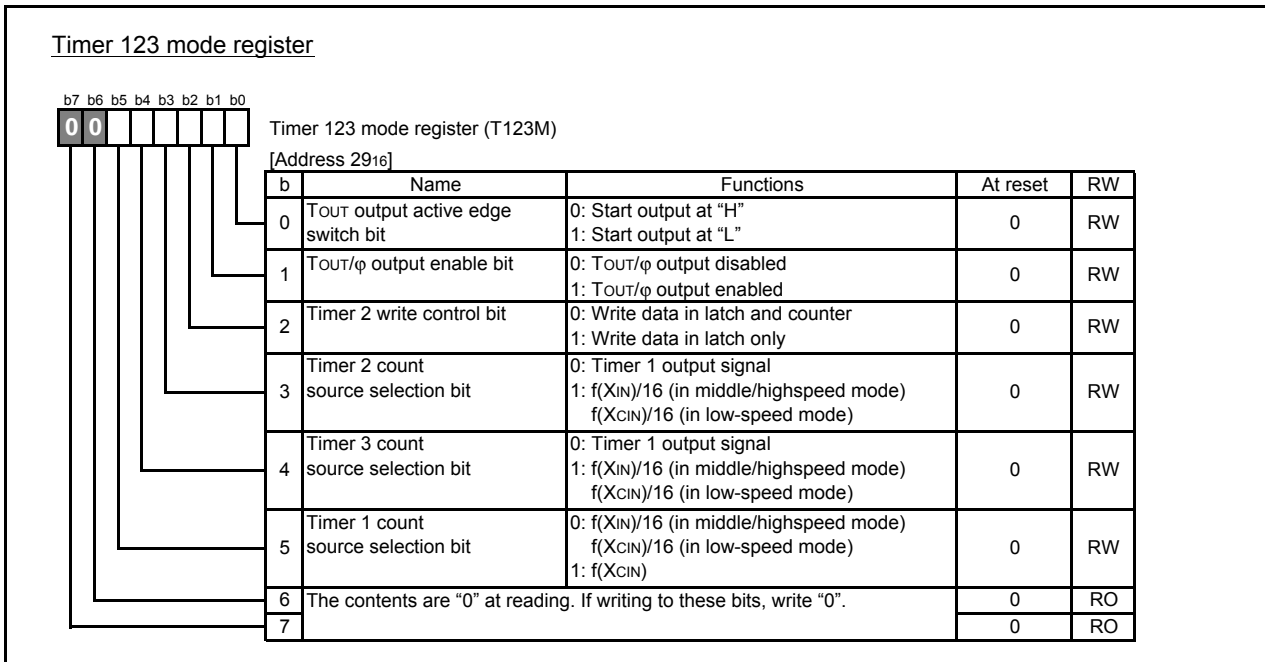


Fig. 4.25 Structure of Timer 123 mode register

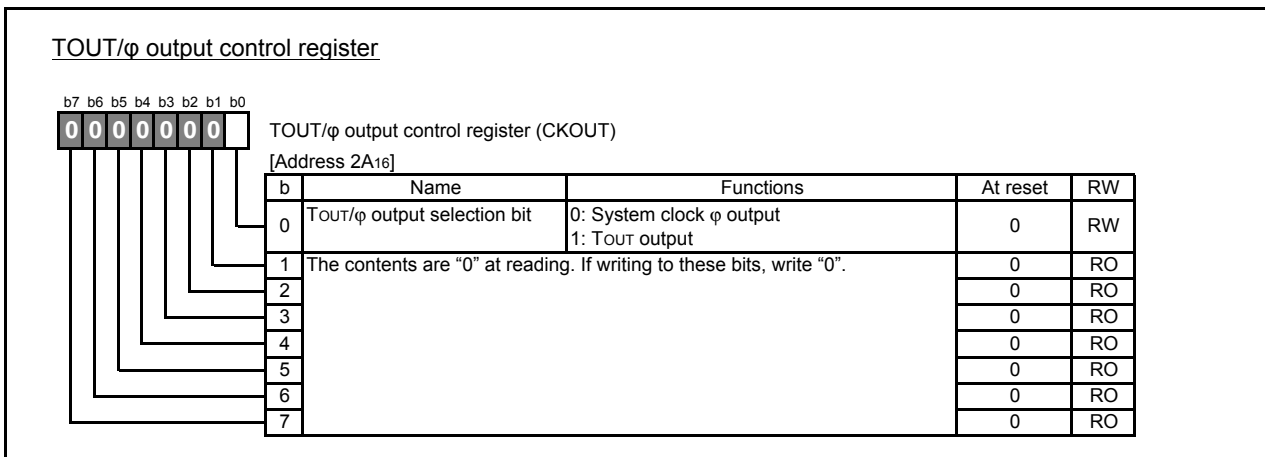


Fig. 4.26 Structure of TOUT/ φ output control register

PWM control register

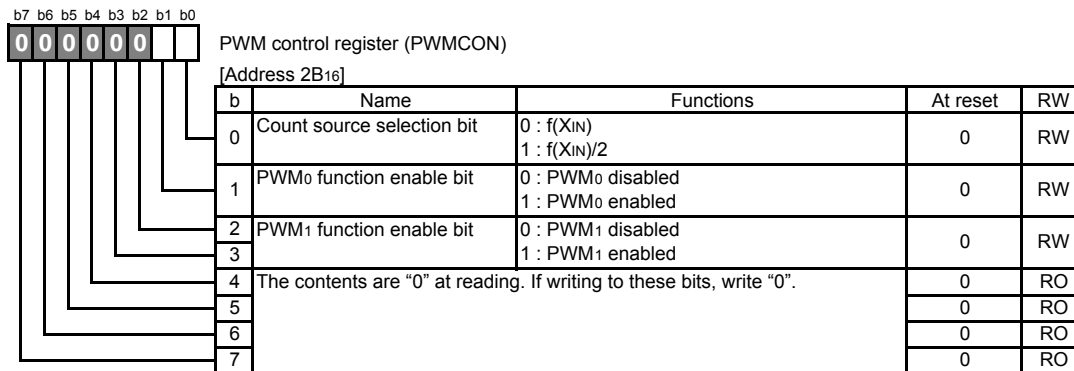


Fig. 4.27 Structure of PWM control register

PWM prescaler

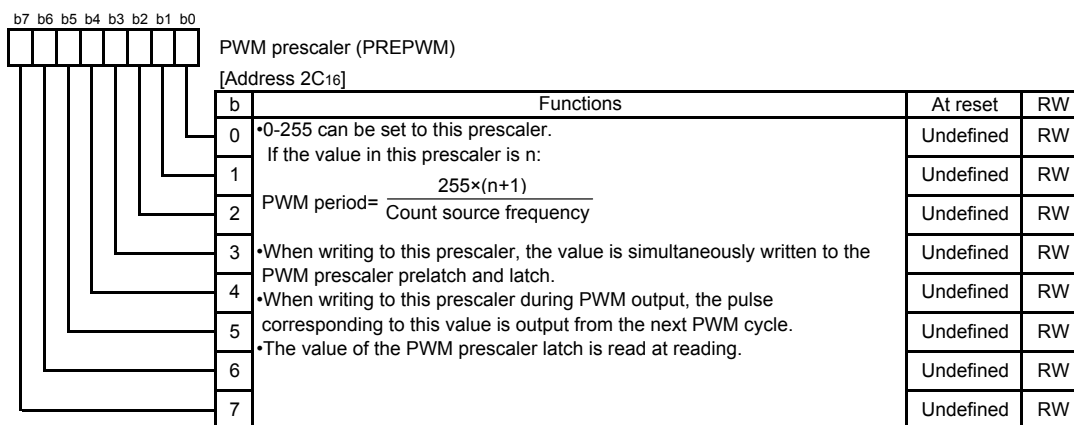


Fig. 4.28 Structure of PWM prescaler

PWM register

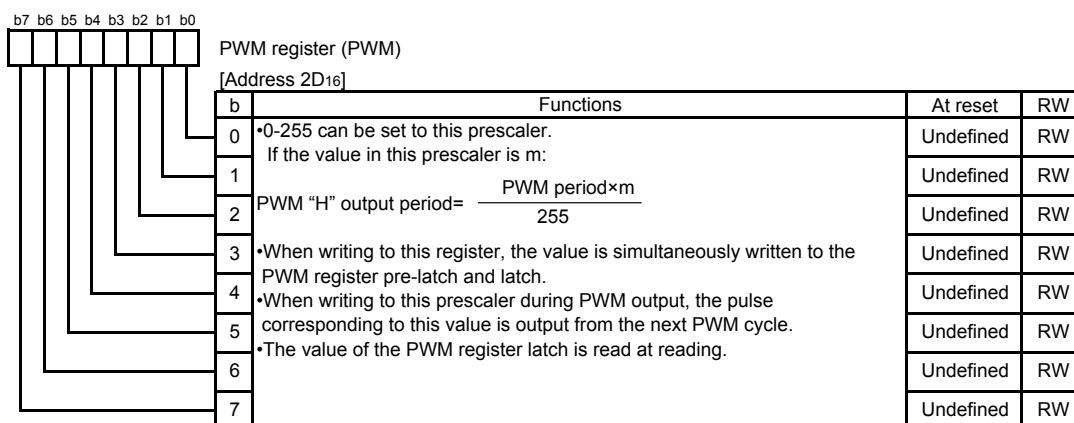


Fig. 4.29 Structure of PWM register

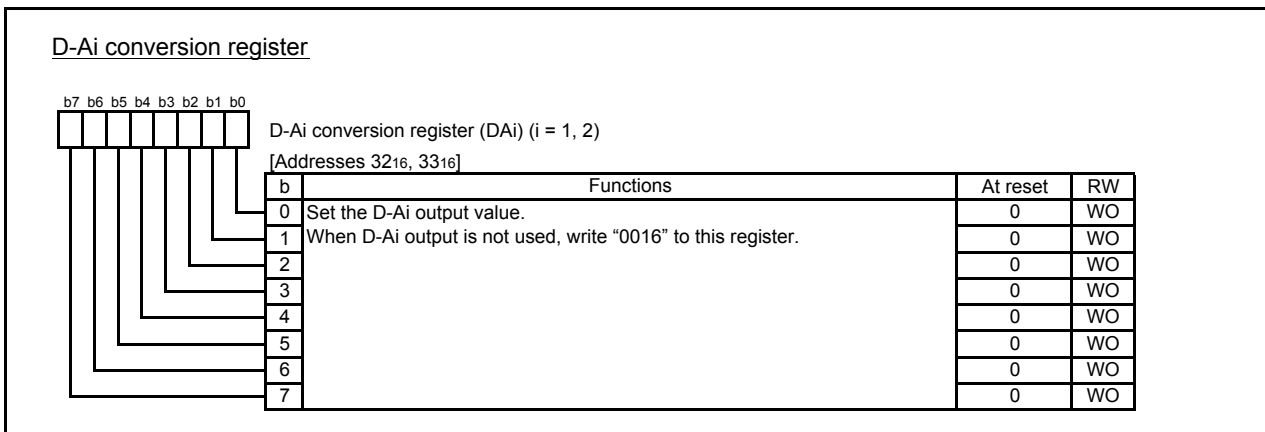


Fig. 4.30 Structure of D-Ai conversion register

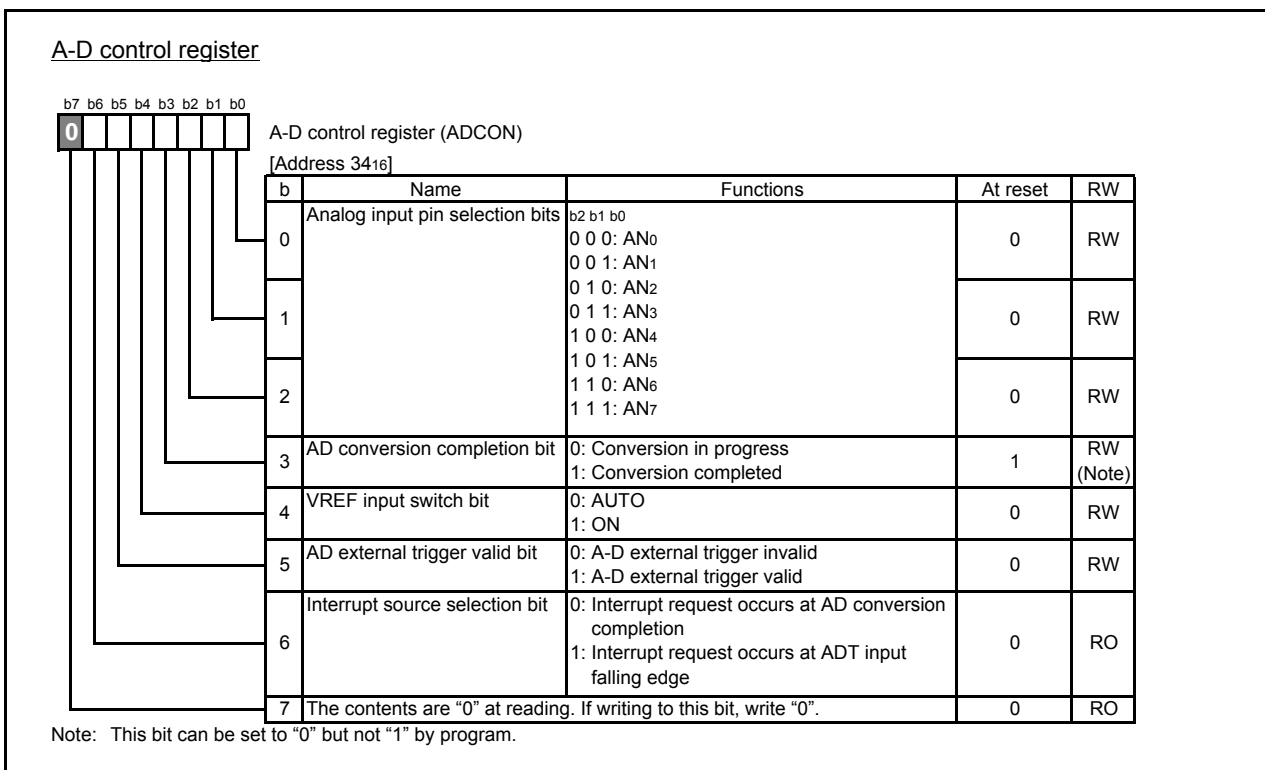


Fig. 4.31 Structure of A-D control register

A-D conversion high-order register

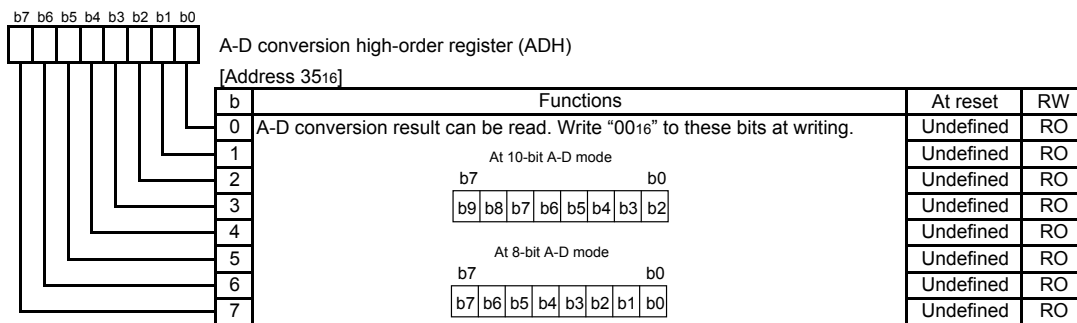


Fig. 4.32 Structure of A-D conversion high-order register

A-D conversion low-order register

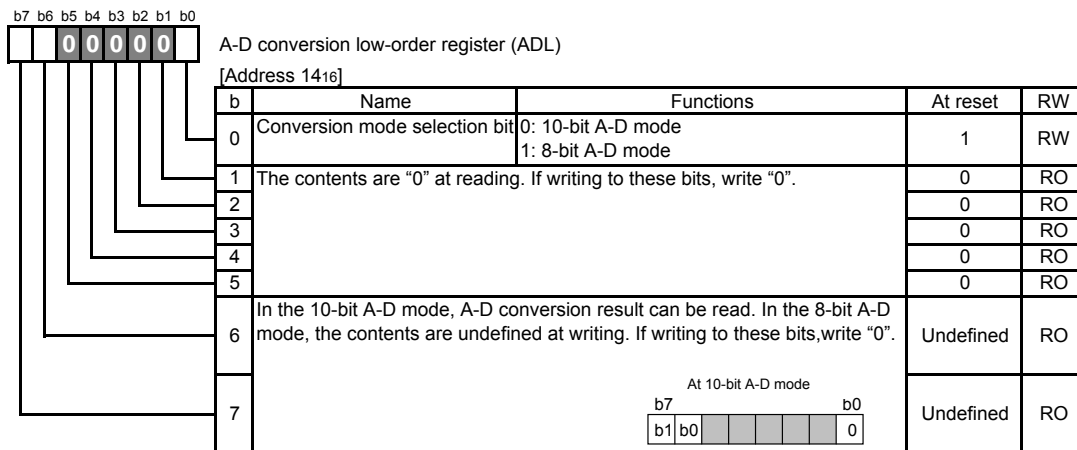


Fig. 4.33 Structure of A-D conversion low-order register

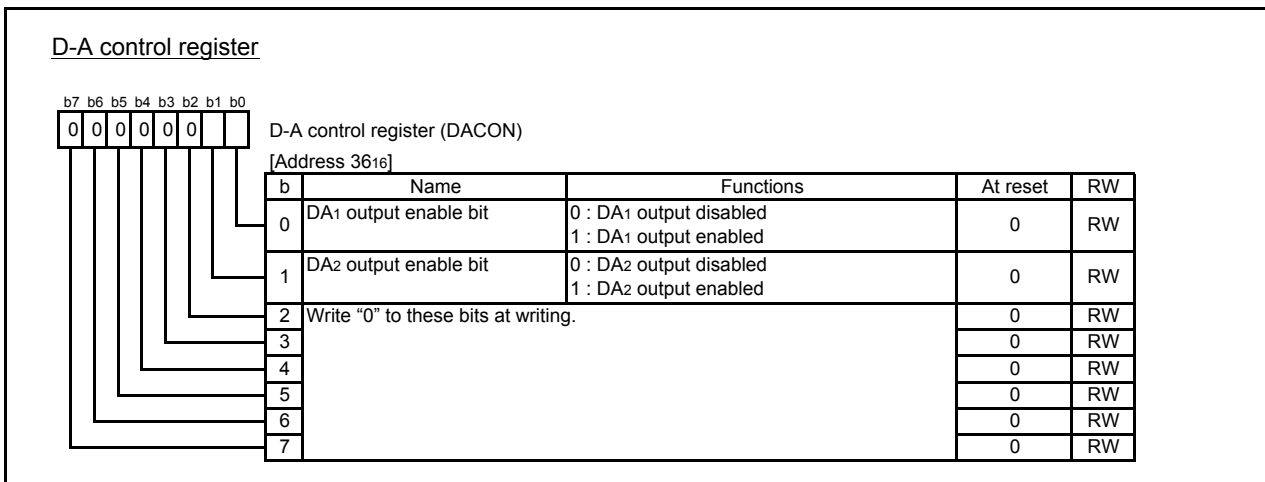


Fig. 4.34 Structure of D-A control register

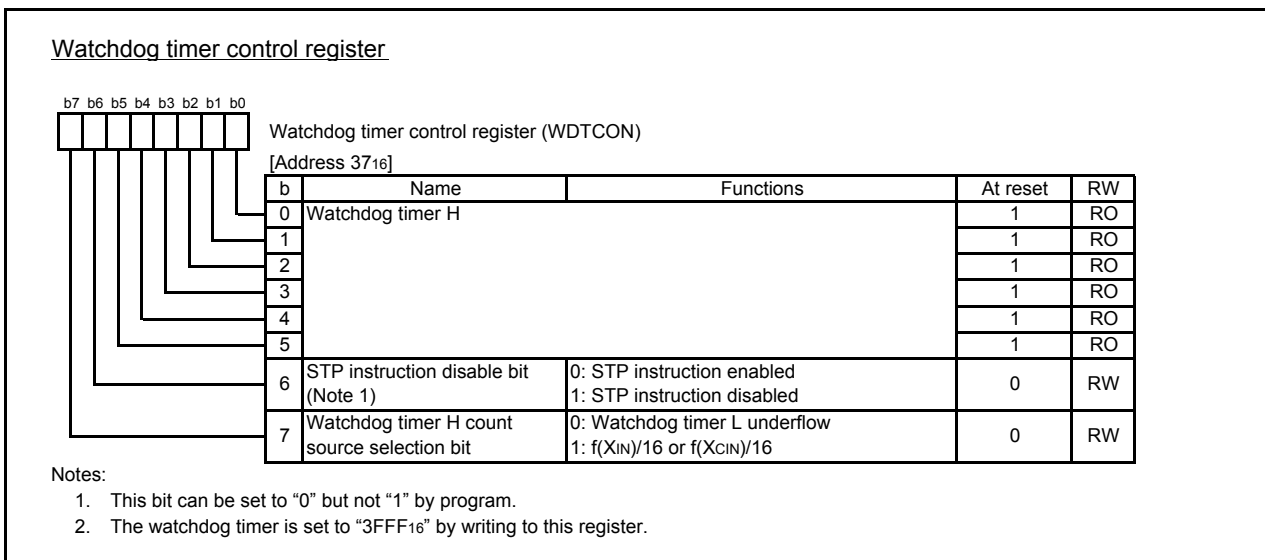


Fig. 4.35 Structure of Watchdog timer control register

Segment output enable register

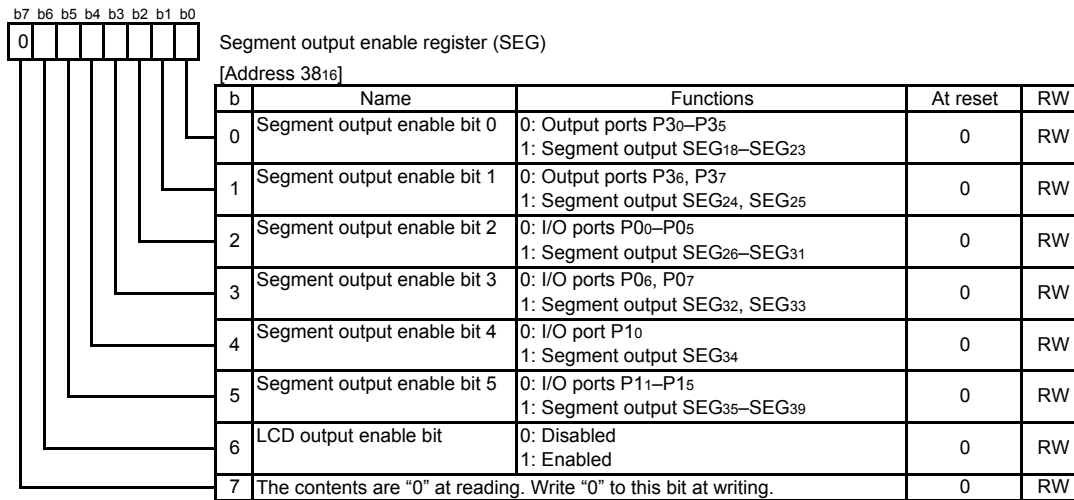
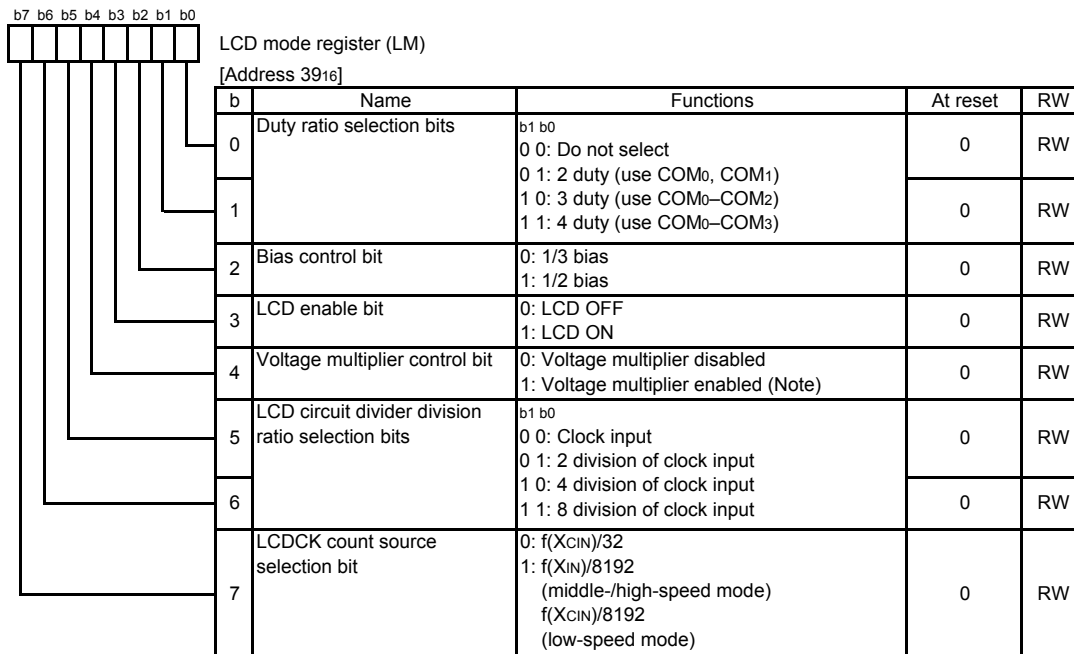


Fig. 4.36 Structure of Segment output enable register

LCD mode register



Note: When the voltage multiplier control bit is set to "1" (enabled), be sure to set the bias control bit to "0" (1/3 bias).

Fig. 4.37 Structure of LCD mode register

Interrupt edge selection register

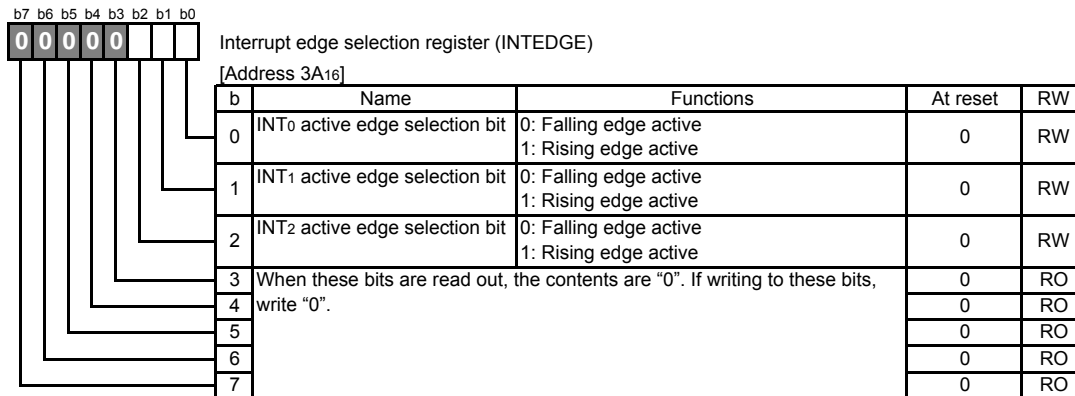


Fig. 4.38 Structure of Interrupt edge selection register

CPU mode register

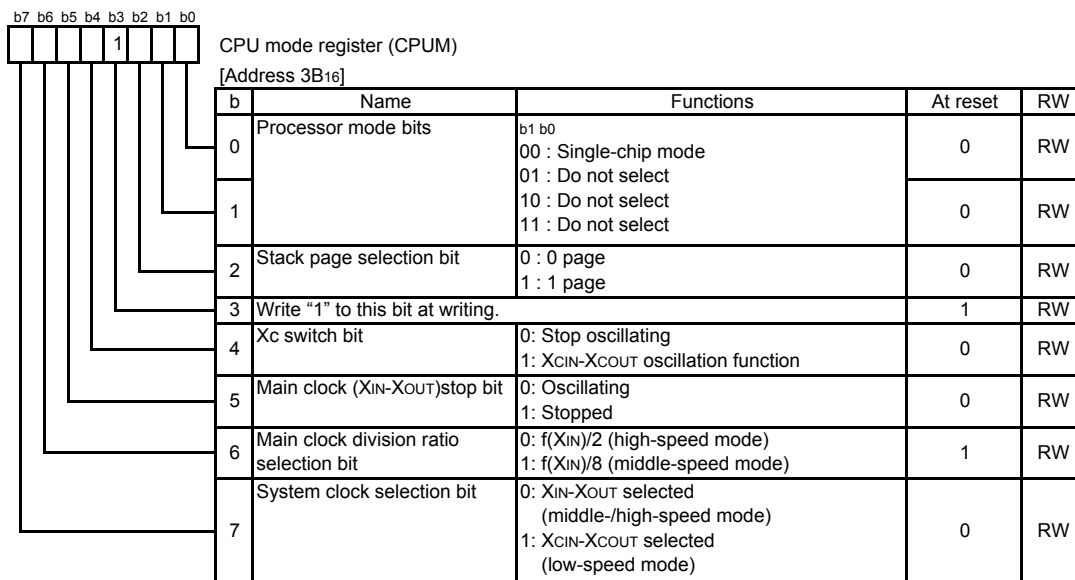
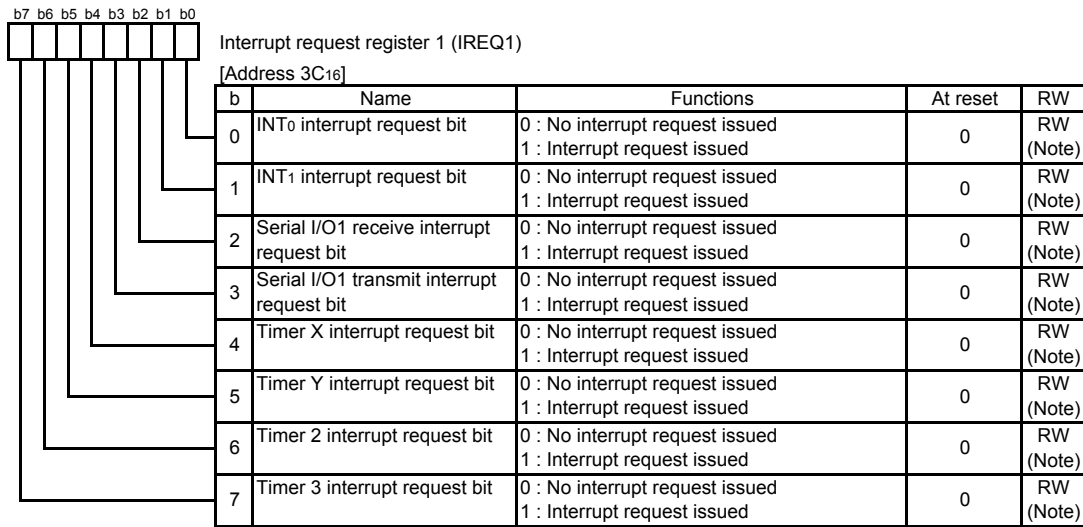


Fig. 4.39 Structure of CPU mode register

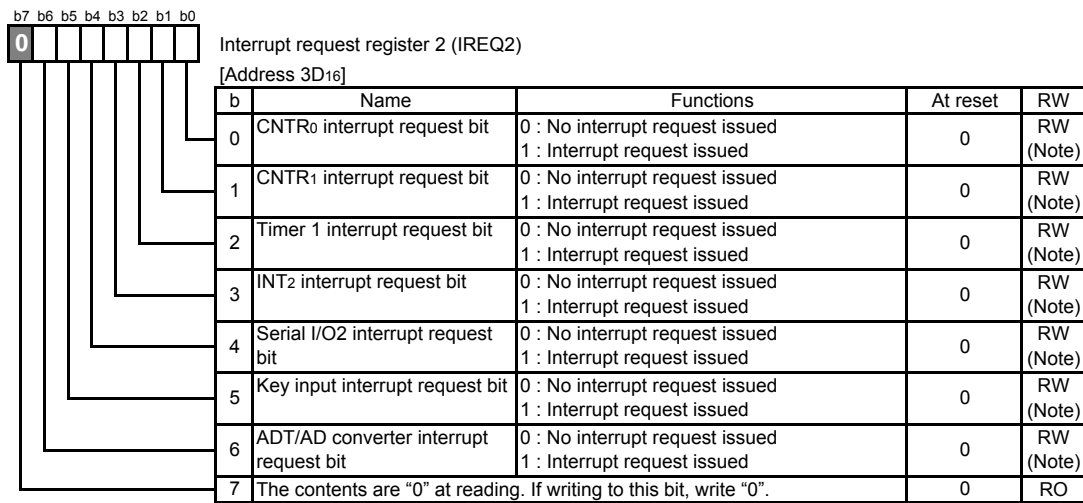
Interrupt request register 1



Note: This bit can be set to "0" but not to "1" by program.

Fig. 4.40 Structure of Interrupt request register 1

Interrupt request register 2



Note: This bit can be set to "0" but not to "1" by program.

Fig. 4.41 Structure of Interrupt request register 2

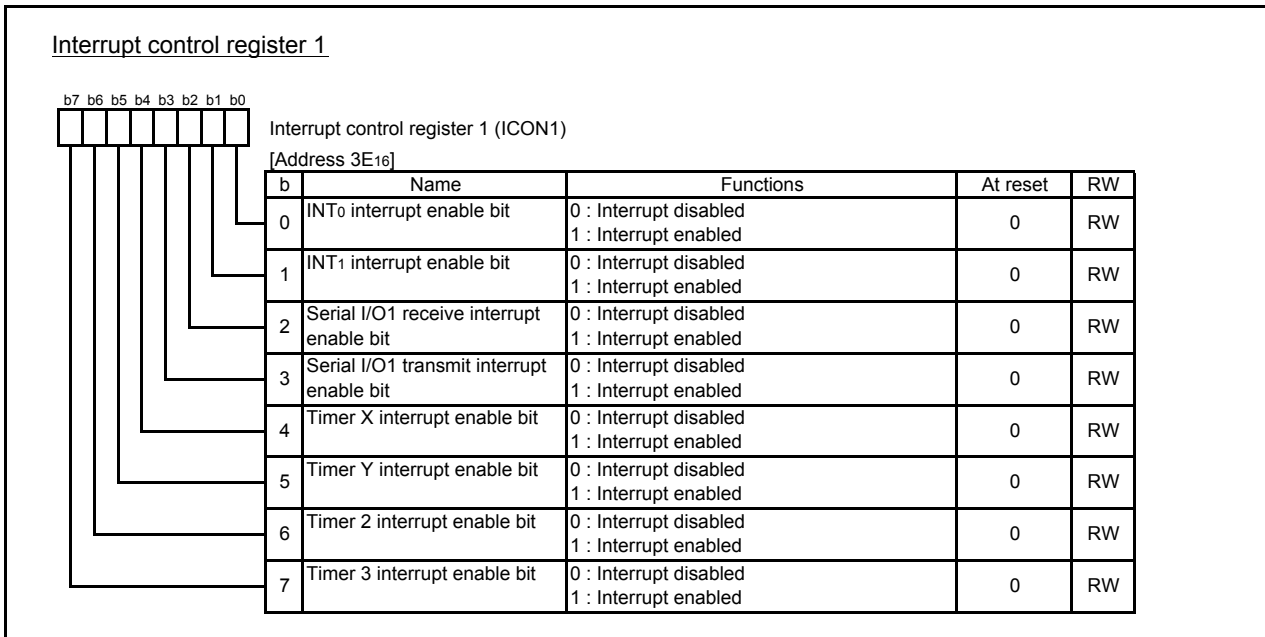


Fig. 4.42 Structure of Interrupt control register 1

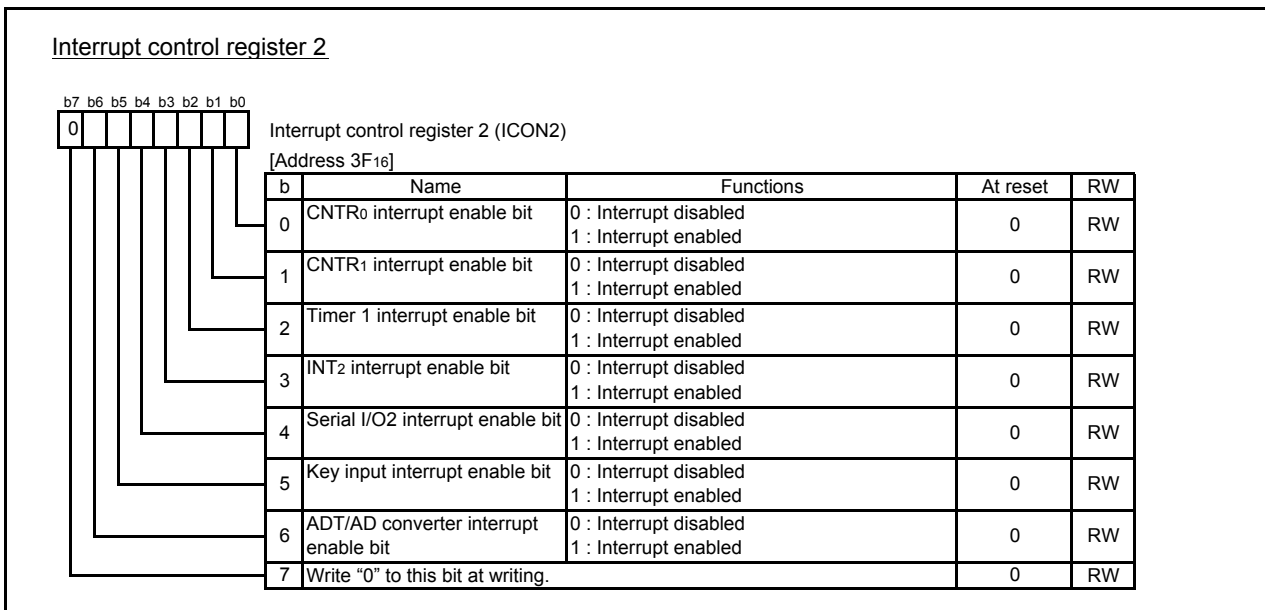


Fig. 4.43 Structure of Interrupt request register 2

LCD display RAM

address	bit	7	6	5	4	3	2	1	0	reset	RW
		COM3	COM2	COM1	COM0	COM3	COM2	COM1	COM0		
40 ₁₆	LRAM0	SEG1				SEG0				Undefined	RW
41 ₁₆	LRAM1	SEG3				SEG2				Undefined	RW
42 ₁₆	LRAM2	SEG5				SEG4				Undefined	RW
43 ₁₆	LRAM3	SEG7				SEG6				Undefined	RW
44 ₁₆	LRAM4	SEG9				SEG8				Undefined	RW
45 ₁₆	LRAM5	SEG11				SEG10				Undefined	RW
46 ₁₆	LRAM6	SEG13				SEG12				Undefined	RW
47 ₁₆	LRAM7	SEG15				SEG14				Undefined	RW
48 ₁₆	LRAM8	SEG17				SEG16				Undefined	RW
49 ₁₆	LRAM9	SEG19				SEG18				Undefined	RW
4A ₁₆	LRAM10	SEG21				SEG20				Undefined	RW
4B ₁₆	LRAM11	SEG23				SEG22				Undefined	RW
4C ₁₆	LRAM12	SEG25				SEG24				Undefined	RW
4D ₁₆	LRAM13	SEG27				SEG26				Undefined	RW
4E ₁₆	LRAM14	SEG29				SEG28				Undefined	RW
4F ₁₆	LRAM15	SEG31				SEG30				Undefined	RW
50 ₁₆	LRAM16	SEG33				SEG32				Undefined	RW
51 ₁₆	LRAM17	SEG35				SEG34				Undefined	RW
52 ₁₆	LRAM18	SEG37				SEG36				Undefined	RW
53 ₁₆	LRAM19	SEG39				SEG38				Undefined	RW

Fig. 4.44 LCD display RAM

5. Reference

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Data Sheet
7560 Group (A version) Data sheet
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Revision Record

Rev.	Date	Description	
		Page	Summary
1.00	Jul.09.04	—	First edition issued

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