

To our customers,

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April 1<sup>st</sup>, 2010  
Renesas Electronics Corporation

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## 7548/7549 Group

### Watchdog Timer

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#### 1. Abstract

The following article introduces and shows an example of how to use the Watchdog Timer on the 7548/7549 Group device.

#### 2. Introduction

The application explained in this document applies to the following MCU and parameter(s):

Applicable MCU: 7548/7549 Group  
Oscillation frequency: 4 MHz

Function set ROM data 0 to 2 are areas used to set peripheral functions by data written to the QzROM and can not be set by program. Data set to these areas are valid after a reset of the MCU is released. Make sure to set values according to the user system regardless of the use of peripheral functions. Set values used in this sample program are as follows.

Function set ROM data 0 FSR0M0 (address FFD8h): 10000000b  
Function set ROM data 1 FSR0M1 (address FFD9h): 10000001b  
Function set ROM data 2 FSR0M2 (address FFDAh): 00001001b

This sample program may include operations of unused bit functions for the convenience of the SFR bit layout. Set the values according to the operational conditions of the user system.

### 3. Contents

#### 3.1 Watchdog Timer

Outline: If a program runs out of control, the MCU returns to reset status by the watchdog timer for internal program runaway detection.

Specifications:

- The watchdog timer enabled.
- High-speed mode of XIN (Note) is used for the internal clock  $\phi$ .
- Select XIN (Note)/16 as the count source for the watchdog timer and select an underflow signal from the watchdog timer L as the count source for the watchdog timer H.
- Before the watchdog timer underflows, writing to the watchdog timer control register is performed at every cycle in the main routine.
- Stop mode is not used.

Note: After releasing reset, the low-speed on-chip oscillator is used until the internal clock is switched to XIN.

Figure 3.1 shows the Watchdog Timer Connection and Division Ratio Setting, Figure 3.2 shows the Relevant Register Settings, and Figure 3.3 shows the Control Procedure.

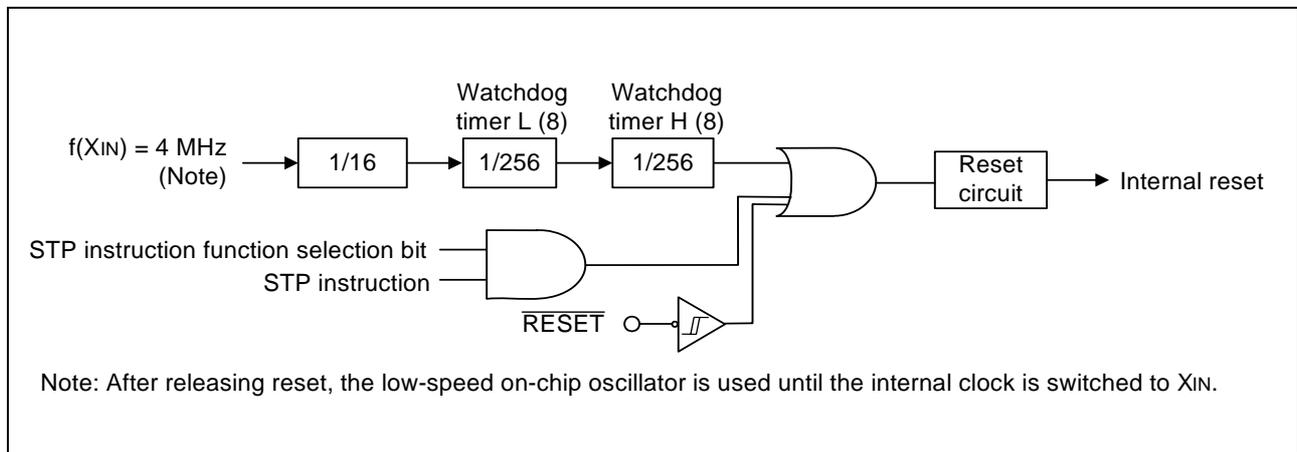


Figure 3.1 Watchdog Timer Connection and Division Ratio Setting

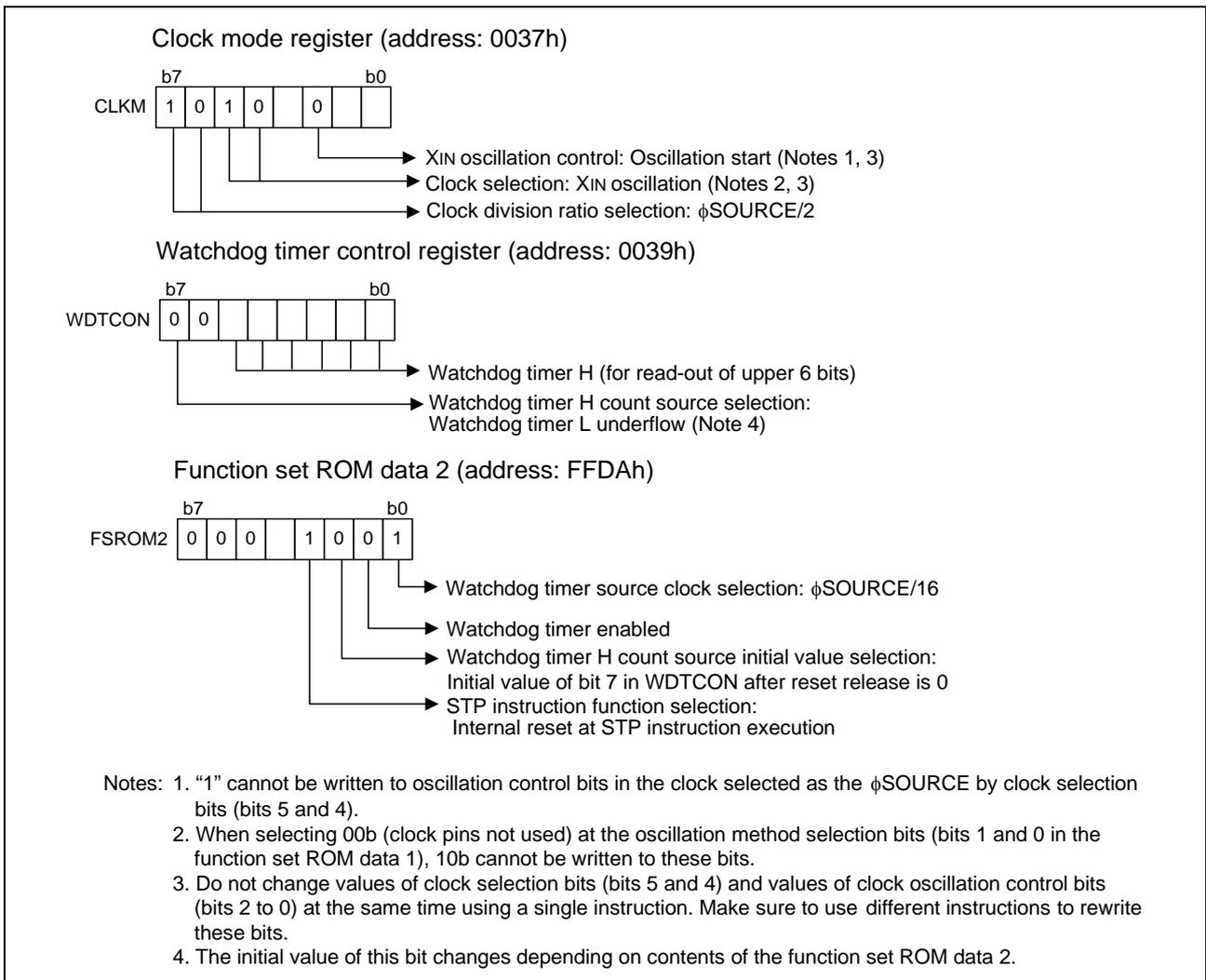


Figure 3.2 Relevant Register Settings

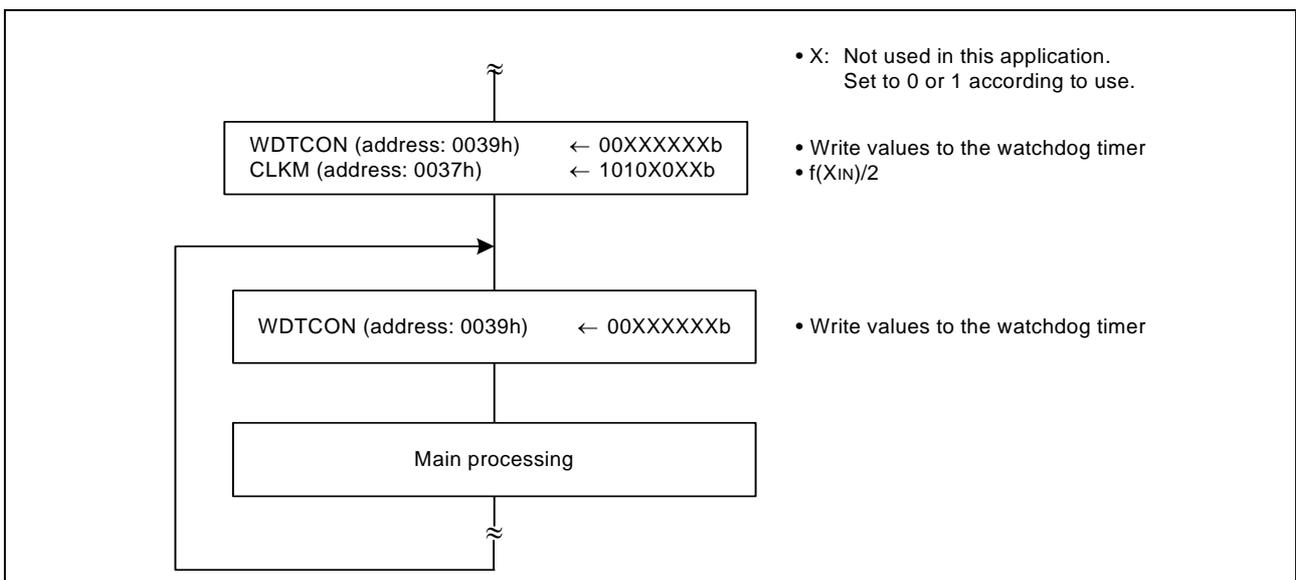


Figure 3.3 Control Procedure

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#### 4. Sample Programming Code

Download a sample program from the Renesas Technology website.

To download, click “Application Notes” in the left side menu on the page of the 7548/7549 Group.

#### 5. Reference Document

Datasheet

7548/7549 Group Datasheet

Download the latest version from the Renesas Technology website.

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REVISION HISTORY	7548/7549 Group Watchdog Timer
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Rev.	Date	Description	
		Page	Summary
1.00	Mar 26, 2007	–	First Edition issued
2.00	Oct 01, 2007	2	One of specifications revised
		3	Figure 3.2 FSR0M2 revised
			Note 1 revised

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