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April 1st, 2010
Renesas Electronics Corporation

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7548/7549 Group

AD Converter

1. Abstract

The following article introduces and shows an example of how to use the AD Converter on the 7548/7549 Group device.

2. Introduction

The application explained in this document applies to the following MCU:

Applicable MCU: 7548/7549 Group

Function set ROM data 0 to 2 are areas used to set peripheral functions by data written to the QzROM and can not be set by program. Data set to these areas are valid after a reset of the MCU is released. Make sure to set values according to the user system regardless of the use of peripheral functions. Set values used in this sample program are as follows.

Function set ROM data 0 FSROM0 (address FFD8h): 10000000b

Function set ROM data 1 FSROM1 (address FFD9h): 10000001b

Function set ROM data 2 FSROM2 (address FFDAh): 00001011b

This sample program may include operations of unused bit functions for the convenience of the SFR bit layout. Set the values according to the operational conditions of the user system.

3. Contents

3.1 Analog Signal Read

Outline: The analog input voltage from a sensor is converted to digital values.

Specifications:

- The analog input voltage from a sensor is converted to digital values.
- The P14/AN4 pin is used as an analog input pin.

Figure 3.1 shows the Connection Diagram, Figure 3.2 shows the Relevant Register Settings, and Figure 3.3 shows the Control Procedure.

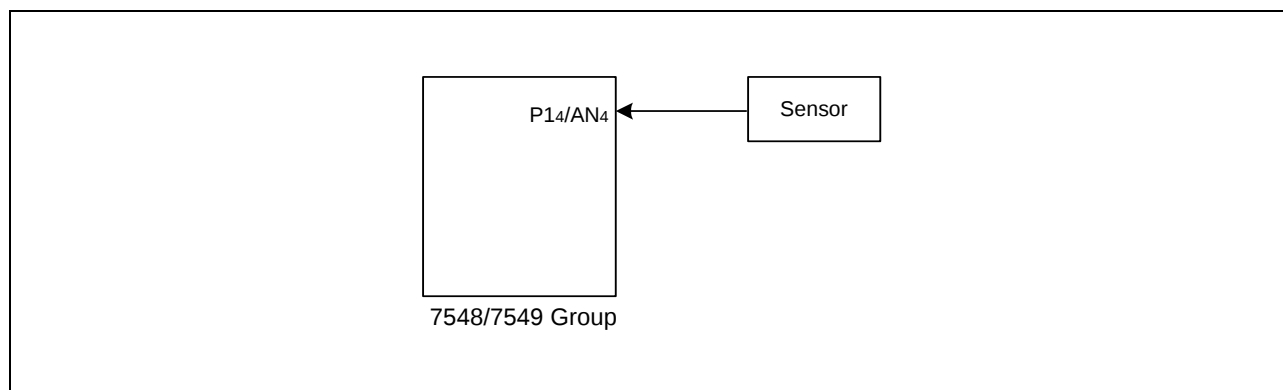
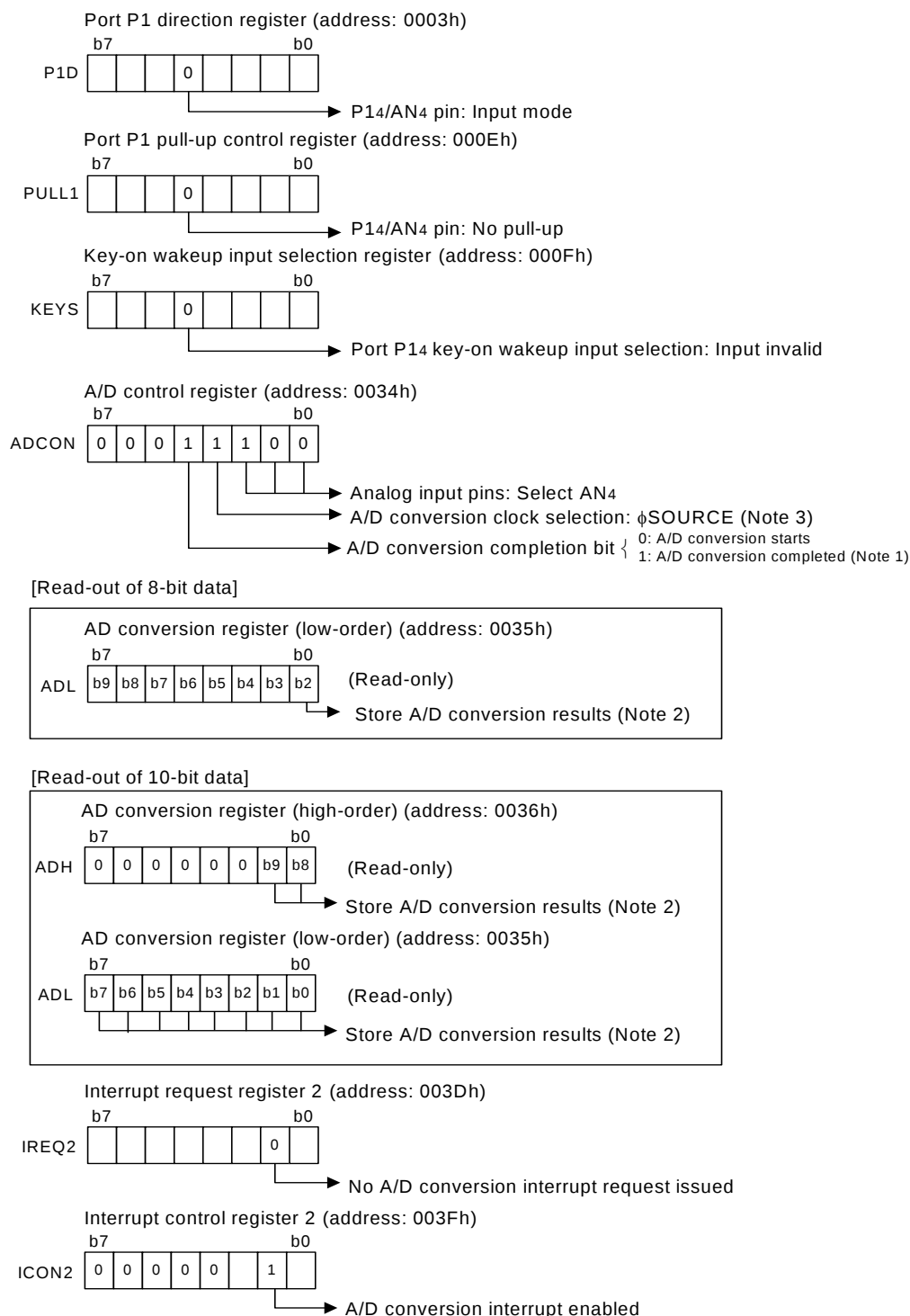


Figure 3.1 Connection Diagram



- Notes: 1. A/D conversion is started when A/D conversion completion bit is set to 0.
Only 0 is valid when writing to A/D conversion completion bit and even if 1 is written, this bit is not set to 1. Therefore, when writing value to ADCON without affecting A/D conversion completion bit, set A/D conversion completion bit to 1.
2. Read the A/D conversion result after AD conversion completion bit is set to 1.
When reading 8-bit data, read only the address 0035h. When reading 10-bit data, read from the address 0036h to the address 0035h.
3. ϕ SOURCE is the clock selected by bits 5 and 4 at the clock mode register (address 0037h).
Timer count sources are not affected by bits 7 and 6 (clock dividing ratio selection bits).

Figure 3.2 Relevant Register Settings

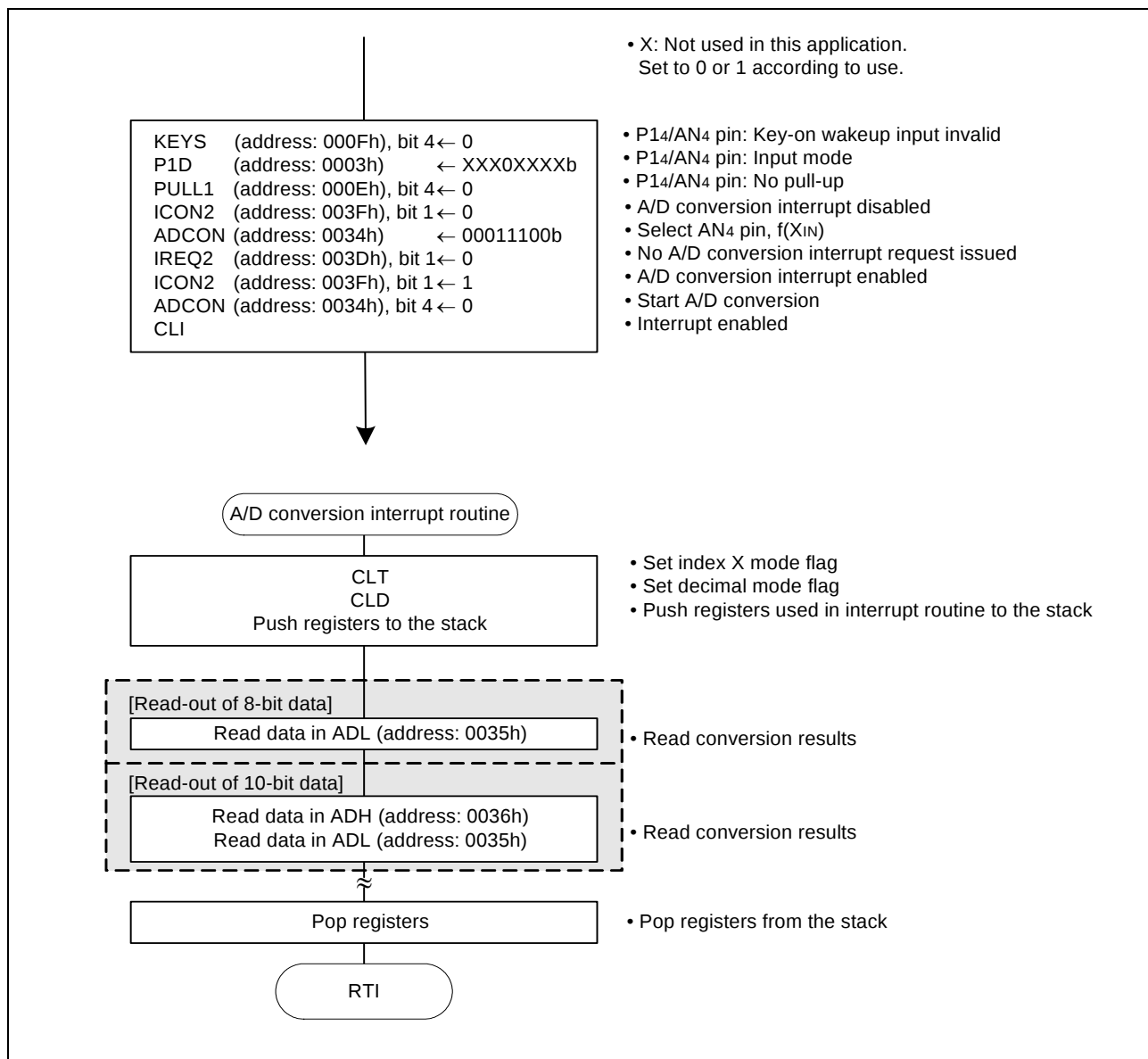


Figure 3.3 Control Procedure

4. Sample Programming Code

Download a sample program from the Renesas Technology website.

To download, click “Application Notes” in the left side menu on the page of the 7548/7549 Group.

5. Reference

Datasheet

7548/7549 Group Datasheet

Download the latest version from the Renesas Technology website.

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REVISION HISTORY	7548/7549 Group AD Converter
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Rev.	Date	Description	
		Page	Summary
1.00	Mar 26, 2007	–	First Edition issued

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