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April 1st, 2010
Renesas Electronics Corporation

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7546/7547 Group

Operation of Timer A (Output Compare Mode)

1. Abstract

The following article introduces and shows an application example of output compare normal mode of timer A.

2. Introduction

The explanation of this issue is applied in the following condition:

- Application MCU: M37546 Group
M37547 Group
- Oscillation frequency: 8MHz

3. Contents

3.1 Description of the application example

- Description
 - Outputs Timer A underflow waveform from P02. The output level will invert when the timer A underflow. The period of timer A is 40ms.
 - Outputs compare waveform from compare channel 0. At first, the phase of the output waveform is at 0ms of one period and the pulse width is 10% period (4ms). Then the pulse width will turn longer 4ms and the phase will delay 4ms every time timer A underflow. If the positive pulse width too longer to output in one period, the waveform will change to the first status and continuously output.
- Operation
 - Selecting external oscillator and setting clock division ratio high-speed.
 - Initialize SFR.
 - Enable timer A and compare (compare 00 match) interrupt.
 - Start timer A and then output the waveform form CMP0 and P02.
 - Rewrite compare latch 00 and 01 value in the compare interrupt service routine.
 - Setting compare latch 00 and 01 reload bit (CMPR.0) to “1”, and then the compare latch will reload from the compare buffer at next timer A underflow.
 - Invert P02 output level to show timer A underflow in the timer A interrupt service routine.

The operation timing, the compare output waveform and the timer A underflow waveform are shown in Fig.1.

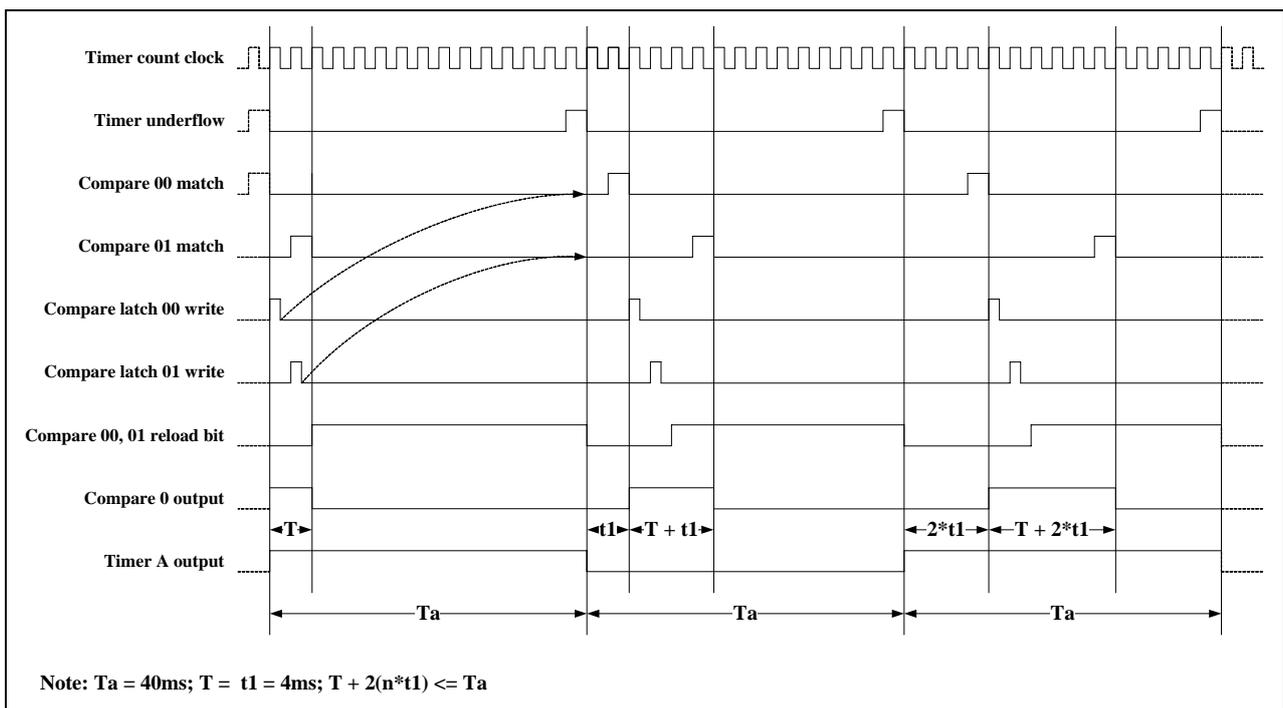
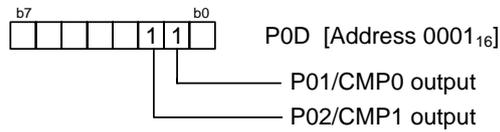


Fig.1: The Operate Timing and Output Waveform of Output Compare Mode

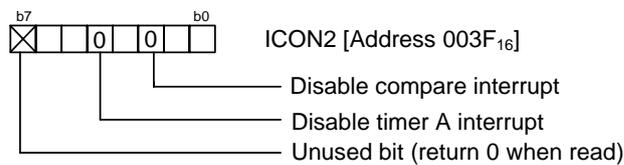
3.2 Register setting

The setup procedures of output compare 0 are shown as follow. When use compare 1~3, the procedures are same as these.

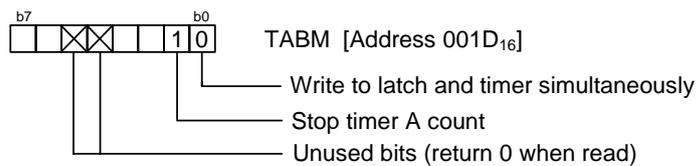
(1) Setting Port P0 direction register



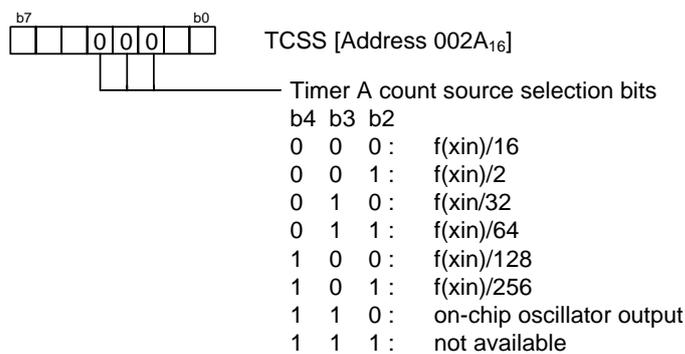
(2) Setting interrupt control register 2



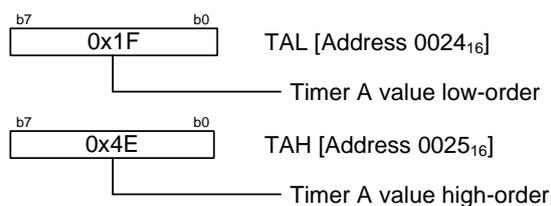
(3) Setting timer A,B mode register



(4) Setting timer count source set register

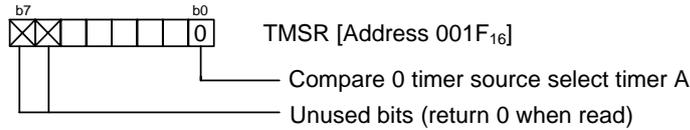


(5) Setting timer A register

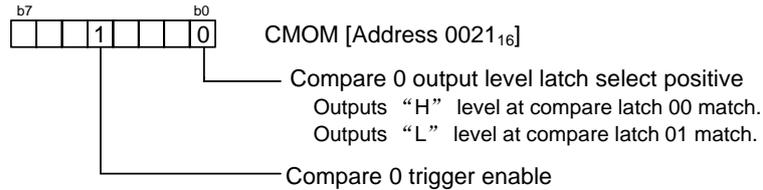


Note: Write to the low-order of timer A first, and the high-order of timer A next and be sure to write both low-order and high-order.

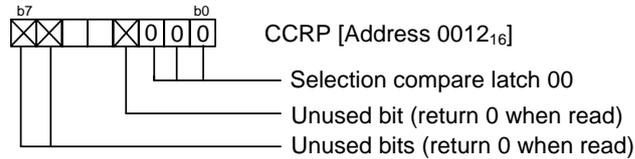
(6) Setting Timer source selection register



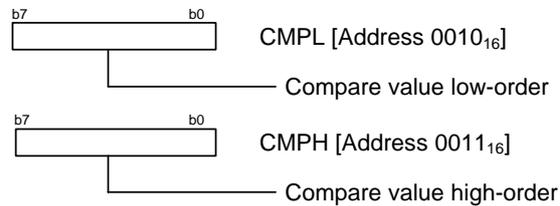
(7) Setting compare output mode register



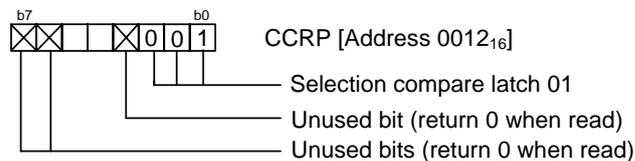
(8) Setting capture/compare register R/W pointer



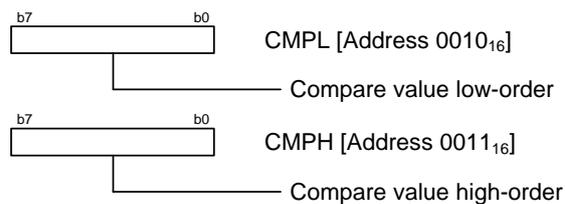
(9) Setting compare latch 00



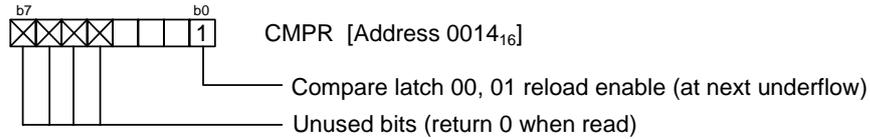
(10) Setting capture/compare register R/W pointer



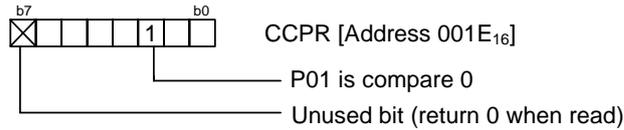
(11) Setting compare latch 01



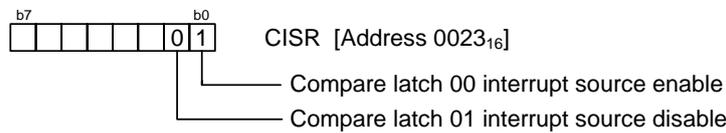
(12) Setting compare register re-load register



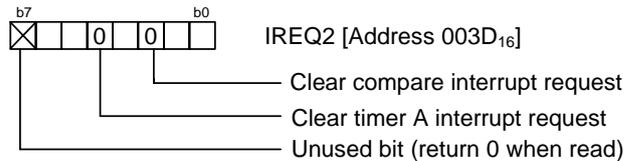
(13) Setting capture/compare port register



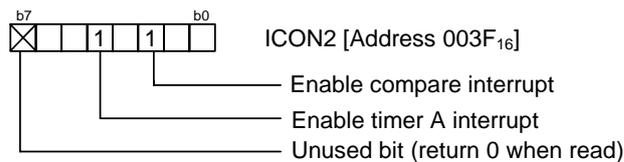
(14) Setting compare interrupt source register



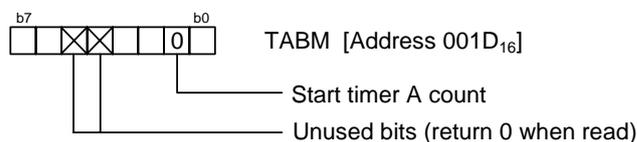
(15) Setting interrupt request register 2



(16) Setting interrupt control register 2



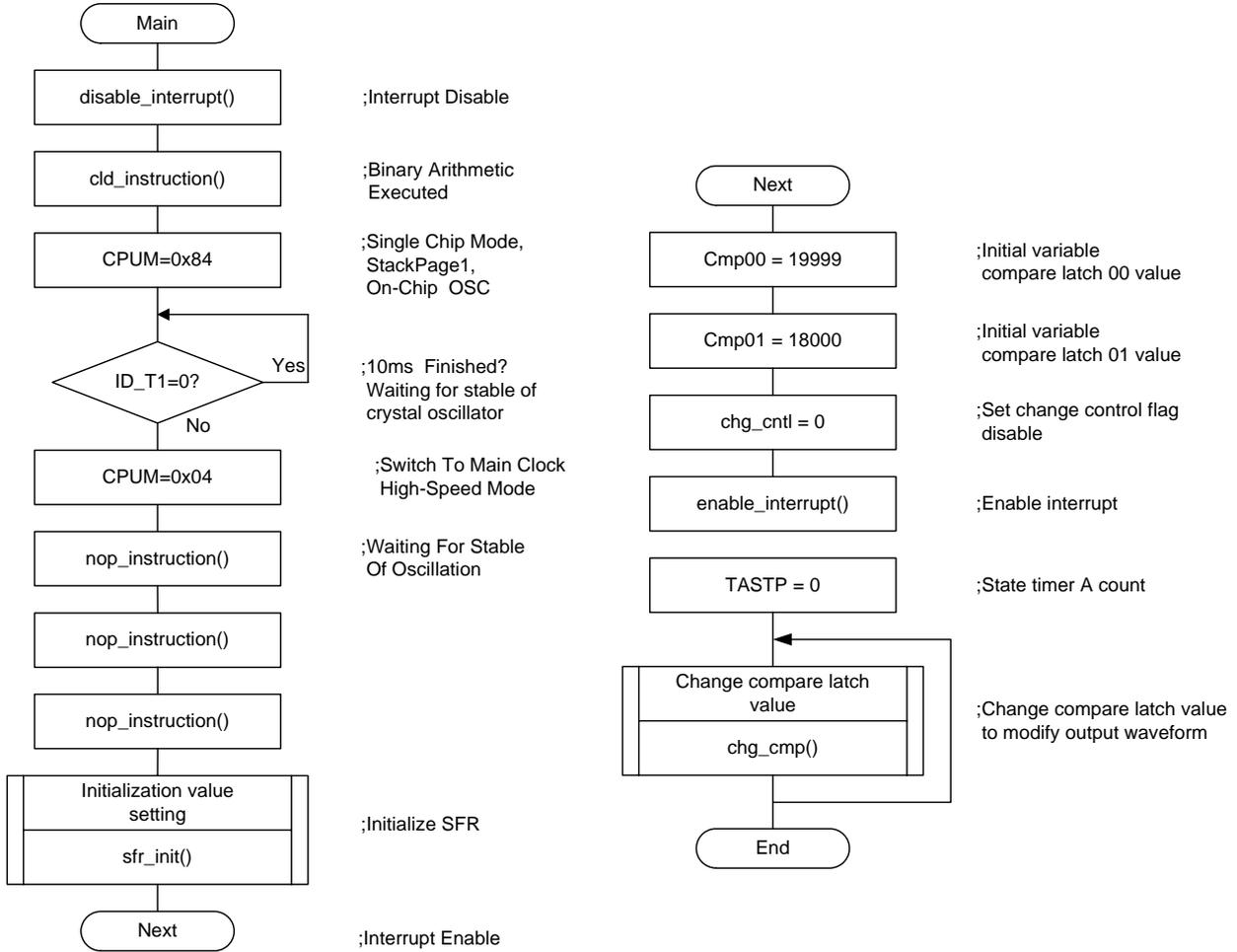
(17) Setting timer A,B mode register



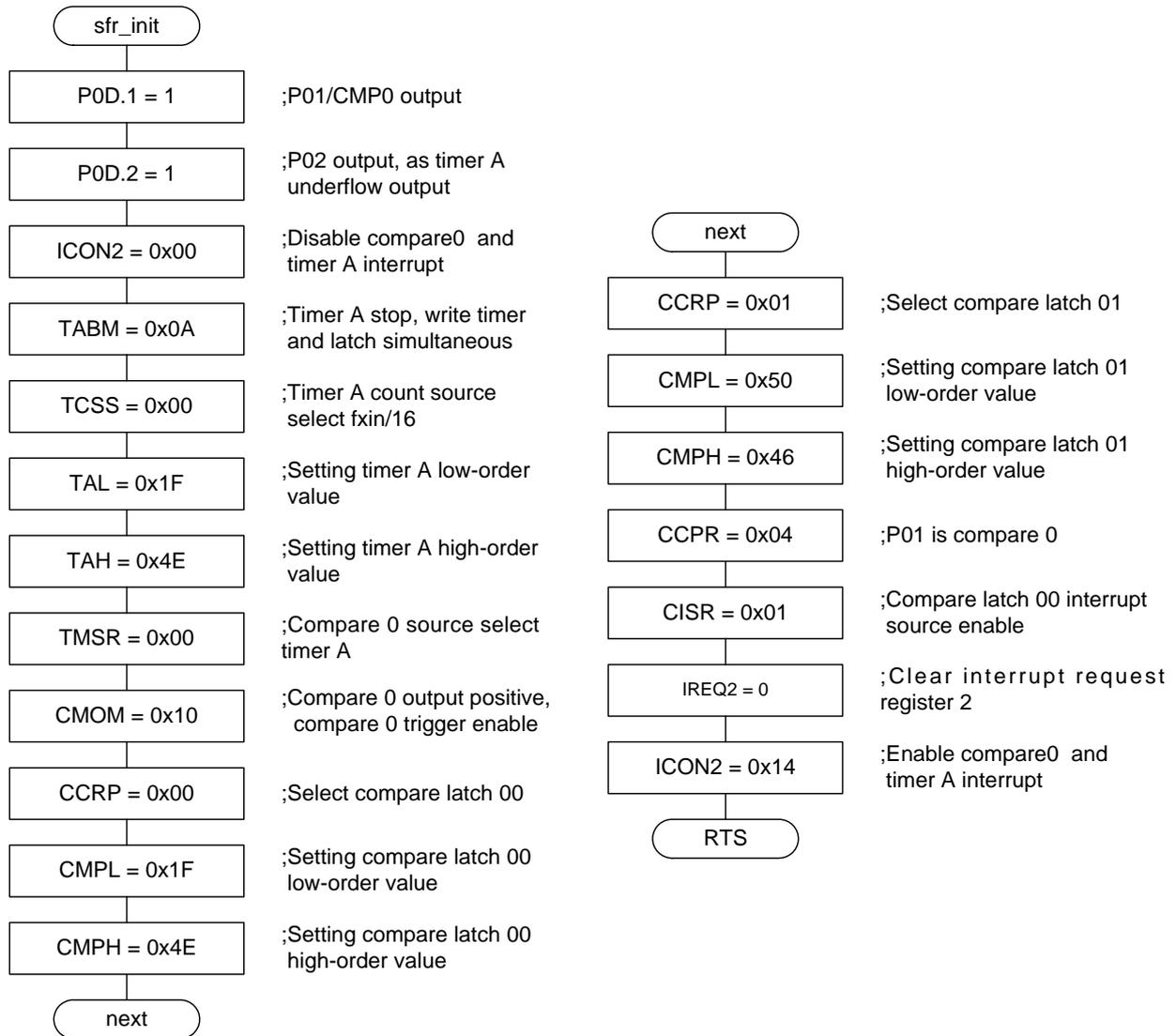
Note: To change compare 0 output waveform when timer A is running, repeat procedures from step (8) to step (12). Must set compare latch 00, 01 reload bit to “1” (reload at next underflow). The compare latch value will be written from compare buffer at next timer underflow. And the output waveform will be changed.

4. Flow chart

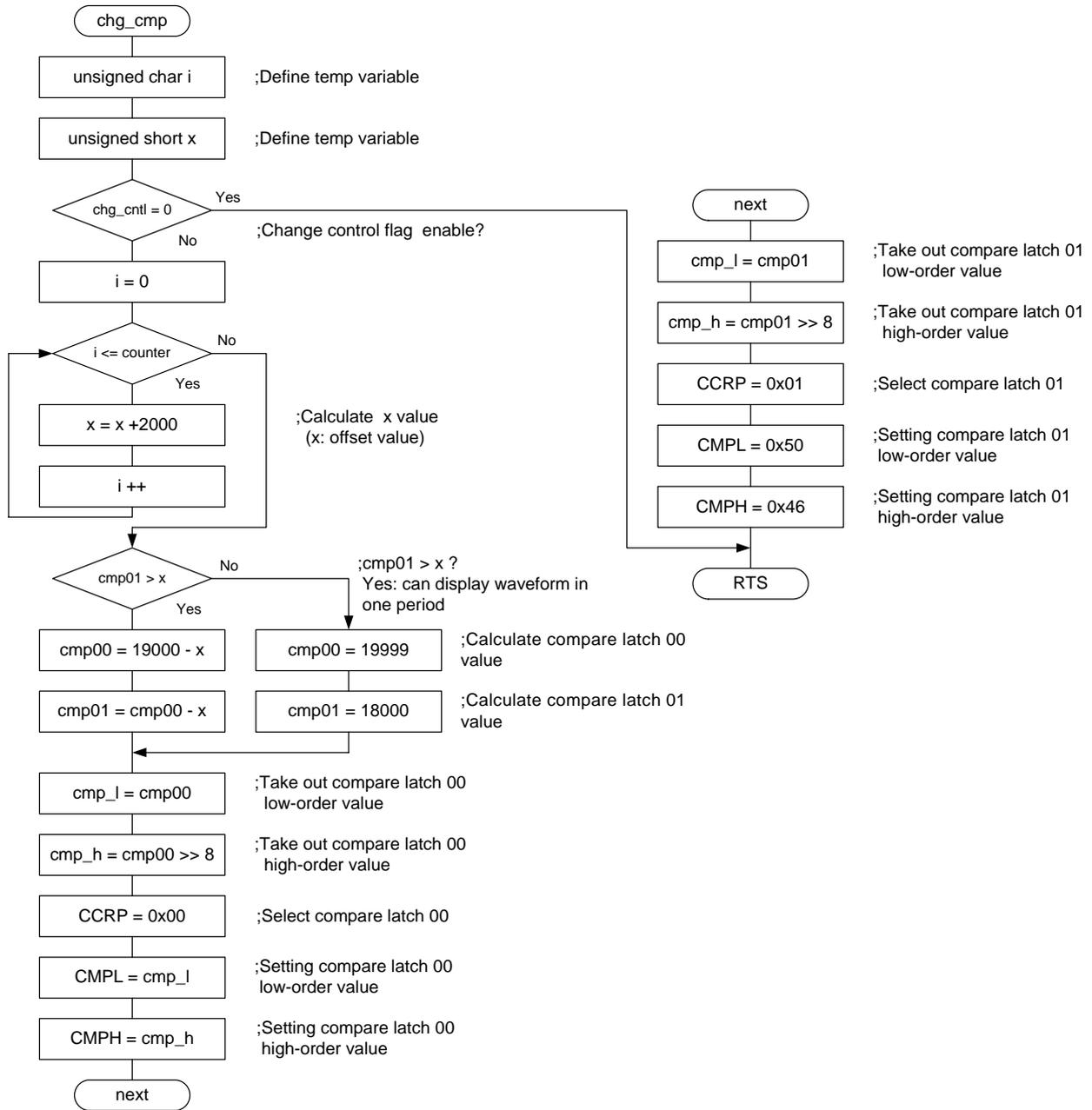
4.1 Flowing is the main loop program chart:



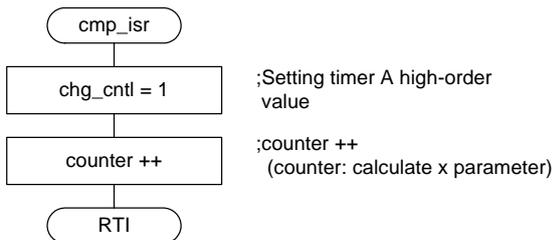
4.2 Flowing is the chart of initial setting subroutine (sfr_init):



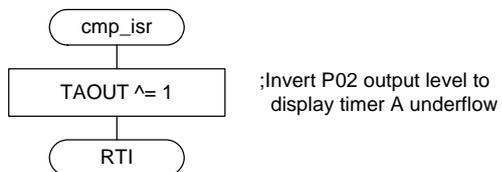
4.3 Flowing is the chart of change compare latch value subroutine (chg_cmp):



4.4 Flowing is the chart of compare interrupt service handle (cmp_isr):



4.5 Flowing is the chart of timer A service handle (ta_isr):



5. Sample program code

```

/*****
 *   File Name : rec05b0014_0100_source.c
 *   CPU       : M37546/47 Group
 *   Function  : Operation of timer A
 *              (Output compare normal mode)
 *   Version   : 1.00 (2006-03-13)
 *   Copyright (C) 2006, Renesas Technology Corp. All right reserved.
 *****/

/*****
 *   Include File
 *****/
#include <intr740.h>
#include "sfr_7546.h"

/*****
 *   Define Macro
 *****/
#define TAOUT    P0_2    /* P02 use as timer A output pin */
#define CMP00_L  0x1F    /* Define compare latch00 (L&H) value 19999 */
#define CMP00_H  0x4E
#define CMP01_L  0x50    /* Define compare latch01 (L&H) value 18000 */
#define CMP01_H  0x46

/*****
 *   Define Variable
 *****/
unsigned char chg_cntl  =0;    /* Change compare waveform enable flag */
unsigned char counter  =0;    /* Software counter */
unsigned short cmp00   =0;    /* Compare latch 00 value */
unsigned short cmp01   =0;    /* Compare latch 01 value */
unsigned char cmp_l    =0;    /* Compare latch low-order value */
unsigned char cmp_h    =0;    /* Compare latch high-order value */

/*****
 *   Function Declaration
 *****/
void sfr_init(void);    /* SFR initialization process */
void chg_cmp(void);    /* Change output waveform */

/*****
Name      : Main
 *****/

void main(void)
{

    disable_interrupt();    /* Interrupt disalbe */
    cld_instruction();    /* Binary arithmetic executed */

    CPUM = 0x84;    /* Single chip mode, stack page1, on-chip OSC */
    
```

```

ID_T1 = 0;          /* Clear timer 1 interrupt discrimination bit */
PRE1  = 0x31;      /* T = 25*50*16/2000000 = 10ms */
T1    = 0x18;
while (!ID_T1) {}  /* Waiting 10ms For Stable Of Oscillation */

CPUM = 0x04;       /* Switch To Main Clock, High-Speed Mode */
nop_instruction();
nop_instruction();
nop_instruction();

sfr_init();        /* SFR Initialize */

IREQ1 = 0x00;      /* All interrupt request bit is cleared */
IREQ2 = 0x00;
INTDIS = 0x00;

chg_cntl = 0;      /* Set change compare control flag disable */
cmp00 = 19999;     /* Compare latch 00 value */
cmp01 = 18000;     /* Compare latch 01 value */

enable_interrupt(); /* Interrupt Enable */

TASTP = 0;         /* timerA start */

while(1){
    chg_cmp();     /* Change compare output waveform */
}
}

/*****
Name      : chg_cmp
Function   : Write compare latch
*****/
void chg_cmp(void){

    unsigned char i;      /* Define temp variable */
    unsigned short x = 0; /* Define temp variable */

    if (!chg_cntl){return;} /* If chg_cntl disable, quit routine */
    chg_cntl = 0;         /* Clear change enable flag */

    for (i=0;i<=counter;i++){
        x = x + 2000;     /* Calculate offset */
    }

    if (cmp01 > x){
        cmp00 = 19999 - x; /* Compare latch 00 value */
        cmp01 = cmp00 - x; /* Compare latch 01 value */
    }
    else {
        cmp00 = 19999;     /* Compare latch 00 value */
        cmp01 = 18000;     /* Compare latch 01 value */
        counter = 0;       /* Clear software counter */
    }
}

```

```

}

/* Rewrite compare 00 register */
cmp_l = cmp00;      /* compare lath 00 low-order value */
cmp_h = cmp00 >> 8; /* compare lath 00 high-order value */
CCRP  = 0x00;      /* Selecte Latch 00 */
CMPL  = cmp_l;     /* Write low-order of compare 00 */
CMPH  = cmp_h;     /* Write high-order of compare 00 */

/* Rewrite compare 01 register */
cmp_l = cmp01;      /* compare lath 01 low-order value */
cmp_h = cmp01 >> 8; /* compare lath 01 high-order value */
CCRP  = 0x01;      /* Selecte Latch 01 */
CMPL  = cmp_l;     /* Write low-order of compare 01 */
CMPH  = cmp_h;     /* Write high-order of compare 01 */

CMPR  = 0x01;      /* Compare latch 00, 01 reload at next underflow */

}

/*****
Name      : cmp_isr
Function  : Compare interrupt service routine
*****/
interrupt void cmp_isr(void){

    chg_cntl = 1;      /* Set change waveform flag to enable */
    counter ++;      /* Software counter */
}

/*****
Name      : ta_isr
Function  : Timer A interrupt service routine
*****/
interrupt void ta_isr(void){

    TAOUT ^= 1;      /* Output timer A underflow waveform */
}

/*****
Name      : sfr_init
Function  : Initialize SFR
*****/
void sfr_init(void)
{
    POD.1 = 1;      /* P01/CMP0 output */
    POD.2 = 1;      /* P02 output, as timer A output */

    ICON1 = 0x00;   /* All interrupt is disable */
    ICON2 = 0x00;
    INTSET = 0x00;

    TABM  = 0x0A;   /* TimerA stop, write timer and latch simultaneous */
}

```

Operation of Timer A (Output Compare Mode)

```

TCSS  = 0x00;          /* timerA select fxin/16 */
TAL   = 0x1F;          /* TAH&L = 19999 */
TAH   = 0x4E;          /* f = 8000000/16/20000 = 25Hz */

TMSR  = 0x00;          /* Compare 0 source select timer A */
CMOM  = 0x10;          /* Compare 0 output positive, trigger enable */

CCRP  = 0x00;          /* Selecte Latch 00 */
Cmpl  = CMP00_L;       /* Write low-order of compare 00 */
CmpH  = CMP00_H;       /* Write high-order of compare 00 */

CCRP  = 0x01;          /* Selecte Latch 01 */
Cmpl  = CMP01_L;       /* Write low-order of compare 01 */
CmpH  = CMP01_H;       /* Write high-order of compare 01 */

CCPR  = 0x04;          /* P01 is compare 0 */
CISR  = 0x01;          /* Compare latch 00 interrupt source enable */

ICON2 = 0x14;          /* Enable timer A and compare interrupt */

}

```

In order to run properly for this program, the timer A interrupt vector and compare interrupt vector need to point to the service routines for the interrupt. The interrupt vector table information is included in the startup file "cstartup.s31".

```

EXTERN ta_isr, cmp_isr ; EXTERN directive
COMMON INTVEC          ; FFDC - FFFB, FFFC - FFFD
?CSTARTUP_INTVEC
WORD init_C             ; FFDC : BRK (use with E8 Emulator Program)
WORD init_C             ; FFDE : AD, Timer1
WORD init_C             ; FFE0 : TimerB
WORD ta_isr             ; FFE2 : TimerA
WORD init_C             ; FFE4 : TimerX
WORD cmp_isr           ; FFE6 : Compare
WORD init_C             ; FFE8 : Capture 1
WORD init_C             ; FFEA : Capture 0
WORD init_C             ; FFEC : CNTR0
WORD init_C             ; FFEE : Key-on wake-up, UART1 bus collision detection
WORD init_C             ; FFF0 : INT1
WORD init_C             ; FFF2 : INT0
WORD init_C             ; FFF4 : Serial I/O2 transmit
WORD init_C             ; FFF6 : Serial I/O2 receive (use with E8 Emulator
Program)
WORD init_C             ; FFF8 : Serial I/O1 transmit
WORD init_C             ; FFFA : Serial I/O1 receive
?CSTARTUP_RESETVEC
WORD init_C             ; FFFC : RESET (use with E8 Emulator Program)
ENDMOD init_C

```

6. Reference

Renesas web-site

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csc@renesas.com

Hardware manual

M37546 Group datasheet

M37547 Group datasheet

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Technical update/Technical news

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Revision

Rev.	Date	Description	
		Page	Summary
1.00	Mar.15.06	-	First edition issued

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