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April 1st, 2010
Renesas Electronics Corporation

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7546 Group

Operation of Bus Collision Detection

1. Abstract

The following article introduces and shows an example of how to use the bus collision detection function in the 7546 Group.

2. Introduction

The application example described in this document is applied to the following MCU and parameter(s):

- MCU : 7546 Group
- Oscillation frequency : 8 MHz

This sample program may include operations of unused bit functions for the SFR bit layout. Set these values according to the operating conditions of the user system.

3. Contents

3.1 Bus Collision Detection Function

This function allows the MCU to detect a bus collision during serial transmission on SIO1. When reception is started in clock synchronous or asynchronous (UART) serial I/O mode, the TxD1 transmit pin is compared with the RxD1 receive pin in synchronization with the rising edge of the receive shift clock. If they do not coincide with each other, a bus collision detection interrupt request is generated.

When a transmit data collision is detected between the LSB and MSB in clock synchronous serial I/O mode, or between the start bit and stop bit in UART mode, a bus collision detection can be performed by both the internal clock and the external clock.

Note: Bus collision detection can be used when SIO1 is operating at full-duplex communication. When SIO1 is operating at half-duplex communication, disable bus collision detection interrupt.

Figure 1 shows the Timing Chart of Bus Collision Detection Function.

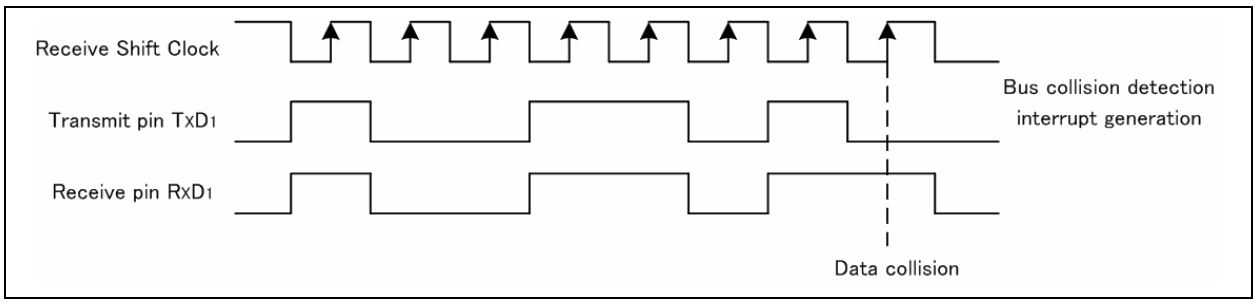


Figure 1 Timing Chart of Bus Collision Detection Function

3.2 Application Sample

In this application, the UART1 bus collision detection (U1BC) function is used to arbitrate multiple UART transmission requests in a system which consists of more than one MCU. The system configuration is described below.

- P11/TxD1 N-channel open-drain output mode is used;
- Both the RxD1 and TxD1 pins from different devices are all connected to a single bus line. A pull-up resistor (internal or external) is connected to that bus;
- Receive is always enabled, even during transmission.

Figure 2 shows the Connection Diagram.

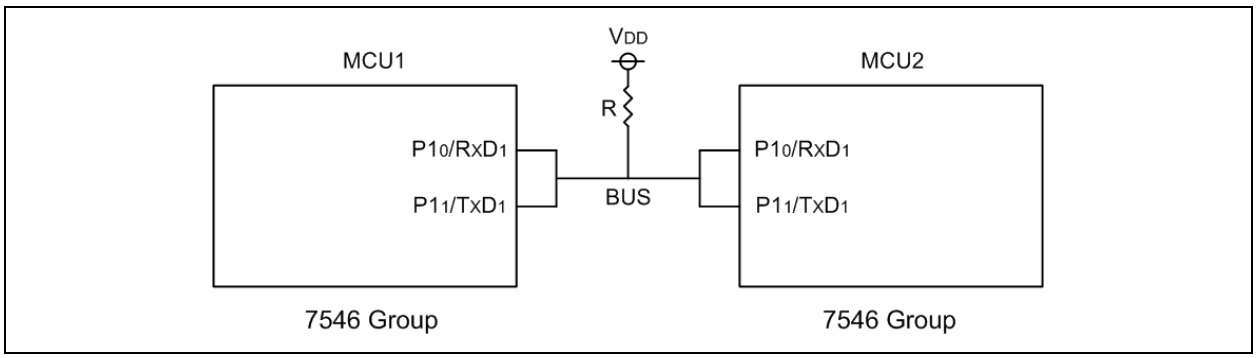
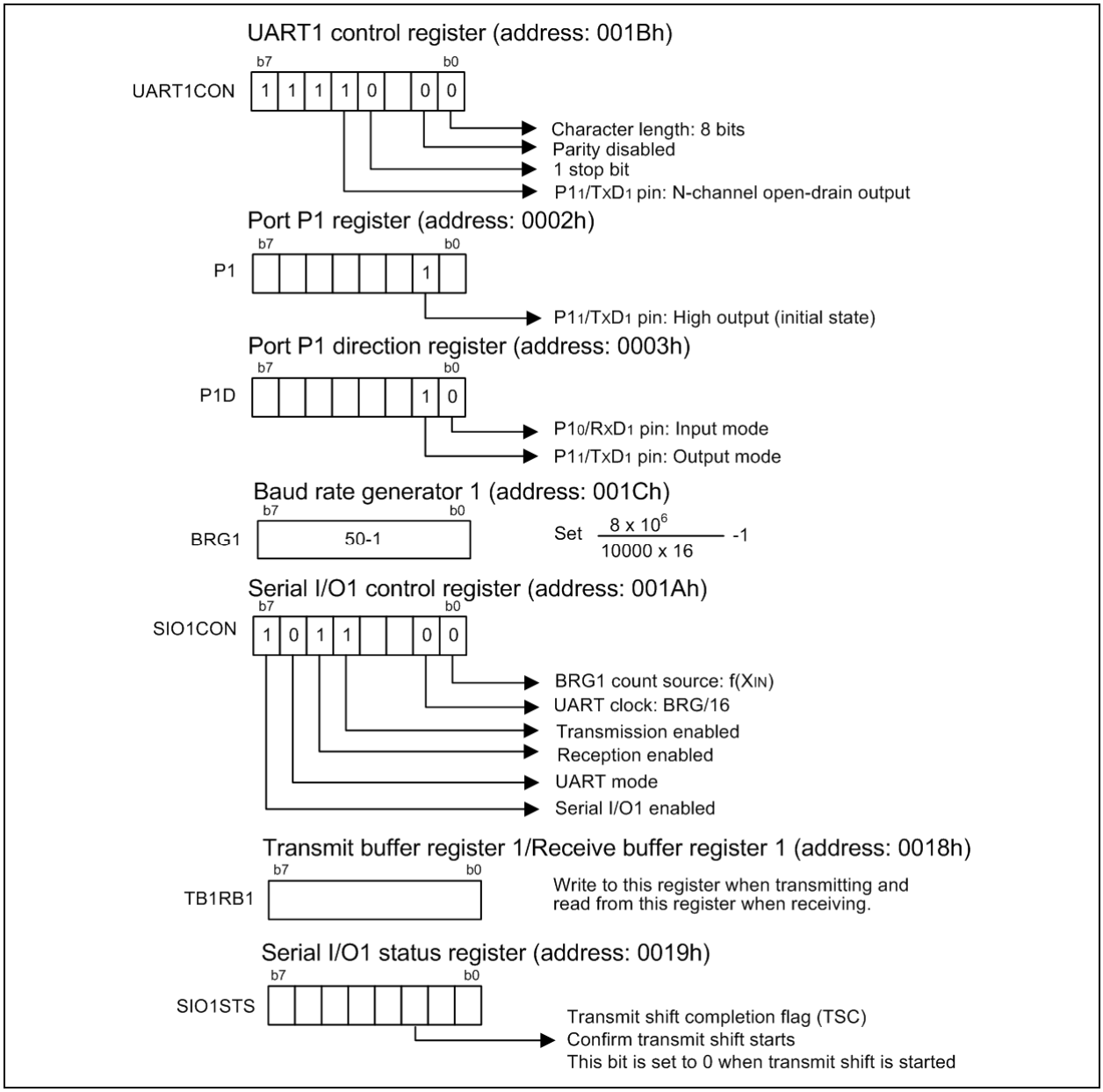


Figure 2 Connection Diagram

An N-channel open-drain bus with a pull-up resistor allows multiple TxD pins with different output levels to connect with each other directly. In this case, a low level has a higher priority than a high level. That means, if both levels are outputted to the bus, the high level will be overridden by the low level. Therefore, a device that outputs a high level through TxD will actually receive a low level on the RxD pin. The mismatch between TxD and RxD will trigger a U1BC interrupt which indicates a loss in arbitration.

This sample system includes two M37546 MCUs. A 10 Kbps baud rate is selected for both transmission and reception. Each device transmits independently after its system is initialized. Once one starts transmission, the other receives. If both devices initiate transmission at the same time (or within a very short time of one another), arbitration will take place on each bit from the START until a bit where the data outputted by two MCUs differ. According to the explanation above, the one sending the high level will loss the arbitration and immediately stop transmission.

Figure 3 shows the Relevant Register Settings, Figure 4 shows the Control Procedure of Main Function and Figure 5 shows the Control Procedure of Interrupt Handlers.



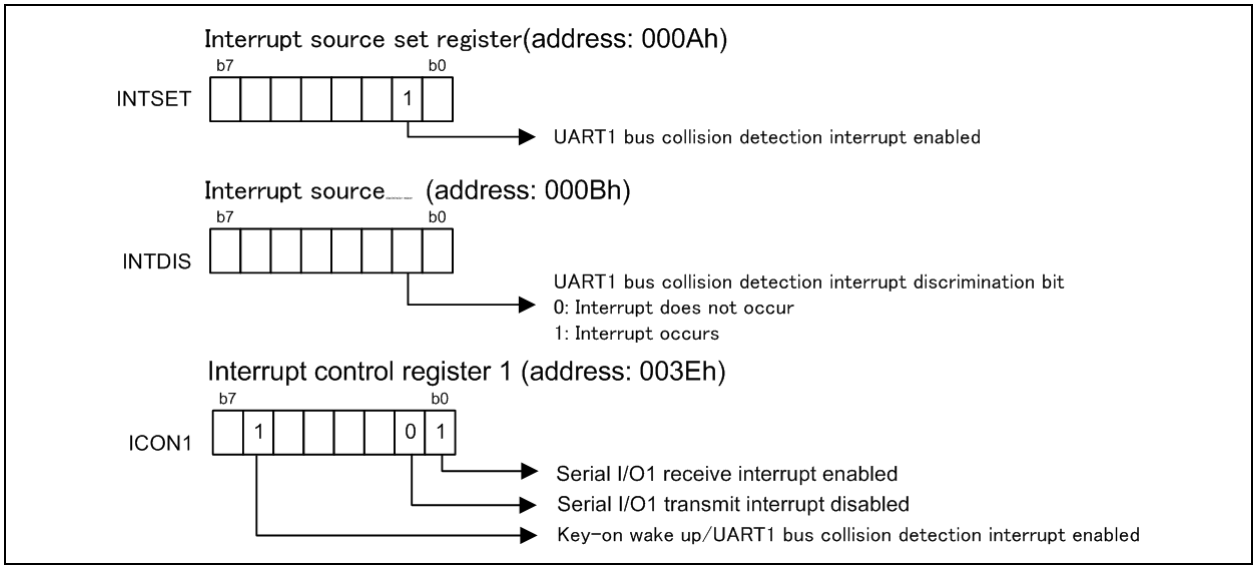


Figure 3 Relevant Register Settings

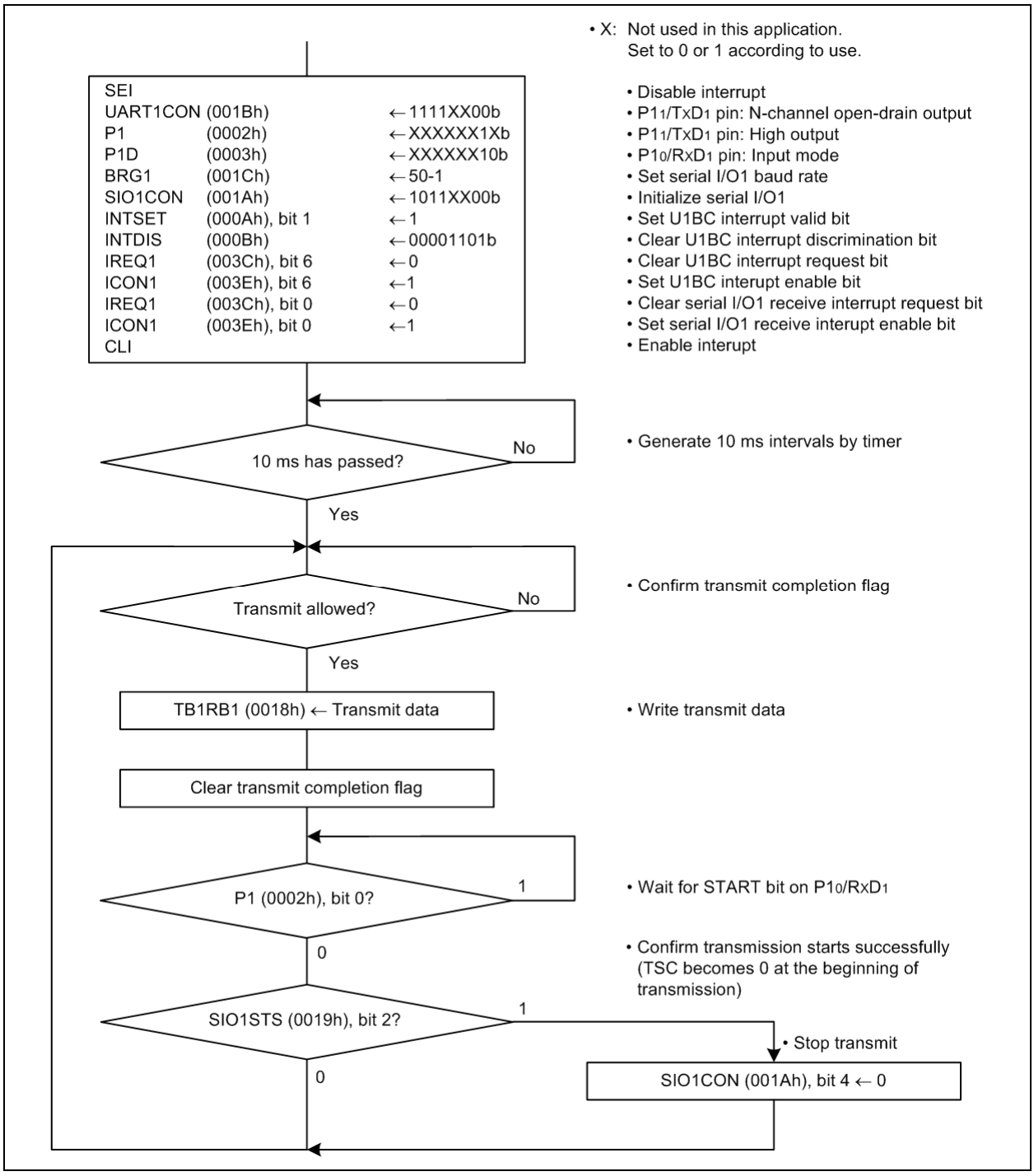


Figure 4 Control Procedure of Main Function

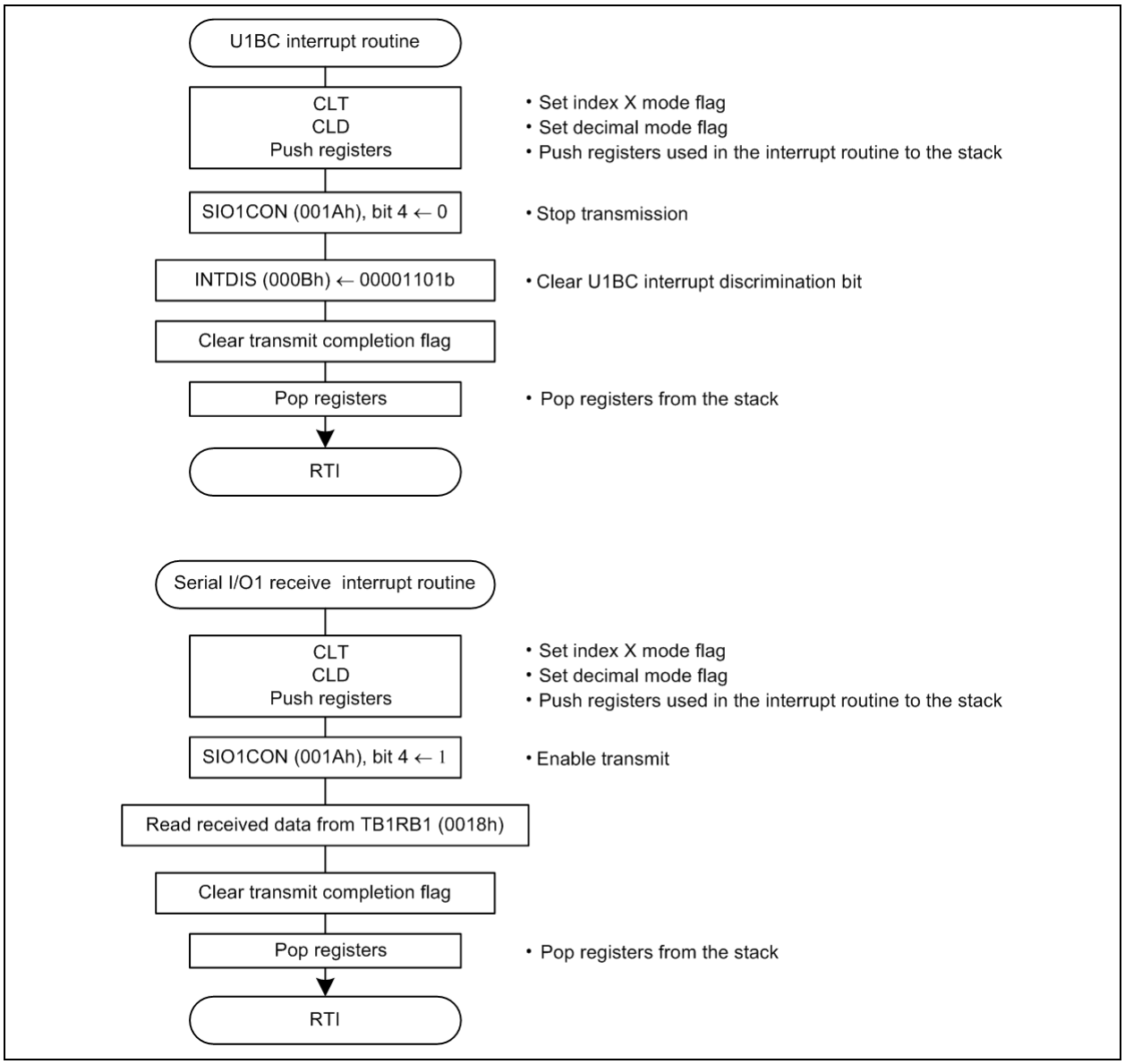


Figure 5 Control Procedure of Interrupt Handlers

4. Sample Programming Code

Please visit the Renesas Technology Web site for the reference program.
Click “Application Notes” in the left side menu on the page of the 7546 Group.

5. Reference Document

Datasheet
7546 Group Datasheet
(Use the latest version of the document on the Renesas Technology Web site.)

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		Page	Summary
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