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7545 Group

Oscillation Control

1. Abstract

The following article introduces and shows an example of oscillation control of the 7545 Group.

2. Introduction

The application example described in this document is applied to the following MCU:

- Applicable MCU: 7545 Group

3. Contents

The 7545 Group MCU can be set to stop the CPU. The CPU can be put on standby using the two power-saving modes listed below:

- Execute the STP instruction to enter stop mode
- Execute the WIT instruction to enter wait mode

3.1 Stop Mode

When the STP instruction is executed, the MCU enters stop mode. In stop mode, the main clock (XIN-XOUT) stops. The system clock ϕ stops "H". The CPU and peripheral functions then stop, and power consumption is reduced.

3.1.1 Status in Stop Mode

Table 3.1 lists the Status in Stop Mode.

Table 3.1 Status in Stop Mode

Item	Function	Pin
Oscillation	Stopped	XIN and XOUT: "H"
CPU	Stopped	-
System clock ϕ	Stopped "H"	-
I/O ports P0, P2, P3, P42	The I/O ports are held in their current state when the STP instruction is executed.	The I/O ports are held in the input state or output level when the STP instruction is executed.
Timers	Stopped (Timers 1, 2, 3)	-
Watchdog timer	Stopped	-
RAM	RAM1 Held(1), RAM2 Held(2)	-
CPU register and SFR	Held(3)	-
Voltage drop detection circuit	Stopped(4)	-

Notes: 1. When voltage supplied to VCC is more than the RAM1 hold voltage.
2. When voltage supplied to VDDR is more than the RAM2 hold voltage.
3. When voltage supplied to VCC is more than the RAM1 hold voltage. However, the CPU register and SFR are initialized when the MCU returns by the reset input.
4. When the STP instruction is executed, the voltage drop detection circuit is stopped, so that the power dissipation is reduced.

- Example to reduce power consumption
  - ✧ Input port: Fix an input port "H" or "L" externally.
  - ✧ Output port: Fix at the level to which the current does not flow externally.

For example, for a circuit that illuminates an LED when current flows during "L" signal output, an "H" level output is fixed.

3.1.2 Exiting Stop Mode

To exit stop mode, generate an enabled interrupt request or reset[(1)]. The MCU's return from stop mode differs between the interrupt request being generated and a reset being input.

- Return by interrupt
  If an enabled interrupt request is generated during stop mode[(2)], stop mode is exited and the main clock starts oscillating. As oscillation is unstable when it starts, a certain amount of time is necessary for oscillation to stabilize (oscillation stabilization time). When the MCU returns from stop mode from an interrupt, prescaler 1 and timer 1 generate the standby time for the system clock ϕ supply to the CPU[(3)]. The standby time is completed when timer 1 underflows and system clock ϕ supply to the CPU starts. The generated interrupt request is accepted and the interrupt routine is executed. The watchdog timer does not operate in stop mode, but operates during the standby time. Write to the watchdog timer control register (address 39_{16}) before the STP instruction is executed to prevent underflow during this time. Figure 3.1 shows an Operation Example When Returning from Stop Mode Using a Generated INT0 Interrupt Request.

Notes:

1. Regarding of reset, input "L" level to the RESET pin as the example of reset.
2. The following show the interrupt sources which can be used for returning from stop mode. Enable the interrupt to be used and execute the STP instruction.
   - ✧ INT0, INT1
   - ✧ Key input (key-on wake up)
3. When the oscillation stabilization time set bit after release of the STP instruction (bit 0 of MISRG (address 38_{16})) is set to "0", "FF_{16}" is automatically set to prescaler 1 and "03_{16}" is automatically set to timer 1. When the oscillation stabilization time set bit after release of the STP instruction is set to "1", set the following to prescaler 1 and timer 1 and execute the STP instruction.
   - ✧ Prescaler 1 register and timer 1 register: standby time
     Set the standby time in the following range:
     Oscillation stabilization time < standby time < time until the watchdog timer underflows
   - ✧ Timer 1 interrupt enable bit: "0" (interrupt disabled)
   - ✧ Timer 1 count stop bit: "0" (enable timer 1 count)

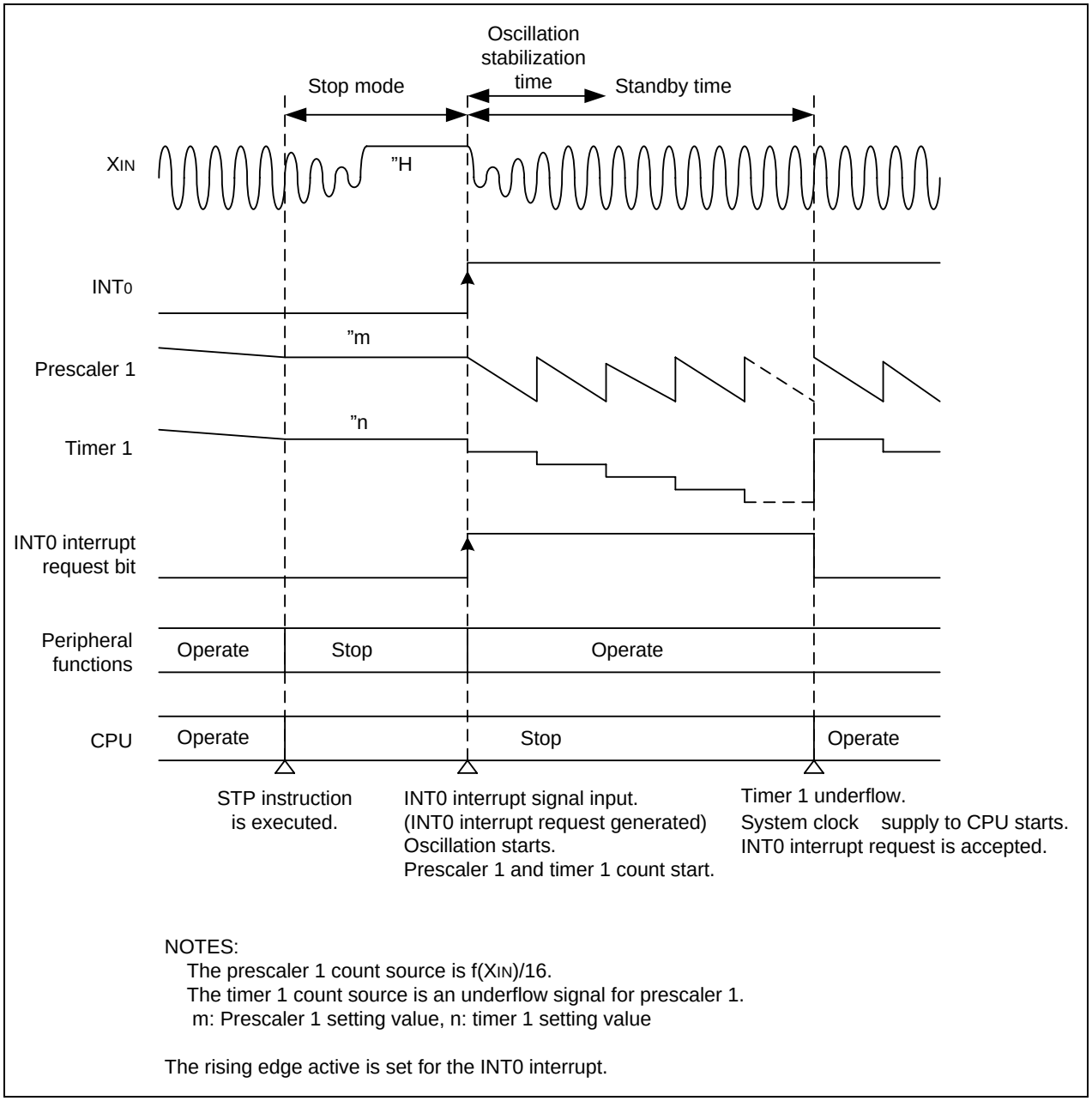

Figure 3.1 Operation Example When Returning from Stop Mode Using a Generated INT0 Interrupt Request

- Return by reset input

  To exit stop mode, the input level to the RESET pin must be “L” in stop mode. All I/O ports are changed to input mode, and main clock (XIN-XOUT) oscillation starts. Oscillation is unstable when it starts, and a certain amount of time is necessary for oscillation to stabilize (oscillation stabilization time). Hold the RESET pin input level “L” until oscillation is stable. An internal reset occurs when RESET pin input level is held “L” for 2µs or more and the MCU operates according to the reset sequence.

3.2 Wait Mode

The MCU enters wait mode when the WIT instruction is executed. In wait mode, oscillation continues but the system clock ϕ stops "H". The CPU stops, but the peripheral functions are active.

3.2.1 Status in Wait Mode

Table 3.2 lists the Status in Wait Mode.

Table 3.2 Status in Wait Mode

Item	Status in Wait Mode
Oscillation	Active
CPU	Stopped
System clock ϕ	Stopped "H"
I/O ports P0, P2, P3, P4$_2$	Hold the input state or output level when the WIT instruction is executed.
Timers	Active
Watchdog timer	Active
RAM	RAM1 Held, RAM2 Held
CPU register and SFR	Held(1)
Voltage drop detection circuit	Active(2)

Notes: 1. Some SFR may be changed depending on peripheral function operations. However, the CPU register and SFR are initialized when the MCU returns by the reset input.
2. The operation of the voltage drop detection circuit is enabled by setting "1" to bit 4 of the function set ROM data (address FFDA$_{16}$).

3.2.2 Exiting Wait Mode

To exit wait mode, generate an enabled interrupt request or reset[1]. The MCU's return from wait mode differs between the interrupt request being generated and a reset being input.

- Return by interrupt
  If an enabled interrupt request is generated during wait mode[2] , wait mode is exited and the system clock ϕ supply to the CPU starts. The generated interrupt request is accepted and its interrupt routine is executed. The watchdog timer is active in wait mode. Write to the watchdog timer control register to prevent underflow. Figure 3.2 shows an Operation Example When Returning from Wait Mode Using a Generated INT0 Interrupt Request.

Notes:
1. Regarding of reset, input "L" level to the RESET pin as the example of reset.
2. All interrupt sources can be used for returning from wait mode. Enable an interrupt and execute the WIT instruction.

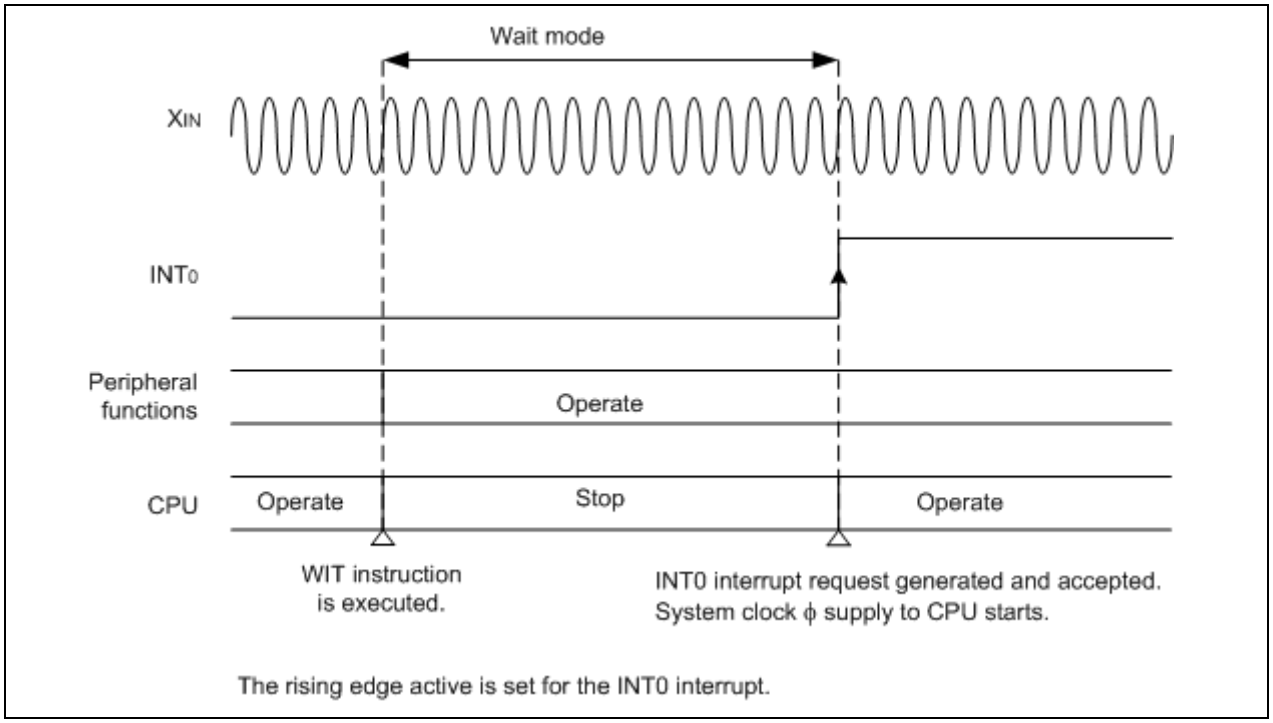

Figure 3.2 Operation Example When Returning from Wait Mode Using a Generated INT0 Interrupt Request

- Return by reset input
  To exit wait mode, the input level to the RESET pin must be "L" in wait mode. All I/O ports are changed to input mode, and main clock (XIN-XOUT) oscillation continues. An internal reset occurs when RESET pin input level is held "L" for 2µs or more and the MCU operates according to the reset sequence.

4. Reference Document

Datasheet
7545 Group Datasheet
(Use the most recent version of the document on the Renesas Technology Website.)

Technical News/Technical Update
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