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7542 Group

Oscillation Control

1. Abstract

This document describes oscillation control of the 7542 Group MCU.

2. Introduction

The application explained in this document applies to the following MCU:

- Applicable MCU: 7542 Group

3. Contents

The 7542 Group MCU can be set to stop the CPU. The CPU can be put on standby using the two power-saving modes listed below:

- Execute the STP instruction to enter stop mode
- Execute the WIT instruction to enter wait mode

3.1 Stop Mode

When the STP instruction is executed, the MCU enters stop mode. In stop mode, the main clock (XIN-XOUT) and on-chip oscillator oscillations stop. The system clock ϕ stops “H”. The CPU and peripheral functions then stop, and power consumption is reduced.

3.1.1 Status in Stop Mode

Table 3.1 lists the Status in Stop Mode.

Table 3.1 Status in Stop Mode

Item	Function	Pin
Oscillation	Stopped	XIN and XOUT: “H”
CPU	Stopped	–
System clock ϕ	Stopped “H”	–
I/O ports P0 to P3	The I/O ports are held in their current state when the STP instruction is executed.	The I/O ports are held in the input state or output level when the STP instruction is executed.
Timers	Stopped (timers 1, X, A and B) However, timer X is only active in event counter mode.	Timers are held in the input state or output level when the STP instruction is executed.
Watchdog timer	Stopped	–
Serial I/O1 and serial I/O2	Stopped However, serial I/O1 and serial I/O2 are only active when an external clock is selected.	Serial I/O1 and serial I/O2 are held in the input state or output level when the STP instruction is executed.
A/D converter	Stopped	The A/D converter is held in its current state when the STP instruction is executed.
RAM	Held ⁽¹⁾	–
CPU register and SFR	Held ⁽²⁾	–

NOTES:

1. When voltage supplied to Vcc is more than the RAM hold voltage.
2. When voltage supplied to Vcc is more than the RAM hold voltage. However, the CPU register and SFRs are initialized when the MCU returns by the reset input.

- Example to reduce power consumption
 - Input port: Fix an input port “H” or “L” externally
 - Output port: Fix at the level to which the current does not flow externally
 For example, for a circuit that illuminates an LED when current flows during “L” signal output, an “H” level output is fixed.
 - A/D input pin: Fix the A/D input pin to “H” or “L” externally
 - Complete an A/D conversion
 Confirm that the AD conversion completion bit (bit 4 in the AD control register (address 3416)) is set to “1”.

3.1.2 Exiting Stop Mode

To exit stop mode, generate an enabled interrupt request or input a reset. The MCU's return from stop mode differs between the interrupt request being generated and a reset being input.

- Return by interrupt

If an enabled interrupt request is generated during stop mode⁽¹⁾, stop mode is exited and the clock which is oscillating when the STP instruction is executed starts oscillating. As oscillation is unstable when it starts, a certain amount of time is necessary for oscillation to stabilize (oscillation stabilization time). When the MCU returns from stop mode from an interrupt, prescaler 1 and timer 1 generate the stand-by time for the system clock ϕ supply to the CPU⁽²⁾. Divide-by-16 of the operating clock source (XIN or ROSC) becomes the count source, and this standby time is allocated for the system clock's oscillation stabilization time⁽³⁾. The standby time is completed when timer 1 underflows and system clock ϕ supply to the CPU starts. The generated interrupt request is accepted and the interrupt routine is executed. The watchdog timer does not operate in stop mode, but operates during the standby time. Write to the watchdog timer control register (address 3916) before the STP instruction is executed to prevent underflow during this time⁽⁴⁾. Figure 3.1 shows an Operation Example When Returning from Stop Mode Using a Generated INT0 Interrupt Request.

NOTES:

1. The following show the interrupt sources which can be used for returning from stop mode. Enable the interrupt to be used and execute the STP instruction.
 - INT0 to INT4
 - CNTR0
 - CAP0 and CAP1
 - Serial I/O1 and serial I/O2 when an external clock is selected
 - Timer X in event counter mode
 - Key input (key-on wake up)
2. When the oscillation stabilization time set bit after release of the STP instruction (bit 0 of MISRG (address 3816)) is set to “0”, “FF16” is automatically set to prescaler 1 and “0116” is set to timer 1. When the oscillation stabilization time set bit after release of the STP instruction is set to “1”, set the following to prescaler 1 and timer 1 and execute the STP instruction.
 - Prescaler 1 register and timer 1 register: standby time
 Set the standby time in the following range:
 Oscillation stabilization time < standby time < time until the watchdog timer underflows
 - Timer 1 interrupt enable bit: “0” (interrupt disabled)

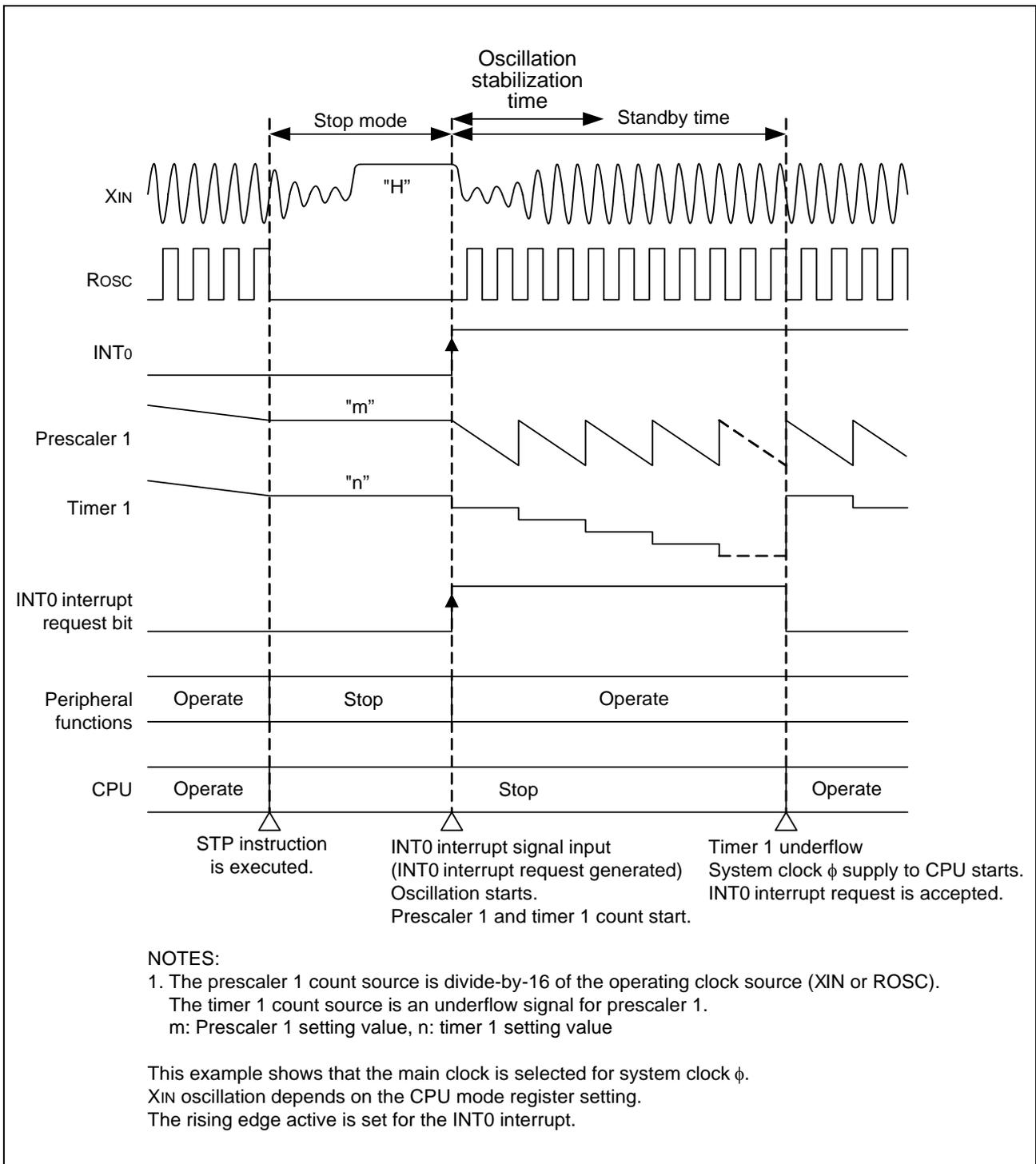


Figure 3.1 Operation Example When Returning from Stop Mode Using a Generated INT0 Interrupt Request

- Return by reset input
To exit stop mode, the input level to the $\overline{\text{RESET}}$ pin must be “L” in stop mode. All I/O ports are changed to input mode, and on-chip oscillator and main clock (XIN-XOUT) oscillations start. On-chip oscillator mode is selected for the system clock. An internal reset occurs when the $\overline{\text{RESET}}$ pin input level is held “L” for 2 μs or more and the MCU operates according to the reset sequence.

3.1.3 Notes on Stop Mode

- In the FLASH version, an internal power supply circuit is changed to low power consumption mode for consumption current reduction at the time of STP instruction execution. Although the internal power supply circuit is usually changed to the normal operation mode at the time of the return from an STP instruction, since a certain time is required to start the power supply to FLASH and operation of FLASH to be enabled, set wait time 100 μs or more with the FLASH version by the oscillation stabilization time set function after release of the STP instruction which uses the timer 1.

3.2 Wait Mode

The MCU enters wait mode when the WIT instruction is executed. In wait mode, oscillation continues but the system clock ϕ stops "H". The CPU stops, but the peripheral functions are active.

3.2.1 Status in Wait Mode

Table 3.2 lists the Status in Wait Mode.

Table 3.2 Status in Wait Mode

Item	State in Wait Mode
Oscillation	Active
CPU	Stopped
System clock ϕ	Stopped "H"
I/O ports P0 to P3	Hold the input state or output level when the WIT instruction is executed.
Timers	Active
Watchdog timer	Active
Serial I/O1 and serial I/O2	Active
A/D converter	Active
RAM	Held
CPU register and SFR	Held ⁽¹⁾

NOTES:

1. Some SFRs may be changed depending on peripheral function operations. The SFRs are initialized when the MCU returns by the reset input.

3.2.2 Exiting Wait Mode

To exit wait mode, generate an enabled interrupt request or input a reset. The MCU's return from wait mode differs between the interrupt request being generated and a reset being input.

- Return by interrupt

If an enabled interrupt request is generated during wait mode⁽¹⁾, wait mode is exited and the system clock ϕ supply to the CPU starts. The generated interrupt request is accepted and its interrupt routine is executed. The watchdog timer is active in wait mode. Write to the watchdog timer control register to prevent underflow.

Figure 3.2 shows an Operation When Returning from Wait Mode Using a Generated INT0 Interrupt Request.

NOTE:

All interrupt sources can be used for returning from wait mode. Enable an interrupt and execute the WIT instruction.

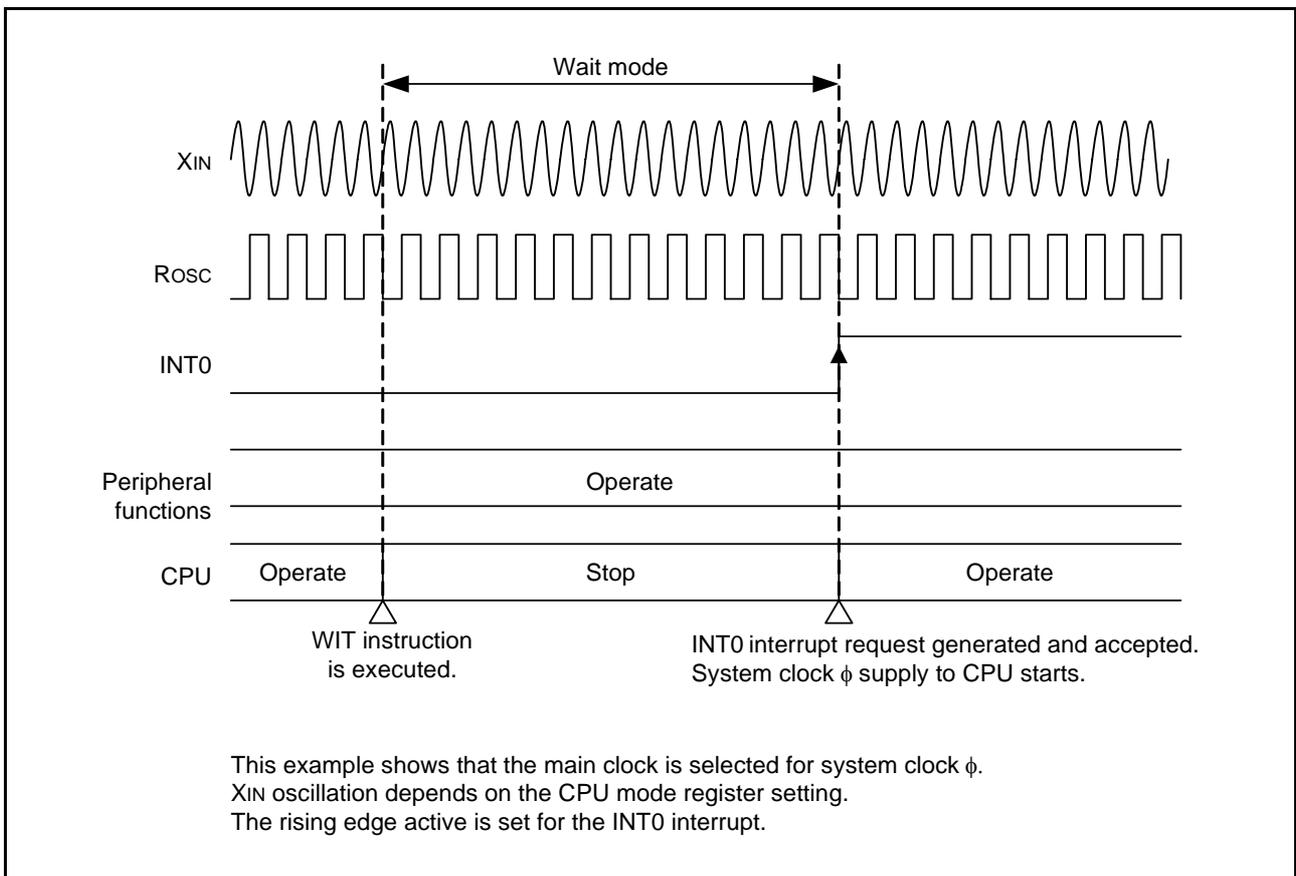


Figure 3.2 Operation When Returning from Wait Mode Using a Generated INT0 Interrupt Request

- Return by reset input

To exit wait mode, the input level to the $\overline{\text{RESET}}$ pin must be “L”. All I/O ports are changed to input mode, and the on-chip oscillator and main clock (XIN - XOUT) oscillations start. On-chip oscillator mode is selected for the system clock. If the main clock oscillates when the WIT instruction is executed, oscillation continues. An internal reset occurs when the $\overline{\text{RESET}}$ pin is held “L” for 2 μs or more and the MCU operates according to the reset sequence. If the main clock stops when the WIT instruction is executed, time for oscillation to stabilize when oscillation starts is necessary. Hold the $\overline{\text{RESET}}$ pin input level “L” or generate waiting time by the on-chip oscillator until oscillation is stable. And an internal reset occurs when the $\overline{\text{RESET}}$ pin input level is held “L” for 2 μs or more and the MCU operates according to the reset sequence.

4. Reference Document

Datasheet

7542 Group Datasheet

Use the most recent version of the document on the Renesas Technology Web site.

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