PCIe® Gen1 - Gen2 Interoperability Issues

Application Note AN-540

Introduction

This application note applies to the following IDT PCIe® 2.0 (Gen2) Switch Devices: IDT89PES24T6G2, IDT89PES24T3G2, IDT89PES16T4AG2, IDT89PES4T4G2, and IDT89HI0524G2PS. A few of the older Gen1 endpoint devices are unable to interoperate with Gen2 link partners including IDT Gen2 switches. This document explains the issue and a proposed solution.

IDT Silicon Revision ZA

IDT has discovered that a few of the Gen1 PCIe devices/adapters fail physical layer interoperability with revision ZA of IDT PCIe 2.0 (Gen2) switches PES24T6G2, PES24T3G2, PES16T4AG2, PES4T4G2, and HI0524G2PS. No workaround is currently available to overcome this interoperability issue in revision ZA silicon. It will be possible to work around this issue in revision ZB of the IDT switch silicon. The workaround is explained later in this document.

The root cause of this incompatibility is a flaw in the design of the endpoint devices and not the IDT switch. Newer revisions of these endpoints available from some vendors are known to have removed the design flaw. Users are encouraged to work with the endpoint vendors to obtain additional details regarding the design flaw and to update their hardware.

IDT has confirmed that the following endpoint devices do not interoperate successfully with the IDT Gen2 switches:

Card/HBA/ Adapter	Chip ID	Board Label	Vendor	Device	Sub	Rev	Fixed[1]
Agilent HHBA-6420C-S02	HPFC-6400C	PMCB00256 - 5288-5836 Rev 3	15BC	0103			
Agilent HHBA-6600	Tachyon QE4 HPFC-6600A	IOSD-0008V-30-0614-00023 (Rev 3)	15BC	1200	0000	04	
PMC HPFC-6700C-P	Tachyon DE4 HPFC-6700C-P	IOSD-0012V-30-0628-00011 (Rev 4)	15BC	1203	0000	06	
LSI 7104EP-LC		LSI7104EP-LC L3-00113-01D	1000	0646	5010	01	02
LSI 7204EP-LC	NA	LSI7204EP-LC L3-00120-01D	1000	0646	1020	01	02
LSI SAS3041E	LSI SAS1064E B1	03-01101-02B	1000	0056	3090	02	08
LSI SAS3801E	NA	L3-01123001B	1000	0058	30A0	02	08
HP Smart Array P400	LSI SAS1078 B0	NA	103C	3230	3234	01	
Xilinx ML 555	Xilinx Virtex-5 XC5VLX50T	ML555 0431438 REV03	10EE	5050			New bitstream available from Xilinx
Syskonnet SK-9E21D	Marvel 88E8052-NNC	60-10-088-001	1148	9E00	21D0	10	
Syskonnet SK-9E22	Marvel 88E8062-BDS	NA	1148	9E00	2200	12	

1. Silicon revision at which the vendor achieved PCIe 2.0 interoperability. An empty cell in this column implies that IDT has not been able to check for updates with the vendor. Users are encouraged to check on their own.

IDT Silicon Revision ZB

Revision ZB of the IDT Gen2 switch silicon enables the user to put in place a workaround for the interoperability problem seen with some of the older PCIe Gen1 endpoints. This workaround can be implemented in the system firmware (BIOS).

The basic logic behind the workaround, applied to each downstream port of the IDT switch, is as follows:

- Step 1: Check to see if the port has link-trained with the partner. If link-trained, no workaround is required, implying that link partner is a Gen2 device or a properly designed Gen1 device.
- Step 2: If not link-trained, determine if the port has no link partner at all, or if it is a problematic Gen1 link partner.
- Step 3: Force the switch downstream port to Gen1 link speed and check if the link can train.
- Step 4: If the link does not train, the implication is that the link has no link partner at all. If the link trains, the implication is that the link partner is one of the problematic endpoints and the workaround has resolved the issue.

Here is some pseudo code to implement this logic (it requires firmware to modify the PCIe configuration space of the IDT switch downstream ports):

```
loop till all ports are tested
    {
    if pcielsts.dllla == 1;          /* bit 13 at configuration space offset 0x052 for the port; implies Data Link Layer is active; link-trained */
        "done with this port";       /* good Gen1 or Gen2 link partner detected and operational */
    else                             /* either no link partner at all, or problematic Gen1 link partner */
        {
        pcielctl2.tls  = 1;          /* bits 3:0 at configuration space offset 0x070 for the port; forces Gen1 link speed */
        pcielctl.ldis  = 1;          /* bit 4 at configuration space offset 0x050 for the port; disables the link */
        delay (10 milliseconds);     /* allows the link to go down */
        pcielctl.ldis = 0;           /* bring up the link */
        delay (100 milliseconds);    /* allows the link to be back up */
        if pcielsts.dllla == 1;      /* bit 13 at configuration space offset 0x052 for the port; implies Data Link Layer is active; link-trained */
            "done with this port";   /* problematic Gen1 link partner detected and operational */
        else
            "no link partner"        /* unused port */
        }
    }
```

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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

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