Impedance Compensation in High Density LIU's Fully Internal Impedance Mode

82P2828/2821/2816/2521/2808 Application Note AN-524

1 INTRODUCTION/SUMMARY

The extra impedance introduced from outside of a silicon chip (bonding, packaging, PCB trace geometry, transformer DC resistance, etc) can alter the overall input/output impedance and therefore impact parameters such as return loss and pulse shape.

This note provides a way to compensate for the extra impedance by fine-tuning the 'reference resistor' (a resistor connected between REF pin and ground) when High Density LIU is configured in the fully internal impedance matching mode.

2 IMPACT OF UNWANTED IMPEDANCE

The IDT High Density LIU products (IDT82P2828/2821/2816/2521/2808) have three built-in options of termination schemes for users to select for receive and transmit impedance matching. They are:

- *Option 1: Fully Internal Impedance Matching with an integrated termination resistor.*
- *Option 2: Partially Internal Impedance Matching with a common external resistor.*
- *Option 3: External Impedance Matching with different external resistors.*

Once the chip is designed into the system, other factors, such as PCB trace geometry, backplane geometry, transformer DC resistance and connectors, will introduce some extra impedance between the High Density LIU analog interface and the cable. The introduced extra impedance will have an unpredictable impact on the port's return loss and transmitted pulse shape when the port is configured for E1/T1/J1 operations.

For the Partially Internal Impedance Matching and External Impedance Matching schemes (Options 2 & 3), the extra impedance introduced by board-level designs and components (described above) can be compensated by fine-tuning the external resistor being used.

3 IMPEDANCE COMPENSATION IN FULLY INTERNAL IMPEDANCE MODE

For Fully Internal Impedance Matching (Option 1), the termination resistor is an internal programmable resistor (IM) which is already trimmed to its nominal value at silicon level. Since there is no external termination resistor for users to tune, we turn to another externally connected resistor for impedance compensation. As recommended in the datasheet, a reference resistor (10 kΩ) is connected between the chip's REF pin and ground. This reference resistor is used to provide a standard reference current for the internal circuits. The overall impedance matching can be compensated to achieve optimal receive / transmit return loss and pulse shape by choosing the right value of this 'reference resistor'.

Changing the resistence value of this reference resistor will affect the High Density LIU's input impedance, output impedance and output pulse amplitude. The receive / transmit return loss can be optimized by fine-tuning the value of the reference resistor. Once the right value is determined, the scale factor – register of SCAL[5:0] can still take effect on the output pulse amplitude with the optimized impedance.

4 FINE-TUNING IMPEDANCE WITH DIFFERENT REFERENCE RESISTOR VALUES

Table 1 gives an example of the actual impedance values and their corresponding 'reference resistor' values when the High Density LIU is configured in the Fully Internal Impedance Matching mode.

Table 1: Reference Resistor Value vs. Output Impedance

Reference Resistor (kΩ)	Mode of Operation	Output Impedance from TTIP/TRING (Ω)	Comment
10	E1 75 coax	85	Measured when SCAL[5:0] = 0x21. (**Note**: The setting has no impact on impedance.)
	T1 100 twisted pair	107	
	E1 120 twisted pair	125	
9.1	E1 75 coax	78	Measured when SCAL[5:0] = 0x20. (**Note**: The setting has no impact on impedance.)
	T1 100 twisted pair	99	
	E1 120 twisted pair	115	
8.8	E1 75 coax	77	Measured when SCAL[5:0] = 0x2F. (**Note**: The setting has no impact on impedance.)
	T1 100 twisted pair	97	
	E1 120 twisted pair	113	

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