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Renesas Electronics Corporation

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1. Abstract

This document presents the method for using the timer of the 455A-group microcomputers and shows an application example.

2. Introduction

The application example explained in this document applies for use with the microcomputers and under the conditions described below.

• Microcomputer : 455A group
• Oscillation frequency : 4 MHz as f(XIN), however; 32.768 kHz as f(XCIN), however
• System clock : Used in through mode (not frequency divided)

In this application note, explanation is made of an example of timer setting method and an application example with respect to the following:

• CNTR output operation: Buzzer output
• CNTR input operation: Event count
• Timer operation: Timer start by external input
• Timer operation: Fixed-cycle counter
• Watchdog timer
3. Related Registers

3.1 Interrupt Control Register V1

Table 3.1 shows the bit configuration of Interrupt Control Register V1.

For write to the register V1, first set a value in the register A and then use the TV1A instruction.

Furthermore, the TAV1 instruction may be used to transfer the content of register V1 to the register A.

Table 3.1 Bit Configuration of Interrupt Control Register V1

<table>
<thead>
<tr>
<th>Interrupt Control Register V1</th>
<th>When reset: 0000</th>
<th>When powered down: 0000</th>
<th>R/W TAV1/TV1A</th>
</tr>
</thead>
<tbody>
<tr>
<td>V13 Timer 2 interrupt enable bit</td>
<td>0</td>
<td>Disables interrupt generation (SNZT2 instruction effective)</td>
<td></td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>Enables interrupt generation (SNZT2 instruction has no effect)</td>
<td></td>
</tr>
<tr>
<td>V12 Timer 1 interrupt enable bit</td>
<td>0</td>
<td>Disables interrupt generation (SNZT1 instruction effective)</td>
<td></td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>Enables interrupt generation (SNZT1 instruction has no effect)</td>
<td></td>
</tr>
<tr>
<td>V11 Unused</td>
<td>0</td>
<td>This bit has no functions assigned, but can be read/written.</td>
<td></td>
</tr>
<tr>
<td></td>
<td>1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>V10 External 0 interrupt enable bit</td>
<td>0</td>
<td>Disables interrupt generation (SNZ0 instruction effective)</td>
<td></td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>Enables interrupt generation (SNZ0 instruction has no effect)</td>
<td></td>
</tr>
</tbody>
</table>

Note 1: The letter R denotes “readable,” and the letter W denotes “writable.”

Note 2: : Unused bits during timer setting.

3.2 Interrupt Control Register V2

Table 3.2 shows the bit configuration of Interrupt Control Register V2.

For write to the register V2, first set a value in the register A and then use the TV2A instruction.

Furthermore, the TAV2 instruction may be used to transfer the content of register V2 to the register A.

Table 3.2 Bit Configuration of Interrupt Control Register V2

<table>
<thead>
<tr>
<th>Interrupt Control Register V2</th>
<th>When reset: 0000</th>
<th>When powered down: 0000</th>
<th>R/W TAV2/TV2A</th>
</tr>
</thead>
<tbody>
<tr>
<td>V23 Unused</td>
<td>0</td>
<td>This bit has no functions assigned, but can be read/written.</td>
<td></td>
</tr>
<tr>
<td></td>
<td>1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>V22 Unused</td>
<td>0</td>
<td>This bit has no functions assigned, but can be read/written.</td>
<td></td>
</tr>
<tr>
<td></td>
<td>1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>V21 Unused</td>
<td>0</td>
<td>This bit has no functions assigned, but can be read/written.</td>
<td></td>
</tr>
<tr>
<td></td>
<td>1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>V20 Timer 3 interrupt enable bit</td>
<td>0</td>
<td>Disables interrupt generation (SNZT3 instruction effective)</td>
<td></td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>Enables interrupt generation (SNZT3 instruction has no effect)</td>
<td></td>
</tr>
</tbody>
</table>

Note 1: The letter R denotes “readable,” and the letter W denotes “writable.”

Note 2: : Unused bits during timer setting.
3.3 Interrupt Control Register I1

Table 3.3 shows the bit configuration of Interrupt Control Register I1.

For write to the register I1, first set a value in the register A and then use the TI1A instruction.

Furthermore, the TAI1 instruction may be used to transfer the content of register I1 to the register A.

Table 3.3 Bit Configuration of Interrupt Control Register I1

<table>
<thead>
<tr>
<th>Interrupt Control Register I1</th>
<th>When reset: 0000z</th>
<th>When powered down: State retained</th>
<th>R/W TAI1/TI1A</th>
</tr>
</thead>
<tbody>
<tr>
<td>I13 INT pin input control bit</td>
<td>0 Disables input</td>
<td>1 Enables input</td>
<td></td>
</tr>
<tr>
<td>I12 INT pin interrupt active waveform/return level select bit</td>
<td>0 Falling waveform/low level (SNZI0 instruction recognizes low level)</td>
<td>1 Rising waveform/high level (SNZI0 instruction recognizes high level)</td>
<td></td>
</tr>
<tr>
<td>I11 INT pin edge detection circuit control bit</td>
<td>0 Detects one edge</td>
<td>1 Detects both edges</td>
<td></td>
</tr>
<tr>
<td>I10 INT pin timer 1 count start synchronizing circuit select bit</td>
<td>0 Deselects timer 1 count start synchronizing circuit</td>
<td>1 Selects timer 1 count start synchronizing circuit</td>
<td></td>
</tr>
</tbody>
</table>

Note 1: The letter R denotes “readable,” and the letter W denotes “writable.”
Note 2: When the contents of these bits (I12 or I13) are changed, the external interrupt request flag (EXF0) may be set.

3.4 Timer Control Register PA

Table 3.4 shows the bit configuration of Timer Control Register PA.

For write to the register PA, first set a value in the register A and then use the TPAA instruction.

Table 3.4 Bit Configuration of Timer Control Register PA

<table>
<thead>
<tr>
<th>Timer Control Register PA</th>
<th>When reset: 0z</th>
<th>When powered down: 0z</th>
<th>W TPAA</th>
</tr>
</thead>
<tbody>
<tr>
<td>PA0 Prescaler control bit</td>
<td>0 Stop (state retained)</td>
<td>1 Start</td>
<td></td>
</tr>
</tbody>
</table>

Note 1: The letter W denotes “writable.”
3.5 Timer Control Register W1

Table 3.5 shows the bit configuration of Timer Control Register W1.

For write to the register W1, first set a value in the register A and then use the TW1A instruction.

Furthermore, the TAW1 instruction may be used to transfer the content of register W1 to the register A.

Table 3.5 Bit Configuration of Timer Control Register W1

<table>
<thead>
<tr>
<th>Timer Control Register W1</th>
<th>When reset: 0000</th>
<th>When powered down: State retained</th>
<th>R/W TAW1/TW1A</th>
</tr>
</thead>
<tbody>
<tr>
<td>W13 Timer 1 count auto stop circuit select bit</td>
<td>0</td>
<td>Deselects timer 1 count auto stop circuit</td>
<td></td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>Selects timer 1 count auto stop circuit</td>
<td></td>
</tr>
<tr>
<td>W12 Timer 1 control bit</td>
<td>0</td>
<td>Stop (state returned)</td>
<td></td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>Start</td>
<td></td>
</tr>
<tr>
<td>W11 Timer 1 count source select bit Note 2</td>
<td>W11 W10</td>
<td>Count source</td>
<td></td>
</tr>
<tr>
<td></td>
<td>0 0</td>
<td>PWM signal (PWMOUT)</td>
<td></td>
</tr>
<tr>
<td></td>
<td>0 1</td>
<td>Prescaler output (ORCLK)</td>
<td></td>
</tr>
<tr>
<td>W10</td>
<td>1 0</td>
<td>Timer 3 underflow signal (T3UDF)</td>
<td></td>
</tr>
<tr>
<td></td>
<td>1 1</td>
<td>CNTR input</td>
<td></td>
</tr>
</tbody>
</table>

Note 1: The letter R denotes “readable,” and the letter W denotes “writable.”

Note 2: This function is usable only when timer 1 count start synchronizing circuit is selected (I10 = 1).

Note 3: If CNTR input is selected for the timer 1 count source, port C output is disabled.

3.6 Timer Control Register W2

Table 3.6 shows the bit configuration of Timer Control Register W2.

For write to the register W2, first set a value in the register A and then use the TW2A instruction.

Furthermore, the TAW2 instruction may be used to transfer the content of register W2 to the register A.

Table 3.6 Bit Configuration of Timer Control Register W2

<table>
<thead>
<tr>
<th>Timer Control Register W2</th>
<th>When reset: 0000</th>
<th>When powered down: 0000</th>
<th>R/W TAW2/TW2A</th>
</tr>
</thead>
<tbody>
<tr>
<td>W23 CNTR pin output control bit</td>
<td>0</td>
<td>Disables CNTR pin output</td>
<td></td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>Enables CNTR pin output</td>
<td></td>
</tr>
<tr>
<td>W22 PWM signal high period extend function control bit</td>
<td>0</td>
<td>Disables PWM signal high period extend function</td>
<td></td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>Enables PWM signal high period extend function</td>
<td></td>
</tr>
<tr>
<td>W21 Timer 2 control bit</td>
<td>0</td>
<td>Stop (state retained)</td>
<td></td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>Start</td>
<td></td>
</tr>
<tr>
<td>W20 Timer 2 count source select bit</td>
<td>0</td>
<td>X1 input</td>
<td></td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>Prescaler output (ORCLK) divided by 2</td>
<td></td>
</tr>
</tbody>
</table>

Note 1: The letter R denotes “readable,” and the letter W denotes “writable.”
3.7 Timer Control Register W3

Table 3.7 shows the bit configuration of Timer Control Register W3.
For write to the register W3, first set a value in the register A and then use the TW3A instruction.
Furthermore, the TAW3 instruction may be used to transfer the content of register W3 to the register A.

Table 3.7 Bit Configuration of Timer Control Register W3

<table>
<thead>
<tr>
<th>Timer Control Register W3</th>
<th>When reset: 0000z</th>
<th>When powered down: State retained</th>
<th>R/W TAW3/TW3A</th>
</tr>
</thead>
<tbody>
<tr>
<td>W33 Timer 3 control bit</td>
<td>0 Stop (initial state)</td>
<td>1 Start</td>
<td></td>
</tr>
<tr>
<td>W32</td>
<td>W3z W3y W3o</td>
<td>Count value</td>
<td></td>
</tr>
<tr>
<td>0 0 0 Generates underflow every 512 counts</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0 1 0 Generates underflow every 2,048 counts</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1 0 0 Generates underflow every 8,192 counts</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1 0 1 Generates underflow every 16,384 counts</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1 1 0 Generates underflow every 32,768 counts</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1 1 1 Generates underflow every 65,536 counts</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Note 1: The letter R denotes “readable,” and the letter W denotes “writable.”

3.8 Timer Control Register W4

Table 3.8 shows the bit configuration of Timer Control Register W4.
For write to the register W4, first set a value in the register A and then use the TW4A instruction.
Furthermore, the TAW4 instruction may be used to transfer the content of register W4 to the register A.

Table 3.8 Bit Configuration of Timer Control Register W4

<table>
<thead>
<tr>
<th>Timer Control Register W4</th>
<th>When reset: 0000z</th>
<th>When powered down: State retained</th>
<th>R/W TAW4/TW4A</th>
</tr>
</thead>
<tbody>
<tr>
<td>W43 Timer LC control bit</td>
<td>0 Stop (state retained)</td>
<td>1 Start</td>
<td></td>
</tr>
<tr>
<td>W42 Timer LC count source select bit</td>
<td>0 Bit 4 of timer 3 (T34)</td>
<td>1 System clock (STCK)</td>
<td></td>
</tr>
<tr>
<td>W41 CNTR pin output auto control circuit select bit</td>
<td>0 Deselects CNTR pin output auto control circuit</td>
<td>1 Selects CNTR pin output auto control circuit</td>
<td></td>
</tr>
<tr>
<td>W40 CNTR pin input count edge select bit</td>
<td>0 Falling edge</td>
<td>1 Rising edge</td>
<td></td>
</tr>
</tbody>
</table>

Note 1: The letter R denotes “readable,” and the letter W denotes “writable.”
Note 2: Unused bits during timer setting.
3.9 Timer Control Register W5
Table 3.9 shows the bit configuration of Timer Control Register W5.
For write to the register W5, first set a value in the register A and then use the TW5A instruction.
Furthermore, the TAW5 instruction may be used to transfer the content of register W5 to the register A.

Table 3.9 Bit Configuration of Timer Control Register W5

<table>
<thead>
<tr>
<th>Timer Control Register W5</th>
<th>When reset: 0000</th>
<th>When powered down: State retained</th>
<th>R/W TAW5/TW5A</th>
</tr>
</thead>
<tbody>
<tr>
<td>W53 Unused</td>
<td>0</td>
<td>This bit has no functions, but can be accessed for read/write.</td>
<td></td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>This bit has no functions, but can be accessed for read/write.</td>
<td></td>
</tr>
<tr>
<td>W52 Unused</td>
<td>0</td>
<td>This bit has no functions, but can be accessed for read/write.</td>
<td></td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>This bit has no functions, but can be accessed for read/write.</td>
<td></td>
</tr>
<tr>
<td>W51 Timer 3 count source select bit</td>
<td>0 0</td>
<td>Xcin input</td>
<td></td>
</tr>
<tr>
<td></td>
<td>0 1</td>
<td>ORCLK input</td>
<td></td>
</tr>
<tr>
<td>W50 Timer 3 count source select bit</td>
<td>1 0</td>
<td>Low-speed on-chip oscillator input (LSOCO)</td>
<td></td>
</tr>
<tr>
<td></td>
<td>1 1</td>
<td>High-speed on-chip oscillator input (HSOCO)</td>
<td></td>
</tr>
</tbody>
</table>

Note 1: The letter R denotes “readable,” and the letter W denotes “writable.”
Note 2: Unused bits during timer setting.

3.10 Port Output Mode Control Register FR2
Table 3.10 shows the bit configuration of Port Output Mode Control Register FR2.
For write to the register FR2, first set a value in the register A and then use the TFR2A instruction.

Table 3.10 Bit Configuration of Port Output Mode Control Register FR2

<table>
<thead>
<tr>
<th>Port Output Mode Control Register FR2</th>
<th>When reset: 0000</th>
<th>When powered down: State retained</th>
<th>W TFR2A</th>
</tr>
</thead>
<tbody>
<tr>
<td>FR2i Port P3x and P3y output mode select bit</td>
<td>0</td>
<td>N-channel open-drain output</td>
<td></td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>CMOS output</td>
<td></td>
</tr>
<tr>
<td>FR2i Port P3x and P3y output mode select bit</td>
<td>0</td>
<td>N-channel open-drain output</td>
<td></td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>CMOS output</td>
<td></td>
</tr>
<tr>
<td>FR2i Port D5 output mode select bit</td>
<td>0</td>
<td>N-channel open-drain output</td>
<td></td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>CMOS output</td>
<td></td>
</tr>
<tr>
<td>FR2i Port D4 output mode select bit</td>
<td>0</td>
<td>N-channel open-drain output</td>
<td></td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>CMOS output</td>
<td></td>
</tr>
</tbody>
</table>

Note 1: The letter W denotes “writable.”
Note 2: Unused bits during timer setting.
4. Timer Application Example

4.1 CNTR Output Operation: Buzzer Output

Point: The square wave output from timer 2 can be used for buzzer output as its application.

Specification: When system clock frequency = 4 MHz, a square wave in frequency of approximately 4 kHz is output from the CNTR pin. Also, a timer 2 interrupt is generated at the same time.

Figure 4.1 shows an example of a peripheral circuit. Figure 4.3 shows an example of how to set the registers for CNTR output.

Figure 4.1 Example of a Peripheral Circuit

4.2 CNTR Input Operation: Event Count

Point: A signal (rising waveform) input from the CNTR pin can be used as an event for count operation.

Specification: Low-frequency pulses are input as the count source for timer 1 from the outside to the CNTR pin, and a timer 1 interrupt is generated every 100 counts.

Figure 4.4 shows an example of how to set the registers for CNTR input.

4.3 Timer Operation: Timer Start by External Input

Point: A fixed length of time can be measured using external input.

Specification: Timer 1 is triggered to start counting by INT input and an interrupt is generated 1 ms later.

Figure 4.5 shows an example of how to set the registers for timer 1 to be started by external 0 input.

4.4 Timer Operation: Fixed-cycle Counter by Timer 3

Point: Exact time can be measured using a 32.768 kHz crystal resonator, making it possible to create a highly accurate time-of-day clock.

Specification: A timer 3 interrupt is generated every 250 ms synchronously with the timing signal derived by dividing the sub-clock frequency (f(XCIN) = 32.768 kHz) with timer 3.

Figure 4.6 shows an example of how to set the registers for a fixed-cycle counter by timer 3.
4.5 Watchdog Timer

The watchdog timer function offers a means for restoring the chip into a reset state when, for example, a program has gone wild and could not be executed normally.

When the watchdog timer function is enabled, always be sure that the WRST instruction is executed at intervals equal to or less than 65,534 counts of a 16-bit timer (i.e., at intervals equal to or less than 65,534 machine cycles).

Point: While operating normally, the WRST instruction is always executed within 65,534 counts of a 16-bit timer. If the program goes wild, the WRST instruction will no longer be executed, causing the chip to be reset.

Specification: Using a system clock frequency of 4.0 MHz, this function detects program runaway by executing the WRST instruction within 49 ms.

Figure 4.2 schematically shows the watchdog timer function. Figure 4.7 shows an example for using the watchdog timer.

![Figure 4.2 Watchdog Timer Function](image)

(1) After reset (after program start), the timer WDT starts counting down.
(2) When the timer WDT underflows upon reaching the minimum count, the flag WDF1 is set to 1.
(3) When the WRST instruction is executed, the flag WDF1 is cleared to 0 and the next instruction is skipped.
(4) If the timer WDT underflows while the flag WDF1 = 1, the flag WDF2 is set to 1 and a watchdog reset signal is output.
(5) The watchdog reset signal causes the output transistor of the RESET# pin to turn on, thereby generating a system reset.

Note: Since the count source for the timer WDT is the instruction clock, the number of counts is the same as the number of machine cycles.
Figure 4.3 Example of CNTR Output Setting

X: Don’t care

To output a square wave whose state is reversed every 126 µs, set the prescaler count value and timer 2 count value as shown below.

126 µs = \(\frac{4.0\text{MHz}}{1}\times\frac{3}{3+1}\times\frac{20}{20+1}\)

* Precautions to be taken when interrupt requests are cleared

If step (4) is executed, be sure to insert a NOP instruction after the SNZT2 instruction because the next instruction may be skipped depending on the state of the interrupt request flag T2F.

(1) Disabling interrupts
Temporarily disable timer 2 interrupt. Interrupt enable flag INTE = 0
Interrupt Control Register V1

(2) Stopping timer and prescaler operations
Temporarily stop timer 2 and prescaler.
Timer Control Register W2
Timer Control Register PA

(3) Setting timer values
Set the count time of timer 2 and prescaler. (Calculation formula is shown in *A below).
Prescaler Reload Register RPS = 0316
Timer 2 Reload Register R2L = 1416
Timer 2 Reload Register R2H = 1416

(4) Clearing interrupt request
Clear the timer 2 interrupt request flag.

Timer 2 interrupt request flag T2F = 0
Timer 2 interrupt request flag cleared (SNZT2 instruction)

(5) Starting timer and prescaler operations
Restart the temporarily stopped timer 2 and prescaler operations. Select the timer 2 count source.
Timer Control Register W2
Timer Control Register PA

(6) Enabling interrupt
Reenable the temporarily disabled timer 2 interrupt.
Interrupt Control Register V1
Interrupt enable flag INTE = 1

(7) Stopping CNTR output
Disable CNTR pin output to place it into the high-impedance state.
Timer Control Register W1
Timer Control Register W2
Figure 4.4 Example of CNTR Input Setting

1. Disabling interrupts
   Temporarily disable timer 1 interrupt.
   - Interrupt enable flag INTE = 0
   - All interrupts disabled (DI instruction)
   - Generation of timer 1 interrupt disabled (TV1A instruction)

2. Stopping timer operation
   Temporarily stop timer 1.
   - Timer 1 stopped (TW1A instruction)

3. Setting input count edge
   Select a rising transition for the count edge.
   - Rising transition selected for the count edge (TW4A instruction)
   - CNTR pin output auto control circuit deselected

4. Setting a timer value
   Set the number of counts for timer 1.
   - Timer 1 count value set to 100–1 (T1AB instruction)

5. Clearing interrupt request
   Clear the timer 1 interrupt request flag.
   - Timer 1 interrupt request flag cleared (SNZT1 instruction)
   - Precautions to be taken when interrupt requests are cleared
     If step (5) is executed, be sure to insert a NOP instruction after the SNZT1 instruction because the next instruction may be skipped depending on the state of the interrupt request flag T1F.

6. Starting timer operation
   Restart the temporarily stopped timer 1 operation.
   - Timer 1 operation started (TW1A instruction)
   - CNTR input selected for the timer 1 count source

7. Enabling interrupt
   Reenable the temporarily disabled timer 1 interrupt.
   - Generation of timer 1 interrupt enabled (TV1A instruction)
   - All interrupts enabled (EI instruction)

X: Don’t care
Figure 4.5 Example of Settings for Timer 1 Started by External 0 Input

(1) Disabling interrupts
Temporarily disable timer 1 and external 0 interrupts.

- Generation of timer 1 interrupt disabled (TV1A instruction)
- Generation of external 0 interrupt disabled

(2) Deselecting the timer 1 count start synchronizing circuit

(3) Stopping timer 1 and prescaler operations
Temporarily stop timer 1 and prescaler.

(4) Setting the port
Set the INT pin for input.

(5) Setting timer values
Set the count time of prescaler and timer 1. (Calculation formula is shown in *A below)

- Prescaler count value set to 15 (TPSAB instruction)
- Timer count value set to 82 (T1AB instruction)

(6) Clearing interrupt request
Clear the timer 1 interrupt request flag.

- Timer 1 interrupt request flag cleared (SNZT1 instruction)

(7) Setting the INT pin for input
Enable input to the INT pin.

- Timer 1 count start synchronizing circuit deselected (TI1A instruction)

(8) Starting timer and prescaler operations
Restart the temporarily stopped timer 1 and prescaler operations.

- Timer 1 operation started (TW1A instruction)

(10) Enabling interrupt
Reenable the temporarily disabled timer 1 interrupt.

- Generation of timer 1 interrupt enabled (TV1A instruction)

* Precautions to be taken when interrupt requests are cleared
If step (6) is executed, be sure to insert a NOP instruction after the SNZT1 instruction because the next instruction may be skipped depending on the state of the interrupt request flag T1F. (The same applies for the external 0 interrupt request flag in (7).)
Figure 4.6 Example of Settings for Fixed-cycle Counter by Timer 3

1. Disabling interrupts
   - Temporarily disable the timer 3 interrupt.
   - Interrupt enable flag INTE = 0
   - All interrupts disabled (DI instruction)

2. Stopping timer operation
   - Temporarily stop timer 3.
   - Timer 3 interrupt request flag T3F = 0
   - Timer 3 interrupt start condition cleared (SNZT3 instruction)

3. Setting count source and count value
   - Set the count source and count value of timer 3.
   - Timer 3 count value set to every 8,192 counts (TW3A instruction)

4. Clearing interrupt request
   - Clear the timer 3 interrupt start condition.
   - Timer 3 interrupt request flag T3F = 0
   - Timer 3 interrupt start condition cleared (SNZT3 instruction)

* Precautions to be taken when interrupt requests are cleared
  If step (4) is executed, be sure to insert a NOP instruction after the SNZT3 instruction because the next instruction may be skipped depending on the state of the interrupt request flag T3F.

5. Starting timer operation
   - Restart the temporarily stopped timer 3 operation.
   - Timer 3 count value set to every 8,192 counts (TW3A instruction)

6. Enabling interrupt
   - Reenable the temporarily disabled timer 3 interrupt.
   - Generation of timer 3 interrupt enabled (TV2A instruction)

Execution of fixed-cycle counter started
(1) Clearing the flag WDF1
Clear the watchdog timer flag WDF1 to 0. “0” Watchdog timer flag WDF1 cleared (WRST instruction)

* Precautions to be taken when the watchdog timer flag is cleared
If step (1) is executed, be sure to insert a NOP instruction after the WRST instruction because the next instruction may be skipped depending on the state of the interrupt request flag WDF1.

Execution of the main routine
Repeated

Do not clear the watchdog timer flag WDF1 in an interrupt handler. Even when the program has gone wild, interrupts may be at work.

When placed into power-down mode

\[
\begin{align*}
\text{WRST} & \quad ; \text{Clear the flag WDF} \\
\text{NOP} & \\
\text{DI} & \quad ; \text{Disable interrupt} \\
\text{EPOF} & \quad ; \text{Enable POF instruction} \\
\text{POF2} & \\
\text{\downarrow} & \quad \text{Oscillation stopped (power-down mode)}
\end{align*}
\]

In power-down mode, the flags WEF, WDF1 and WDF2 are initialized. However, if the flag WDF2 is set to 1 at the same time power-down mode is entered into, the microcomputer may be reset. If the watchdog timer and power-down mode are used, be sure to execute the WRST instruction to initialize the flag WDF1 immediately before entering power-down mode.

Figure 4.7 Example for Using the Watchdog Timer
5. Reference Documents

Data sheet
455A Group Data Sheet
(The latest version is available from the Renesas Technology Web site.)

Technical news / Technical Update
(The latest information is available from the Renesas Technology Web site.)
6. Sample Programs

Sample programs are available from the Renesas Technology Web site.
To download one, click the screen menu "Application Note" on the left side of 455A group Web site.
Renesas Web Site and Where to Contact

Renesas Technology Web site:
http://japan.renesas.com/

Where to contact:
http://japan.renesas.com/inquiry
csc@renesas.com

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