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455A Group

Power-Down Function

1. Abstract

This document presents the method for using the power-down function of the 455A-group microcomputers and shows an application example.

2. Introduction

The application example explained in this document applies for use with the microcomputers and under the conditions described below.

- Microcomputer : 455A group
- Oscillator frequency : 32.768 kHz as sub-clock f(XCIN), however
- System clock : Used in through mode (not frequency divided)

3. Related Registers

3.1 Interrupt Control Register V2

Table 3.1 shows the bit configuration of Interrupt Control Register V2.

For write to the register V2, first set a value in the register A and then use the TV2A instruction.

Furthermore, the TAV2 instruction may be used to transfer the content of register V2 to the register A.

Table 3.1 Bit Configuration of Interrupt Control Register V2

Interrupt Control Register V2		When reset: 0000 ₂	When powered down: 0000 ₂	R/W TAV2/TV2A
V2 ₃	Not used	0	This bit has no functions assigned, but can be read/written.	
		1		
V2 ₂	Not used	0	This bit has no functions assigned, but can be read/written.	
		1		
V2 ₁	Not used	0	This bit has no functions assigned, but can be read/written.	
		1		
V2 ₀	Timer 3 interrupt enable bit	0	Disables interrupt generation (SNZT3 instruction effective)	
		1	Enables interrupt generation (SNZT3 instruction has no effect)	

Note 1: The letter R denotes “readable,” and the letter W denotes “writable.”

Note 2: : Unused bits during power-down function setting.

3.2 Interrupt Control Register I1

Table 3.2 shows the bit configuration of Interrupt Control Register I1.

For write to the register I1, first set a value in the register A and then use the TI1A instruction.

Furthermore, the TAI1 instruction may be used to transfer the content of register I1 to the register A.

Table 3.2 Bit Configuration of Interrupt Control Register I1

Interrupt Control Register I1		When reset: 0000 ₂	When powered down: State retained	R/W TAI1/TI1A
I1 ₃	INT pin input control bit ^{Note 2}	0	Disables input	
		1	Enables input	
I1 ₂	INT pin interrupt active waveform/return level select bit ^{Note 2}	0	Falling waveform/low level (SNZI0 instruction recognizes low level on INT pin)	
		1	Rising waveform/high level (SNZI0 instruction recognizes high level on INT pin)	
I1 ₁	INT pin edge detection circuit control bit	0	Detects one edge	
		1	Detects both edges	
I1 ₀	INT pin timer 1 count start synchronizing circuit select bit	0	Deselects timer 1 count start synchronizing circuit	
		1	Selects timer 1 count start synchronizing circuit	

Note 1: The letter R denotes “readable,” and the letter W denotes “writable.”

Note 2: When the contents of these bits (I1₂ or I1₃) are changed, the external interrupt request flag (EXF0) may be set.

Note 3: : Unused bits during power-down function setting.

3.3 LCD Control Register L1

Table 3.3 shows the bit configuration of LCD Control Register L1.

For write to the register L1, first set a value in the register A and then use the TL1A instruction.

Furthermore, the TAL1 instruction may be used to transfer the content of register L1 to the register A.

Table 3.3 Bit Configuration of LCD Control Register L1

LCD Control Register L1		When reset: 0000 ₂		When powered down: State retained		R/W TAL1/TL1A
L13	LCD power supply internal dividing resistor select bit ^{Note 2}	0	2r × 3, 2r × 2			
		1	r × 3, r × 2			
L12	LCD control bit	0	Stop (turned off)			
		1	Start			
L11	LCD duty cycle/bias select bit	L11	L10	Duty cycle		Bias
		0	0	Use prohibited		Use prohibited
		0	1	1/2		1/2
L10		1	0	1/3		1/3
		1	1	1/4		1/3

Note 1: The letter R denotes “readable,” and the letter W denotes “writable.”

Note 2: When 1/3 bias is selected, a “x3” resistor is used; when 1/2 bias is selected, a “x2” resistor is used.

3.4 LCD Control Register L2

Table 3.4 shows the bit configuration of LCD Control Register L2.

For write to the register L2, first set a value in the register A and then use the TL2A instruction.

Table 3.4 Bit Configuration of LCD Control Register L2

LCD Control Register L2		When reset: 0000 ₂		When powered down: State retained		W TL2A
L23	SEG0/V _{LC3} pin function select bit ^{Note 2}	0	SEG0			
		1	V _{LC3}			
L22	SEG1/V _{LC2} pin function select bit ^{Note 3}	0	SEG1			
		1	V _{LC2}			
L21	SEG2/V _{LC1} pin function select bit ^{Note 3}	0	SEG2			
		1	V _{LC1}			
L20	LCD power supply internal dividing resistor control bit	0	Enables internal dividing resistor			
		1	Disables internal dividing resistor			

Note 1: The letter W denotes “writable.”

Note 2: When SEG0 pin is selected, VLC3 is connected to VDD internally in the chip.

Note 3: When SEG1 and SEG2 pins are selected, always be sure to use the internal dividing resistor.

3.5 LCD Control Register L3

Table 3.5 shows the bit configuration of the LCD Control Register L3.

For write to the register L3, first set a value in the register A and then use the TL3A instruction.

Table 3.5 Bit Configuration of LCD Control Register L3

LCD Control Register L3		When reset: 1111 ₂	When powered down: State retained	W TL3A
L3 ₃	P2 ₃ /SEG ₂₇ pin function select bit	0	SEG ₂₇	
		1	P2 ₃	
L3 ₂	P2 ₂ /SEG ₂₆ pin function select bit	0	SEG ₂₆	
		1	P2 ₂	
L3 ₁	P2 ₁ /SEG ₂₅ pin function select bit	0	SEG ₂₅	
		1	P2 ₁	
L3 ₀	P2 ₀ /SEG ₂₄ pin function select bit	0	SEG ₂₄	
		1	P2 ₀	

Note 1: The letter W denotes “writable.”

3.6 LCD Control Register C1

Table 3.6 shows the bit configuration of the LCD Control Register C1.

For write to the register C1, first set a value in the register A and then use the TC1A instruction.

Table 3.6 Bit Configuration of LCD Control Register C1

LCD Control Register C1		When reset: 1111 ₂	When powered down: State retained	W TC1A
C1 ₃	P0 ₃ /SEG ₁₉ pin function select bit	0	SEG ₁₉	
		1	P0 ₃	
C1 ₂	P0 ₂ /SEG ₁₈ pin function select bit	0	SEG ₁₈	
		1	P0 ₂	
C1 ₁	P0 ₁ /SEG ₁₇ pin function select bit	0	SEG ₁₇	
		1	P0 ₁	
C1 ₀	P0 ₀ /SEG ₁₆ pin function select bit	0	SEG ₁₆	
		1	P0 ₀	

Note 1: The letter W denotes “writable.”

3.7 LCD Control Register C2

Table 3.7 shows the bit configuration of the LCD Control Register C2.

For write to the register C2, first set a value in the register A and then use the TC2A instruction.

Table 3.7 Bit Configuration of LCD Control Register C2

LCD Control Register C2		When reset: 1111 ₂	When powered down: State retained	W TC2A
C2 ₃	P1 ₃ /SEG ₂₃ pin function select bit	0	SEG ₂₃	
		1	P1 ₃	
C2 ₂	P1 ₂ /SEG ₂₂ pin function select bit	0	SEG ₂₂	
		1	P1 ₂	
C2 ₁	P1 ₁ /SEG ₂₁ pin function select bit	0	SEG ₂₁	
		1	P1 ₁	
C2 ₀	P1 ₀ /SEG ₂₀ pin function select bit	0	SEG ₂₀	
		1	P1 ₀	

Note 1: The letter W denotes “writable.”

3.8 LCD Control Register C3

Table 3.8 shows the bit configuration of the LCD Control Register C3.

For write to the register C3, first set a value in the register A and then use the TC3A instruction.

Table 3.8 Bit Configuration of LCD Control Register C3

LCD Control Register C3		When reset: 1111 ₂	When powered down: State retained	W TC3A
C3 ₃	P3 ₃ /SEG ₃₁ pin function select bit	0	SEG ₃₁	
		1	P3 ₃	
C3 ₂	P3 ₂ /SEG ₃₀ pin function select bit	0	SEG ₃₀	
		1	P3 ₂	
C3 ₁	P3 ₁ /SEG ₂₉ pin function select bit	0	SEG ₂₉	
		1	P3 ₁	
C3 ₀	P3 ₀ /SEG ₂₈ pin function select bit	0	SEG ₂₈	
		1	P3 ₀	

Note 1: The letter W denotes “writable.”

3.9 Timer Control Register W3

Table 3.9 shows the bit configuration of Timer Control Register W3.

For write to the register W3, first set a value in the register A and then use the TW3A instruction.

Furthermore, the TAW3 instruction may be used to transfer the content of register W3 to the register A.

Table 3.9 Bit Configuration of Timer Control Register W3

Timer Control Register W3		When reset: 0000 ₂		When powered down: State retained		R/W TAW3/TW3A
W3 ₃	Timer 3 control bit	0	Stop (initial state)			
		1	Start			
W3 ₂	Timer 3 count value select bit	W3 ₂	W3 ₁	W3 ₀	Count value	
		0	0	0	Generates underflow every 512 counts	
		0	0	1	Generates underflow every 1,024 counts	
W3 ₁		0	1	0	Generates underflow every 2,048 counts	
		0	1	1	Generates underflow every 4,096 counts	
		1	0	0	Generates underflow every 8,192 counts	
W3 ₀		1	0	1	Generates underflow every 16,384 counts	
		1	1	0	Generates underflow every 32,768 counts	
		1	1	1	Generates underflow every 65,536 counts	

Note 1: The letter R denotes “readable,” and the letter W denotes “writable.”

3.10 Timer Control Register W4

Table 3.10 shows the bit configuration of Timer Control Register W4.

For write to the register W4, first set a value in the register A and then use the TW4A instruction.

Furthermore, the TAW4 instruction may be used to transfer the content of register W4 to the register A.

Table 3.10 Bit Configuration of Timer Control Register W4

Timer Control Register W4		When reset: 0000 ₂		When powered down: State retained		R/W TAW4/TW4A
W4 ₃	Timer LC control bit	0	Stop (state retained)			
		1	Start			
W4 ₂	Timer LC count source select bit	0	Bit 4 of timer 3 (T3 ₄)			
		1	System clock (STCK)			
W4 ₁	CNTR pin output auto control circuit select bit	0	Deselects CNTR pin output auto control circuit			
		1	Selects CNTR pin output auto control circuit			
W4 ₀	CNTR pin input count edge select bit	0	Falling edge			
		1	Rising edge			

Note 1: The letter R denotes “readable,” and the letter W denotes “writable.”

Note 2: : Unused bits during power-down function setting.

3.11 Timer Control Register W5

Table 3.11 shows the bit configuration of the Timer Control Register W5.

For write to the register W5, first set a value in the register A and then use the TW5A instruction.

Furthermore, the TAW5 instruction may be used to transfer the content of register W5 to the register A.

Table 3.11 Bit Configuration of Timer Control Register W5

Timer Control Register W5		When reset: 0000 ₂		When powered down: State retained	R/W TAW5/TW5A
W5 ₃	Unused	0	This bit has no functions, but can be accessed for read/write.		
		1	This bit has no functions, but can be accessed for read/write.		
W5 ₂	Unused	0	This bit has no functions, but can be accessed for read/write.		
		1	This bit has no functions, but can be accessed for read/write.		
W5 ₁	Timer 3 count source select bit	W5 ₁	W5 ₀	Count source	
		0	0	XCIN input	
		0	1	ORCLK input	
		1	0	Low-speed on-chip oscillator input (LSOCO)	
W5 ₀		1	1	High-speed on-chip oscillator input (HSOCO)	

Note 1: The letter R denotes “readable,” and the letter W denotes “writable.”

Note 2: : Unused bits during power-down function setting.

3.12 Key-on Wakeup Control Register K2

Table 3.12 shows the bit configuration of Key-on Wakeup Control Register K2.

For write to the register K2, first set a value in the register A and then use the TK2A instruction.

Furthermore, the TAK2 instruction may be used to transfer the content of register K2 to the register A.

Table 3.12 Bit Configuration of Key-on Wakeup Control Register K2

Key-on Wakeup Control Register K2		When reset: 0000 ₂		When powered down: State retained	R/W TAK2/TK2A
K2 ₂	Port P3 ₂ and P3 ₃ ^{Note 3} key-on wakeup control bit	0	Disables key-on wakeup		
		1	Enables key-on wakeup		
K2 ₂	Port P3 ₀ and P3 ₁ ^{Note 2} key-on wakeup control bit	0	Disables key-on wakeup		
		1	Enables key-on wakeup		
K2 ₁	INT pin return condition select bit	0	Level returned		
		1	Edge returned		
K2 ₀	INT pin key-on wakeup control bit	0	Disables key-on wakeup		
		1	Enables key-on wakeup		

Note 1: The letter R denotes “readable,” and the letter W denotes “writable.”

Note 2: To disable the key-on wakeup function of ports P3₀ and P3₁ (K2₂ = 0), set the values of registers K3₀ and K3₁ to 0.

Note 3: To disable the key-on wakeup function of ports P3₂ and P3₃ (K2₃ = 0), set the values of registers K3₂ and K3₃ to 0.

Note 4: : Unused bits during power-down function setting.

3.13 Port Output Mode Control Register FR2

Table 3.13 shows the bit configuration of Port Output Mode Control Register FR2.

For write to the register FR2, first set a value in the register A and then use the TFR2A instruction.

Table 3.13 Bit Configuration of Port Output Mode Control Register FR2

Port Output Mode Control Register FR2		When reset: 0000 ₂	When powered down: State retained	W TFR2A
FR2 ₃	Port P3 ₂ and P3 ₃ output mode select bit	0	N-channel open-drain output	
		1	CMOS output	
FR2 ₂	Port P3 ₀ and P3 ₁ output mode select bit	0	N-channel open-drain output	
		1	CMOS output	
FR2 ₁	Port D ₅ output mode select bit	0	N-channel open-drain output	
		1	CMOS output	
FR2 ₀	Port D ₄ output mode select bit	0	N-channel open-drain output	
		1	CMOS output	

Note 1: The letter W denotes “writable.”

Note 2: : Unused bits during power-down function setting.

3.14 Clock Control Register RG

Table 3.14 shows the bit configuration of the Clock Control Register RG.

For write to the register RG, first set a value in the register A and then use the TRGA instruction.

Table 3.14 Bit Configuration of Clock Control Register RG

Clock Control Register RG		When reset: 000 ₂	When powered down: State retained	W TRGA
RG ₃	Low-speed on-chip oscillator (f(LSOCO)) control bit ^{Note 3}	0	Low-speed on-chip oscillator (f(LSOCO)) to oscillate	
		1	Low-speed on-chip oscillator (f(LSOCO)) from oscillating	
RG ₂	Sub-clock (f(XCIN)) control bit ^{Note 3}	0	Enables sub-clock (f(XCIN)) to oscillate, with ports D ₆ and D ₇ unselected	
		1	Stops sub-clock (f(XCIN)) from oscillating, with ports D ₆ and D ₇ selected	
RG ₁	Main clock (f(XIN)) control bit ^{Note 3}	0	Enables main clock (f(XIN)) to oscillate	
		1	Stops main clock (f(XIN)) from oscillating	
RG ₀	On-chip oscillator (f(RING)) control bit ^{Note 3}	0	Enables on-chip oscillator (f(RING)) to oscillate	
		1	Stops on-chip oscillator (f(RING)) from oscillating	

Note 1: The letter W denotes “writable.”

Note 2: : Unused bits during power-down function setting.

Note 3: Any oscillator circuit that is selected for the system clock cannot be turned off.

4. Application Example for the Power-Down Function

4.1 Time-of-Day Clock Mode

A combined use of a 32.768 kHz crystal resonator for the sub-clock and the POF instruction makes it possible to produce a low power, yet highly accurate time-of-day clock.

Point : Use of the POF instruction helps to reduce the power consumption in the chip.

Specification : An LCD and a 32.768 kHz crystal resonator are used to show the time of day.

Figure 4.1 shows an example of an LCD display panel. Figure 4.2 shows an example of RAM arrangement for LCD display. Figure 4.3 shows an example of a segment arrangement for an LCD display panel.

Figure 4.4 shows a state transition diagram. Figure 4.5 shows an example of how to set the registers for operation in time-of-day clock mode (example 1). Figure 4.6 shows an example of how to set the registers for operation in time-of-day clock mode (example 2).

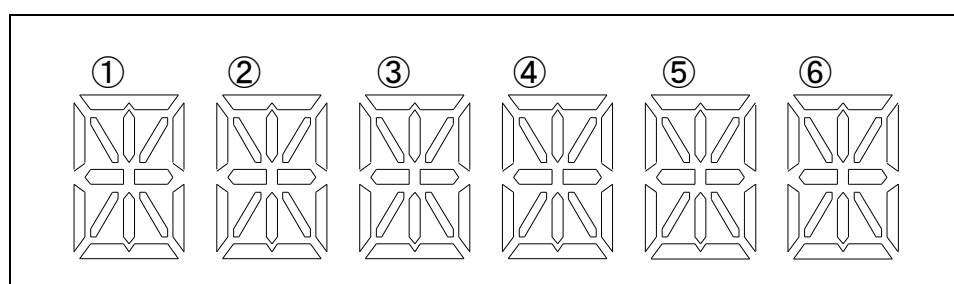


Figure 4.1 Example of an LCD Display Panel

Register Z	1															
Register X	12				13				14				15			
Register Y	3	2	1	0	3	2	1	0	3	2	1	0	3	2	1	0
8	SEG0	SEG0	SEG0	SEG0	SEG8	SEG8	SEG8	SEG8	SEG16	SEG16	SEG16	SEG16	SEG24	SEG24	SEG24	SEG24
9	SEG1	SEG1	SEG1	SEG1	SEG9	SEG9	SEG9	SEG9	SEG17	SEG17	SEG17	SEG17	SEG25	SEG25	SEG25	SEG25
10	SEG2	SEG2	SEG2	SEG2	SEG10	SEG10	SEG10	SEG10	SEG18	SEG18	SEG18	SEG18	SEG26	SEG26	SEG26	SEG26
11	SEG3	SEG3	SEG3	SEG3	SEG11	SEG11	SEG11	SEG11	SEG19	SEG19	SEG19	SEG19	SEG27	SEG27	SEG27	SEG27
12	SEG4	SEG4	SEG4	SEG4	SEG12	SEG12	SEG12	SEG12	SEG20	SEG20	SEG20	SEG20	SEG28	SEG28	SEG28	SEG28
13	SEG5	SEG5	SEG5	SEG5	SEG13	SEG13	SEG13	SEG13	SEG21	SEG21	SEG21	SEG21	SEG29	SEG29	SEG29	SEG29
14	SEG6	SEG6	SEG6	SEG6	SEG14	SEG14	SEG14	SEG14	SEG22	SEG22	SEG22	SEG22	SEG30	SEG30	SEG30	SEG30
15	SEG7	SEG7	SEG7	SEG7	SEG15	SEG15	SEG15	SEG15	SEG23	SEG23	SEG23	SEG23	SEG31	SEG31	SEG31	SEG31
COM	COM3	COM2	COM1	COM0	COM3	COM2	COM1	COM0	COM3	COM2	COM1	COM0	COM3	COM2	COM1	COM0

Figure 4.2 Example of RAM Arrangement for LCD Display

Register Z	1															
Register X	12				13				14							
Register Y	3	2	1	0	3	2	1	0	3	2	1	0				
8	①-d	①-c	①-b	①-a	③-d	③-c	③-b	③-a	⑤-d	⑤-c	⑤-b	⑤-a				
9	①-h	①-g	①-f	①-e	③-h	③-g	③-f	③-e	⑤-h	⑤-g	⑤-f	⑤-e				
10	①-k	①-j		①-i	③-k	③-j		③-i	⑤-k	⑤-j		⑤-i				
11	①-n	①-l		①-m	③-n	③-l		③-m	⑤-n	⑤-l		⑤-m				
12	②-d	②-c	②-b	②-a	④-d	④-c	④-b	④-a	⑥-d	⑥-c	⑥-b	⑥-a				
13	②-h	②-g	②-f	②-e	④-h	④-g	④-f	④-e	⑥-h	⑥-g	⑥-f	⑥-e				
14	②-k	②-j		②-i	④-k	④-j		④-i	⑥-k	⑥-j		⑥-i				
15	②-n	②-l		②-m	④-n	④-l		④-m	⑥-n	⑥-l		⑥-m				
COM	COM3	COM2	COM1	COM0	COM3	COM2	COM1	COM0	COM3	COM2	COM1	COM0				

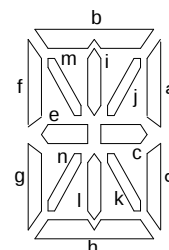


Figure 4.3 Example of a Segment Arrangement for an LCD Display Panel

4.2 RAM Backup Mode

Use of the POF2 instruction permits clock oscillations to be stopped while retaining the RAM and reset circuit functions and states intact, making it possible to reduce the power consumption in the chip without a possibility of losing RAM data.

Point : Use of the POF2 instruction helps to reduce the power consumption in the chip.

Specification : The microcomputer is waked up with the press of a switch (key-on wakeup), and the number of wakeup times is displayed up to 9 times on an LCD. When 9 times is exceeded, the count recycles to 0 and starts over. This application uses the same LCD panel that is used in Section 4.1, "Time-of-Day Clock Mode."

Figure 4.7 shows an example of how to set the registers for RAM backup mode (example 1). Figure 4.8 shows an example of how to set the registers for RAM backup mode (example 2). Figure 4.9 shows an example of how to set the registers for RAM backup mode (example 3).

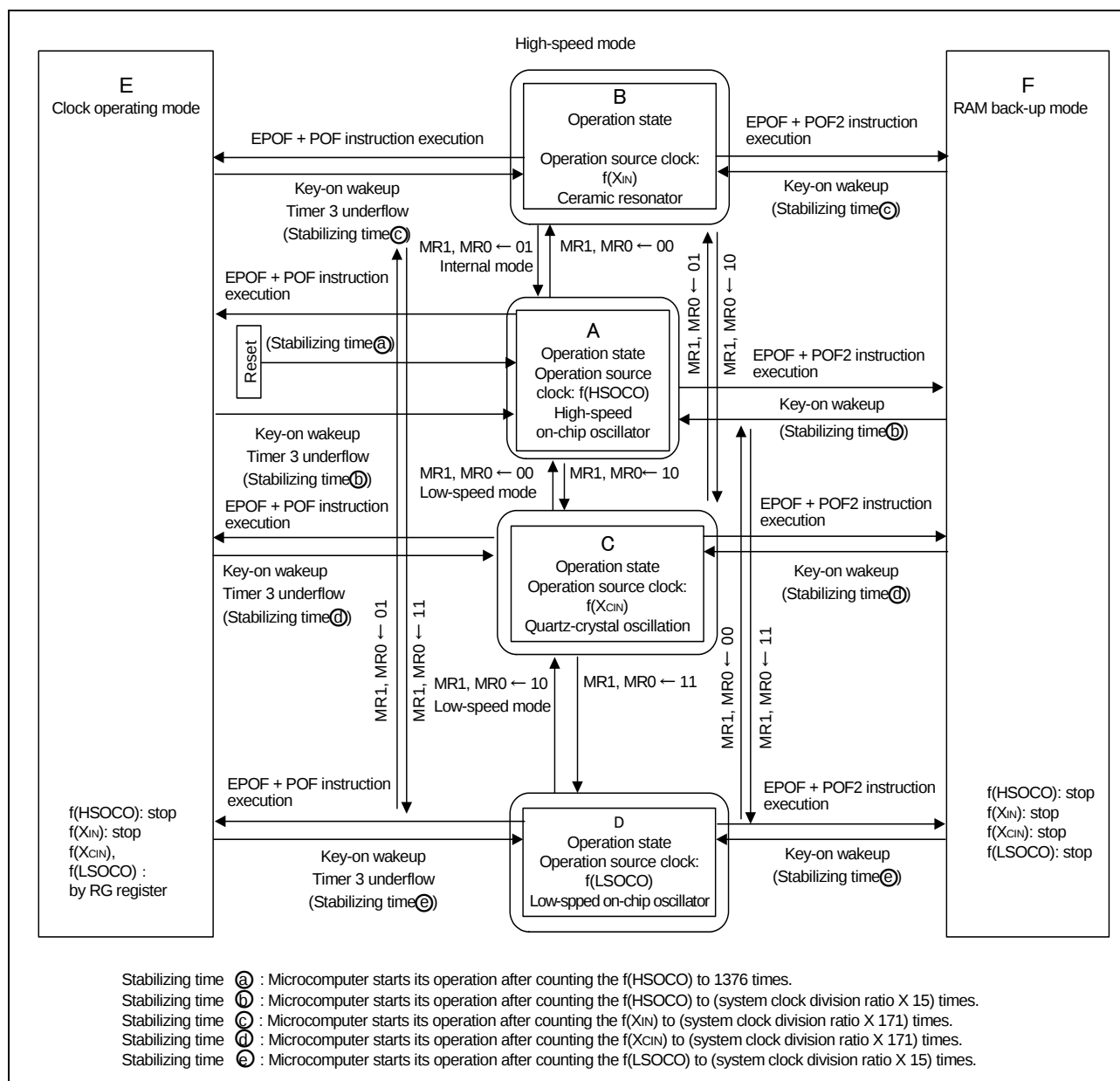


Figure 4.4 State Transition Diagram

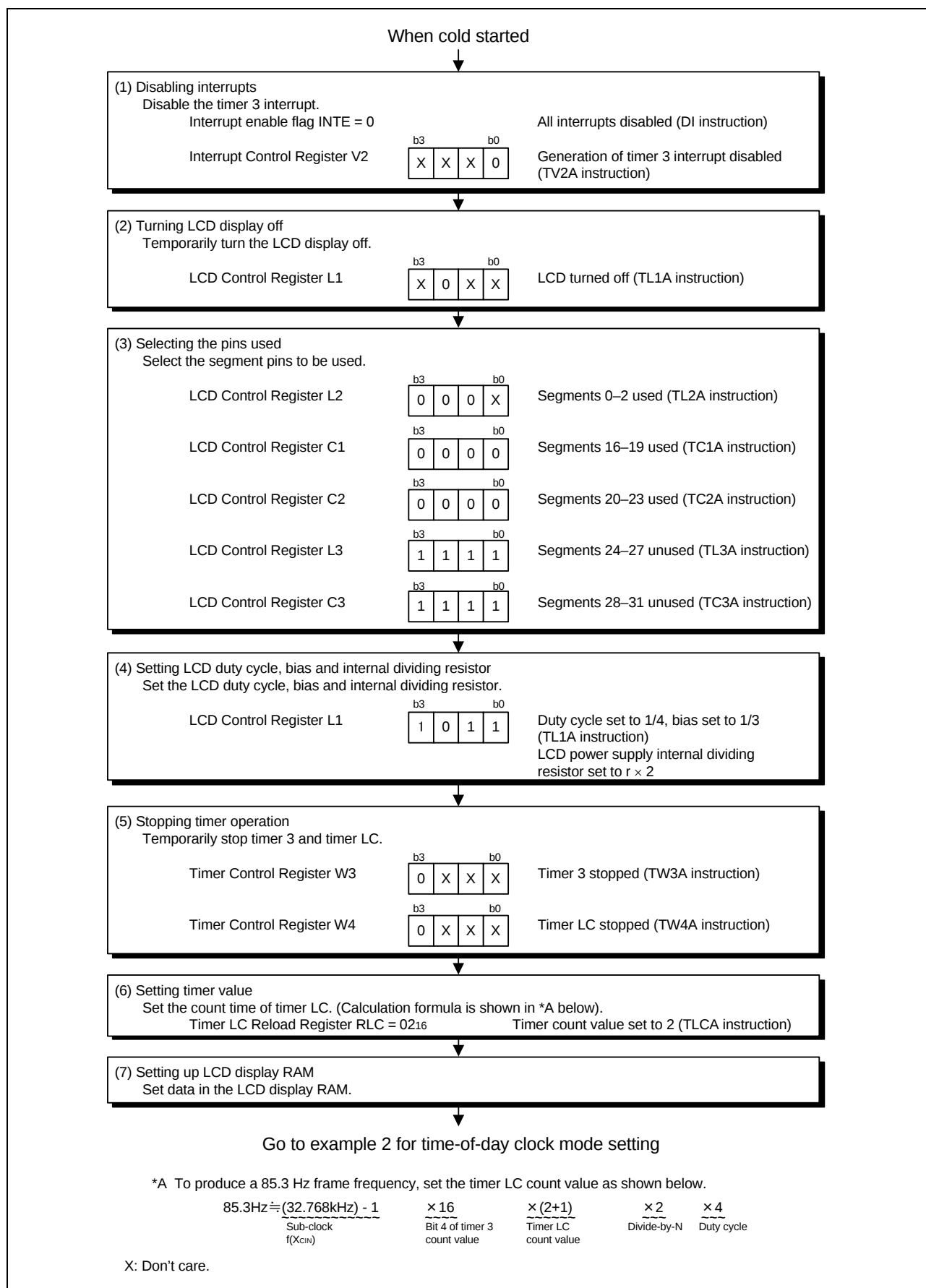


Figure 4.5 Example 1 for Time-of-Day Clock Mode Setting

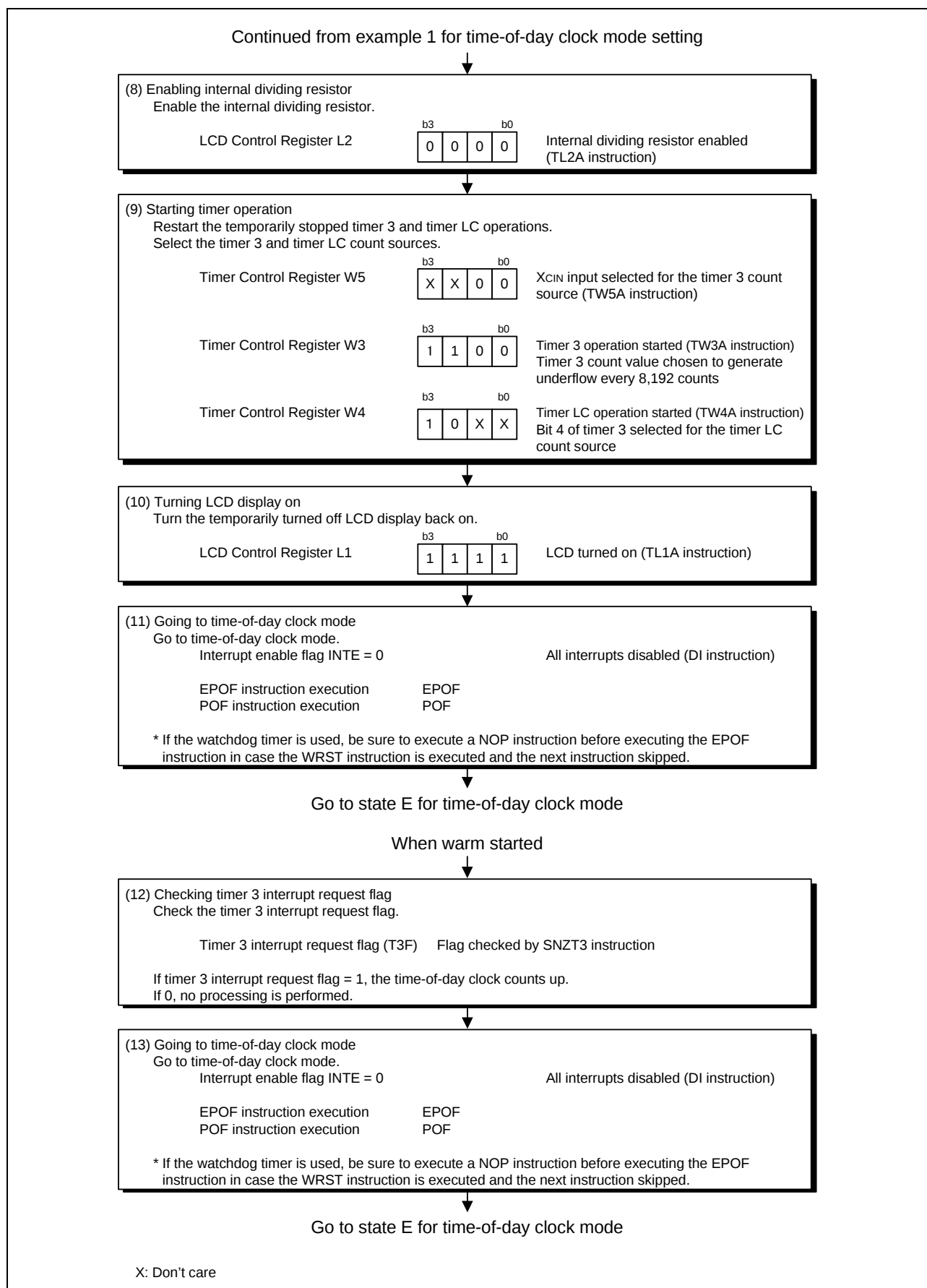


Figure 4.6 Example 2 for Time-of-Day Clock Mode Setting

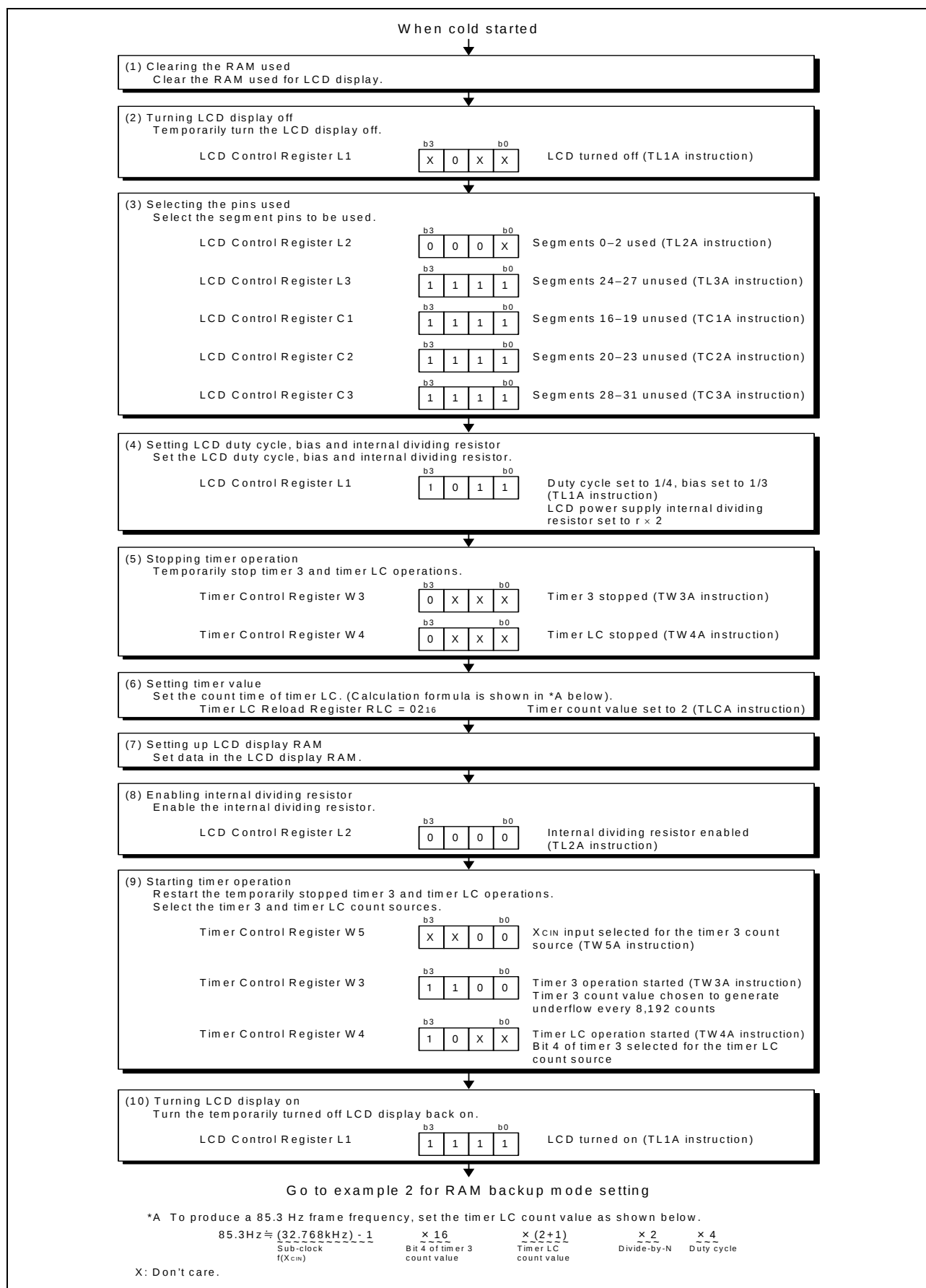


Figure 4.7 Example 1 for RAM Backup Mode Setting

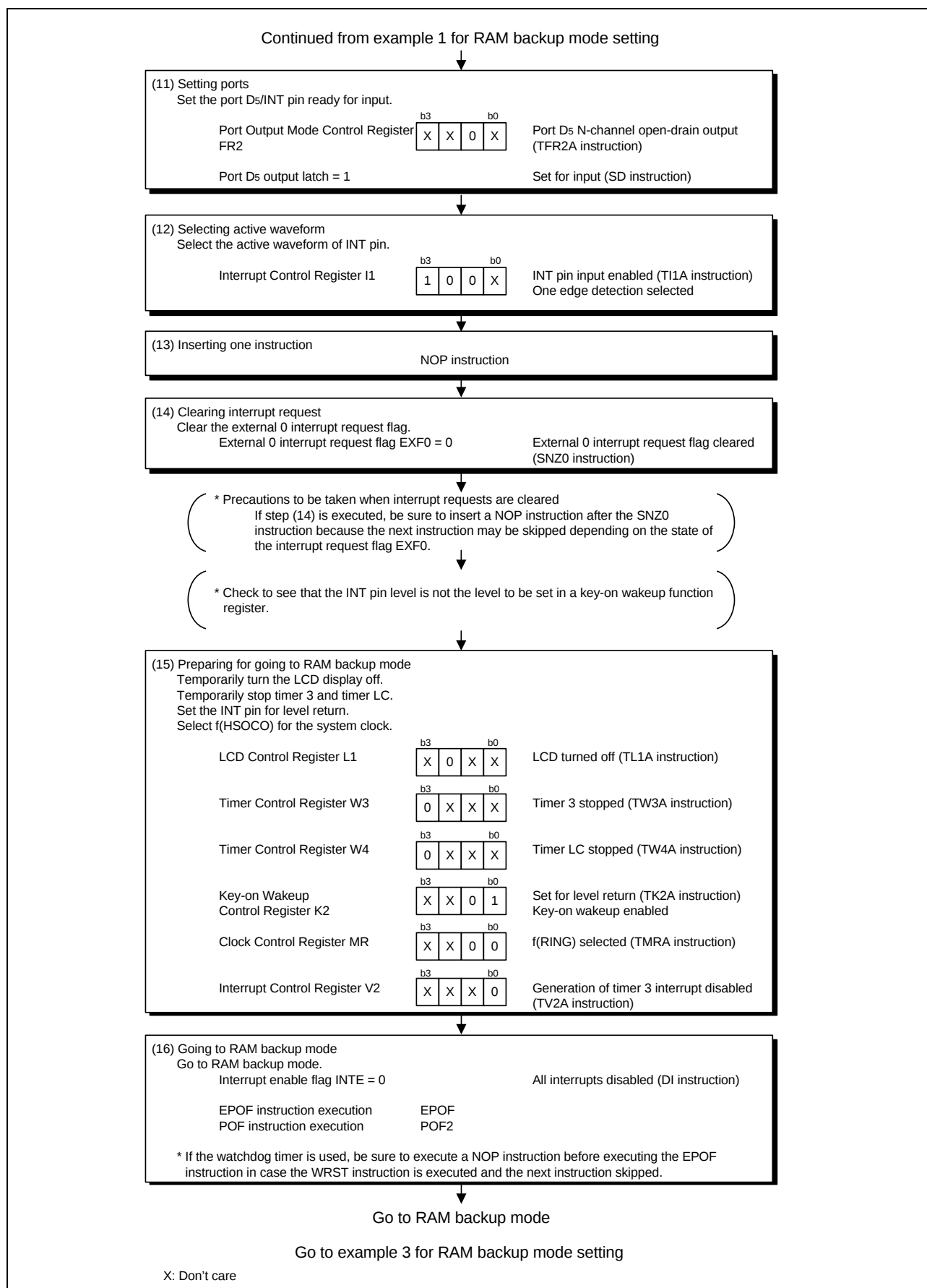


Figure 4.8 Example 2 for RAM Backup Mode Setting

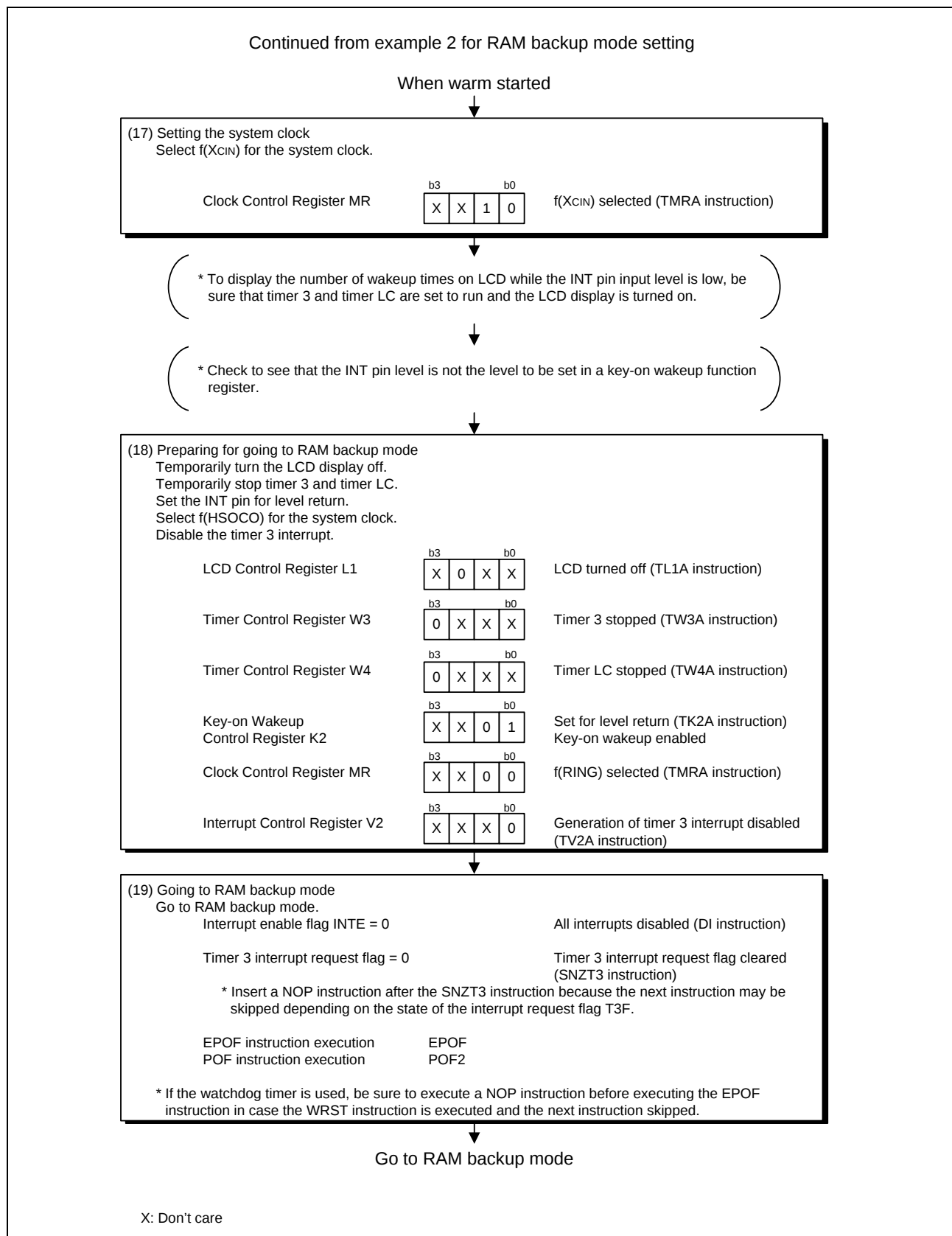


Figure 4.9 Example 3 for RAM Backup Mode Setting

5. Reference Documents

Data sheet

455A Group Data sheet

(The latest version is available from the Renesas Technology Web site.)

Technical news / Technical Update

(The latest information is available from the Renesas Technology Web site.)

6. Sample Programs

Sample programs are available from the Renesas Technology Web site.

To download one, click the screen menu “Application Note” on the left side of 455A group Web site.

Renesas Web Site and Where to Contact

Renesas Technology Web site:
<http://japan.renesas.com/>

Where to contact:
<http://japan.renesas.com/inquiry>
csc@renesas.com

Revision history	455A Group Power-Down Function
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Rev.	Date	Description	
		Page	Points
1.00	2008.02.29	–	First edition issued

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