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4559 Group

Power-Down Function

1. Abstract

This document shows an example of how to set the power-down function of the 4559 group of Renesas microcomputers and an application example for using it.

2. Introduction

The application example explained in this document applies for use with the microcomputers and under the conditions described below.

- Microcomputer : 4559 group
- Oscillator frequency : 32.768 kHz as sub-clock f(XCIN), however
- System clock : Used in through mode (not frequency divided)

Please note that the sample program for the 4559 group may somewhere in it manipulate the bits of unused functions for reasons of bit arrangement in the control registers. The values of these bits in a user system should be set to suit the usage condition of the system.

3. Related Registers

3.1 Interrupt Control Register V2

Table 3.1 shows the bit configuration of Interrupt Control Register V2.

For write to the register V2, first set a value in the register A and then use the TV2A instruction.

Furthermore, the TAV2 instruction may be used to transfer the content of register V2 to the register A.

Table 3.1 Bit Configuration of Interrupt Control Register V2

Interrupt Control Register V2		When reset: 0000_2		When powered down: 0000_2	R/W TAV2/TV2A
$V2_3$	Not used	0	This bit has no functions assigned, but can be read/written.		
		1			
$V2_2$	Not used	0	This bit has no functions assigned, but can be read/written.		
		1			
$V2_1$	Not used	0	This bit has no functions assigned, but can be read/written.		
		1			
$V2_0$	Timer 3 interrupt enable bit	0	Disables interrupt generation (SNZT3 instruction effective)		
		1	Enables interrupt generation (SNZT3 instruction has no effect)		

Note 1: The letter R denotes “readable,” and the letter W denotes “writable.”

Note 2: : Unused bits during power-down function setting.

3.2 Interrupt Control Register I1

Table 3.2 shows the bit configuration of Interrupt Control Register I1.

For write to the register I1, first set a value in the register A and then use the TI1A instruction.

Furthermore, the TAI1 instruction may be used to transfer the content of register I1 to the register A.

Table 3.2 Bit Configuration of Interrupt Control Register I1

Interrupt Control Register I1		When reset: 0000_2		When powered down: State retained	R/W TAI1/TI1A
$I1_3$	INT pin input control bit Note 2	0	Disables input		
		1	Enables input		
$I1_2$	INT pin interrupt active waveform/return level select bit Note 2	0	Falling waveform/low level (SNZI0 instruction recognizes low level on INT pin)		
		1	Rising waveform/high level (SNZI0 instruction recognizes high level on INT pin)		
$I1_1$	INT pin edge detection circuit control bit	0	Detects one edge		
		1	Detects both edges		
$I1_0$	INT pin timer 1 count start synchronizing circuit select bit	0	Deselects timer 1 count start synchronizing circuit		
		1	Selects timer 1 count start synchronizing circuit		

Note 1: The letter R denotes “readable,” and the letter W denotes “writable.”

Note 2: When the contents of these bits ($I1_2$ or $I1_3$) are changed, the external interrupt request flag (EXF0) may be set.

Note 3: : Unused bits during power-down function setting.

3.3 LCD Control Register L1

Table 3.3 shows the bit configuration of LCD Control Register L1.

For write to the register L1, first set a value in the register A and then use the TL1A instruction.

Furthermore, the TAL1 instruction may be used to transfer the content of register L1 to the register A.

Table 3.3 Bit Configuration of LCD Control Register L1

LCD Control Register L1		When reset: 0000_2	When powered down: State retained		R/W TAL1/TL1A
$L1_3$	LCD power supply internal dividing resistor select bit Note 2	0	2r × 3, 2r × 2		
		1	r × 3, r × 2		
$L1_2$	LCD control bit	0	Stop (turned off)		
		1	Start		
$L1_1$	LCD duty cycle/bias select bit	$L1_1$	$L1_0$	Duty cycle	Bias
		0	0	Use prohibited	Use prohibited
		0	1	1/2	1/2
$L1_0$		1	0	1/3	1/3
		1	1	1/4	1/3

Note 1: The letter R denotes “readable,” and the letter W denotes “writable.”

Note 2: When 1/3 bias is selected, a “x3” resistor is used; when 1/2 bias is selected, a “x2” resistor is used.

3.4 LCD Control Register L2

Table 3.4 shows the bit configuration of LCD Control Register L2.

For write to the register L2, first set a value in the register A and then use the TL2A instruction.

Table 3.4 Bit Configuration of LCD Control Register L2

LCD Control Register L2		When reset: 0000_2	When powered down: State retained	W TL2A
$L2_3$	SEG_0/V_{LC3} pin function select bit Note 2	0	SEG_0	
		1	V_{LC3}	
$L2_2$	SEG_1/V_{LC2} pin function select bit Note 3	0	SEG_1	
		1	V_{LC2}	
$L2_1$	SEG_2/V_{LC1} pin function select bit Note 3	0	SEG_2	
		1	V_{LC1}	
$L2_0$	LCD power supply internal dividing resistor control bit	0	Enables internal dividing resistor	
		1	Disables internal dividing resistor	

Note 1: The letter W denotes “writable.”

Note 2: When SEG_0 pin is selected, V_{LC3} is connected to VDD internally in the chip.

Note 3: When SEG_1 and SEG_2 pins are selected, always be sure to use the internal dividing resistor.

3.5 LCD Control Register L3

Table 3.5 shows the bit configuration of the LCD Control Register L3.

For write to the register L3, first set a value in the register A and then use the TL3A instruction.

Table 3.5 Bit Configuration of LCD Control Register L3

LCD Control Register L3		When reset: 1111_2		When powered down: State retained	W TL3A
$L3_3$	$P2_3$/SEG_{27} pin function select bit	0	SEG_{27}		
		1	$P2_3$		
$L3_2$	$P2_2$/SEG_{26} pin function select bit	0	SEG_{26}		
		1	$P2_2$		
$L3_1$	$P2_1$/SEG_{25} pin function select bit	0	SEG_{25}		
		1	$P2_1$		
$L3_0$	$P2_0$/SEG_{24} pin function select bit	0	SEG_{24}		
		1	$P2_0$		

Note 1: The letter W denotes “writable.”

3.6 LCD Control Register C1

Table 3.6 shows the bit configuration of the LCD Control Register C1.

For write to the register C1, first set a value in the register A and then use the TC1A instruction.

Table 3.6 Bit Configuration of LCD Control Register C1

LCD Control Register C1		When reset: 1111_2		When powered down: State retained	W TC1A
$C1_3$	$P0_3$/SEG_{19} pin function select bit	0	SEG_{19}		
		1	$P0_3$		
$C1_2$	$P0_2$/SEG_{18} pin function select bit	0	SEG_{18}		
		1	$P0_2$		
$C1_1$	$P0_1$/SEG_{17} pin function select bit	0	SEG_{17}		
		1	$P0_1$		
$C1_0$	$P0_0$/SEG_{16} pin function select bit	0	SEG_{16}		
		1	$P0_0$		

Note 1: The letter W denotes “writable.”

3.7 LCD Control Register C2

Table 3.7 shows the bit configuration of the LCD Control Register C2.

For write to the register C2, first set a value in the register A and then use the TC2A instruction.

Table 3.7 Bit Configuration of LCD Control Register C2

LCD Control Register C2		When reset: 1111_2		When powered down: State retained	W TC2A
$C2_3$	$P1_3/SEG_{23}$ pin function select bit	0	SEG_{23}		
		1	$P1_3$		
$C2_2$	$P1_2/SEG_{22}$ pin function select bit	0	SEG_{22}		
		1	$P1_2$		
$C2_1$	$P1_1/SEG_{21}$ pin function select bit	0	SEG_{21}		
		1	$P1_1$		
$C2_0$	$P1_0/SEG_{20}$ pin function select bit	0	SEG_{20}		
		1	$P1_0$		

Note 1: The letter W denotes “writable.”

3.8 LCD Control Register C3

Table 3.8 shows the bit configuration of the LCD Control Register C3.

For write to the register C3, first set a value in the register A and then use the TC3A instruction.

Table 3.8 Bit Configuration of LCD Control Register C3

LCD Control Register C3		When reset: 1111_2		When powered down: State retained	W TC3A
$C3_3$	$P3_3/SEG_{31}$ pin function select bit	0	SEG_{31}		
		1	$P3_3$		
$C3_2$	$P3_2/SEG_{30}$ pin function select bit	0	SEG_{30}		
		1	$P3_2$		
$C3_1$	$P3_1/SEG_{29}$ pin function select bit	0	SEG_{29}		
		1	$P3_1$		
$C3_0$	$P3_0/SEG_{28}$ pin function select bit	0	SEG_{28}		
		1	$P3_0$		

Note 1: The letter W denotes “writable.”

3.9 Timer Control Register W3

Table 3.9 shows the bit configuration of Timer Control Register W3.

For write to the register W3, first set a value in the register A and then use the TW3A instruction.

Furthermore, the TAW3 instruction may be used to transfer the content of register W3 to the register A.

Table 3.9 Bit Configuration of Timer Control Register W3

Timer Control Register W3		When reset: 0000_2		When powered down: State retained	R/W TAW3/TW3A
$W3_3$	Timer 3 count source select bit	0	X_{CIN} input		
		1	Prescaler output (ORCLK) divided by 2		
$W3_2$	Timer 3 control bit	0	Stop (initial state)		
		1	Start		
$W3_1$	Timer 3 count value select bit	$W3_1$	$W3_0$	Count value	
		0	0	Generates underflow every 8,192 counts	
		0	1	Generates underflow every 16,384 counts	
$W3_0$		1	0	Generates underflow every 32,768 counts	
		1	1	Generates underflow every 65,536 counts	

Note 1: The letter R denotes “readable,” and the letter W denotes “writable.”

3.10 Timer Control Register W4

Table 3.10 shows the bit configuration of Timer Control Register W4.

For write to the register W4, first set a value in the register A and then use the TW4A instruction.

Furthermore, the TAW4 instruction may be used to transfer the content of register W4 to the register A.

Table 3.10 Bit Configuration of Timer Control Register W4

Timer Control Register W4		When reset: 0000_2		When powered down: State retained	R/W TAW4/TW4A
$W4_3$	Timer LC control bit	0	Stop (state retained)		
		1	Start		
$W4_2$	Timer LC count source select bit	0	Bit 4 of timer 3 ($T3_4$)		
		1	System clock (STCK)		
$W4_1$	CNTR pin output auto control circuit select bit	0	Deselects CNTR pin output auto control circuit		
		1	Selects CNTR pin output auto control circuit		
$W4_0$	CNTR pin input count edge select bit	0	Falling edge		
		1	Rising edge		

Note 1: The letter R denotes “readable,” and the letter W denotes “writable.”

Note 2: : Unused bits during power-down function setting.

3.11 Key-on Wakeup Control Register K2

Table 3.11 shows the bit configuration of Key-on Wakeup Control Register K2.

For write to the register K2, first set a value in the register A and then use the TK2A instruction.

Furthermore, the TAK2 instruction may be used to transfer the content of register K2 to the register A.

Table 3.11 Bit Configuration of Key-on Wakeup Control Register K2

Key-on Wakeup Control Register K2		When reset: 0000_2	When powered down: State retained	R/W TAK2/TK2A
$K2_2$	Port $P3_2$ and $P3_3$ Note 3 key-on wakeup control bit	0	Disables key-on wakeup	
		1	Enables key-on wakeup	
$K2_2$	Port $P3_0$ and $P3_1$ Note 2 key-on wakeup control bit	0	Disables key-on wakeup	
		1	Enables key-on wakeup	
$K2_1$	INT pin return condition select bit	0	Level returned	
		1	Edge returned	
$K2_0$	INT pin key-on wakeup control bit	0	Disables key-on wakeup	
		1	Enables key-on wakeup	

Note 1: The letter R denotes "readable," and the letter W denotes "writable."

Note 2: To disable the key-on wakeup function of ports $P3_0$ and $P3_1$ ($K2_2$ = 0), set the values of registers $K3_0$ and $K3_1$ to 0.

Note 3: To disable the key-on wakeup function of ports $P3_2$ and $P3_3$ ($K2_3$ = 0), set the values of registers $K3_2$ and $K3_3$ to 0.

Note 4: : Unused bits during power-down function setting.

3.12 Port Output Mode Control Register FR2

Table 3.12 shows the bit configuration of Port Output Mode Control Register FR2.

For write to the register FR2, first set a value in the register A and then use the TFR2A instruction.

Table 3.12 Bit Configuration of Port Output Mode Control Register FR2

Port Output Mode Control Register FR2		When reset: 0000_2	When powered down: State retained	W TFR2A
$FR2_3$	Port $P3_2$ and $P3_3$ output mode select bit	0	N-channel open-drain output	
		1	CMOS output	
$FR2_2$	Port $P3_0$ and $P3_1$ output mode select bit	0	N-channel open-drain output	
		1	CMOS output	
$FR2_1$	Port D_5 output mode select bit	0	N-channel open-drain output	
		1	CMOS output	
$FR2_0$	Port D_4 output mode select bit	0	N-channel open-drain output	
		1	CMOS output	

Note 1: The letter W denotes "writable."

Note 2: : Unused bits during power-down function setting.

3.13 Clock Control Register RG

Table 3.13 shows the bit configuration of the Clock Control Register RG.

For write to the register RG, first set a value in the register A and then use the TRGA instruction.

Table 3.13 Bit Configuration of Clock Control Register RG

Clock Control Register RG		When reset: 000_2	When powered down: State retained	W TRGA
RG_2	Sub-clock ($f(X_{CIN})$) control bit Note 2	0	Enables sub-clock ($f(X_{CIN})$) to oscillate, with ports D_6 and D_7 unselected	
		1	Stops sub-clock ($f(X_{CIN})$) from oscillating, with ports D_6 and D_7 selected	
RG_1	Main clock ($f(X_{IN})$) control bit Note 2	0	Enables main clock ($f(X_{IN})$) to oscillate	
		1	Stops main clock ($f(X_{IN})$) from oscillating	
RG_0	On-chip oscillator (f(RING)) control bit Note 2	0	Enables on-chip oscillator (f(RING)) to oscillate	
		1	Stops on-chip oscillator (f(RING)) from oscillating	

Note 1: The letter W denotes “writable.”

Note 2: Any oscillator circuit that is selected for the system clock cannot be turned off.

4. Application Example for the Power-Down Function

4.1 Time-of-Day Clock Mode

A combined use of a 32.768 kHz crystal resonator for the sub-clock and the POF instruction makes it possible to produce a low power, yet highly accurate time-of-day clock.

Point : Use of the POF instruction helps to reduce the power consumption in the chip.
Specification : An LCD and a 32.768 kHz crystal resonator are used to show the time of day.

Figure 4.1 shows an example of an LCD display panel. Figure 4.2 shows an example of RAM arrangement for LCD display. Figure 4.3 shows an example of a segment arrangement for an LCD display panel.
Figure 4.4 shows a state transition diagram. Figure 4.5 shows an example of how to set the registers for operation in time-of-day clock mode (example 1). Figure 4.6 shows an example of how to set the registers for operation in time-of-day clock mode (example 2).

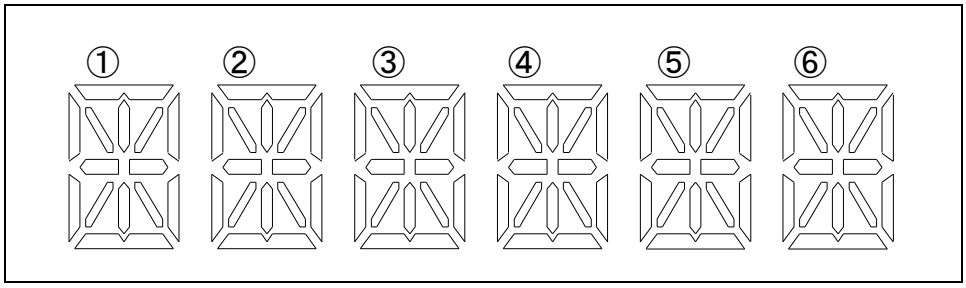

Figure 4.1 Example of an LCD Display Panel

Register Z	1															
Register X	0				1				2				3			
bit / Register Y	3	2	1	0	3	2	1	0	3	2	1	0	3	2	1	0
8	SEG_0	SEG_0	SEG_0	SEG_0	SEG_8	SEG_8	SEG_8	SEG_8	SEG_{16}	SEG_{16}	SEG_{16}	SEG_{16}	SEG_{24}	SEG_{24}	SEG_{24}	SEG_{24}
9	SEG_1	SEG_1	SEG_1	SEG_1	SEG_9	SEG_9	SEG_9	SEG_9	SEG_{17}	SEG_{17}	SEG_{17}	SEG_{17}	SEG_{25}	SEG_{25}	SEG_{25}	SEG_{25}
10	SEG_2	SEG_2	SEG_2	SEG_2	SEG_{10}	SEG_{10}	SEG_{10}	SEG_{10}	SEG_{18}	SEG_{18}	SEG_{18}	SEG_{18}	SEG_{26}	SEG_{26}	SEG_{26}	SEG_{26}
11	SEG_3	SEG_3	SEG_3	SEG_3	SEG_{11}	SEG_{11}	SEG_{11}	SEG_{11}	SEG_{19}	SEG_{19}	SEG_{19}	SEG_{19}	SEG_{27}	SEG_{27}	SEG_{27}	SEG_{27}
12	SEG_4	SEG_4	SEG_4	SEG_4	SEG_{12}	SEG_{12}	SEG_{12}	SEG_{12}	SEG_{20}	SEG_{20}	SEG_{20}	SEG_{20}	SEG_{28}	SEG_{28}	SEG_{28}	SEG_{28}
13	SEG_5	SEG_5	SEG_5	SEG_5	SEG_{13}	SEG_{13}	SEG_{13}	SEG_{13}	SEG_{21}	SEG_{21}	SEG_{21}	SEG_{21}	SEG_{29}	SEG_{29}	SEG_{29}	SEG_{29}
14	SEG_6	SEG_6	SEG_6	SEG_6	SEG_{14}	SEG_{14}	SEG_{14}	SEG_{14}	SEG_{22}	SEG_{22}	SEG_{22}	SEG_{22}	SEG_{30}	SEG_{30}	SEG_{30}	SEG_{30}
15	SEG_7	SEG_7	SEG_7	SEG_7	SEG_{15}	SEG_{15}	SEG_{15}	SEG_{15}	SEG_{23}	SEG_{23}	SEG_{23}	SEG_{23}	SEG_{31}	SEG_{31}	SEG_{31}	SEG_{31}
COM	COM_3	COM_2	COM_1	COM_0	COM_3	COM_2	COM_1	COM_0	COM_3	COM_2	COM_1	COM_0	COM_3	COM_2	COM_1	COM_0

Figure 4.2 Example of RAM Arrangement for LCD Display

Register Z	1											
Register X	0				1				2			
bit / Register Y	3	2	1	0	3	2	1	0	3	2	1	0
8	①-d	①-c	①-b	①-a	③-d	③-c	③-b	③-a	⑤-d	⑤-c	⑤-b	⑤-a
9	①-h	①-g	①-f	①-e	③-h	③-g	③-f	③-e	⑤-h	⑤-g	⑤-f	⑤-e
10	①-k	①-j		①-i	③-k	③-j		③-i	⑤-k	⑤-j		⑤-i
11	①-n	①-l		①-m	③-n	③-l		③-m	⑤-n	⑤-l		⑤-m
12	②-d	②-c	②-b	②-a	④-d	④-c	④-b	④-a	⑥-d	⑥-c	⑥-b	⑥-a
13	②-h	②-g	②-f	②-e	④-h	④-g	④-f	④-e	⑥-h	⑥-g	⑥-f	⑥-e
14	②-k	②-j		②-i	④-k	④-j		④-i	⑥-k	⑥-j		⑥-i
15	②-n	②-l		②-m	④-n	④-l		④-m	⑥-n	⑥-l		⑥-m
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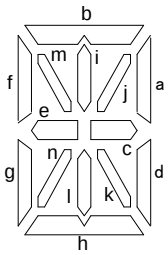


Figure 4.3 Example of a Segment Arrangement for an LCD Display Panel

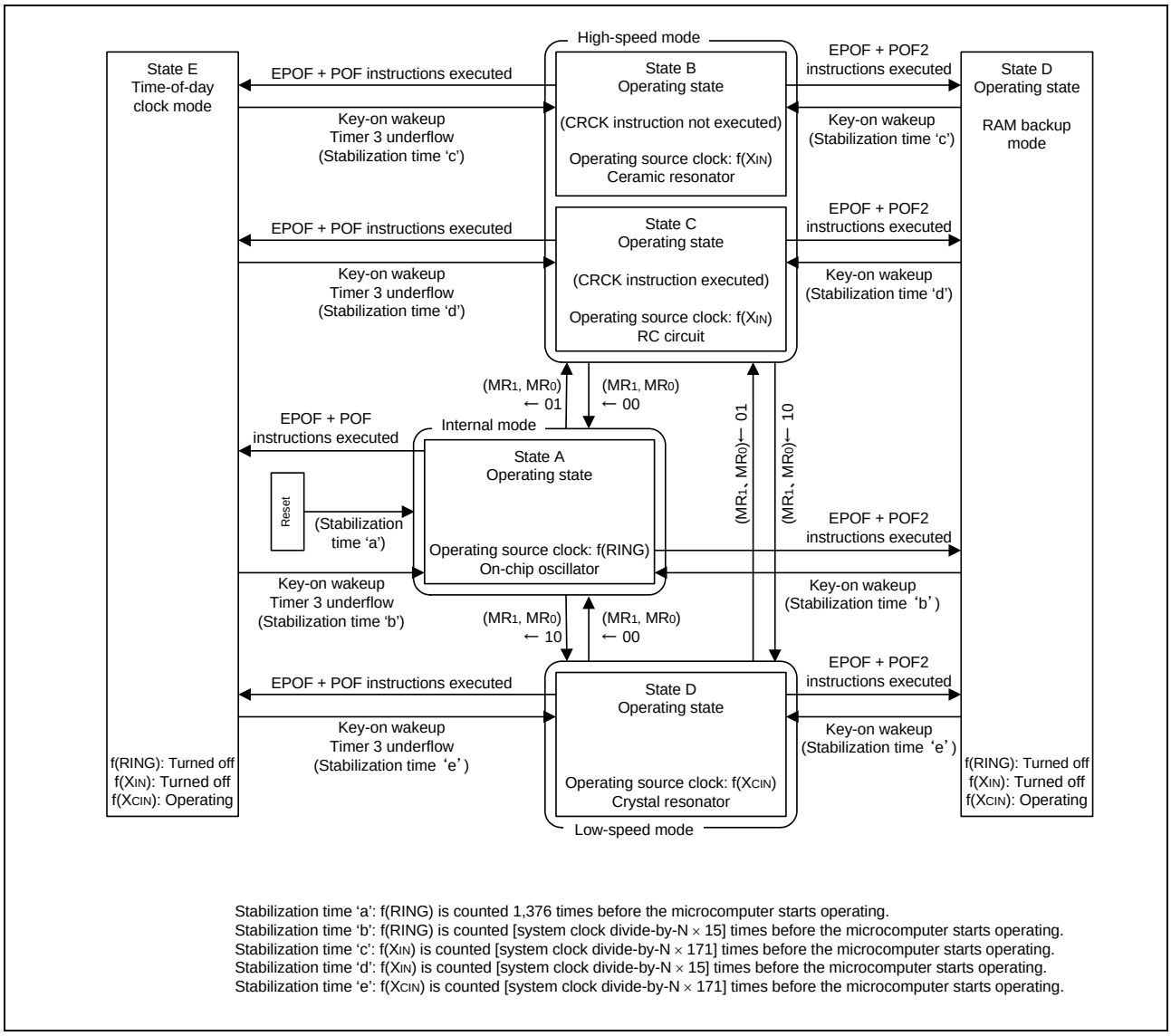
4.2 RAM Backup Mode

Use of the POF2 instruction permits clock oscillations to be stopped while retaining the RAM and reset circuit functions and states intact, making it possible to reduce the power consumption in the chip without a possibility of losing RAM data.

Point : Use of the POF2 instruction helps to reduce the power consumption in the chip.

Specification : The microcomputer is waked up with the press of a switch (key-on wakeup), and the number of wakeup times is displayed up to 9 times on an LCD. When 9 times is exceeded, the count recycles to 0 and starts over. This application uses the same LCD panel that is used in Section 4.1, "Time-of-Day Clock Mode."

Figure 4.7 shows an example of how to set the registers for RAM backup mode (example 1). Figure 4.8 shows an example of how to set the registers for RAM backup mode (example 2). Figure 4.9 shows an example of how to set the registers for RAM backup mode (example 3).



Stabilization time 'a': f(RING) is counted 1,376 times before the microcomputer starts operating.
Stabilization time 'b': f(RING) is counted [system clock divide-by-N × 15] times before the microcomputer starts operating.
Stabilization time 'c': f(XIN) is counted [system clock divide-by-N × 171] times before the microcomputer starts operating.
Stabilization time 'd': f(XIN) is counted [system clock divide-by-N × 15] times before the microcomputer starts operating.
Stabilization time 'e': f(XCIN) is counted [system clock divide-by-N × 171] times before the microcomputer starts operating.

Figure 4.4 State Transition Diagram

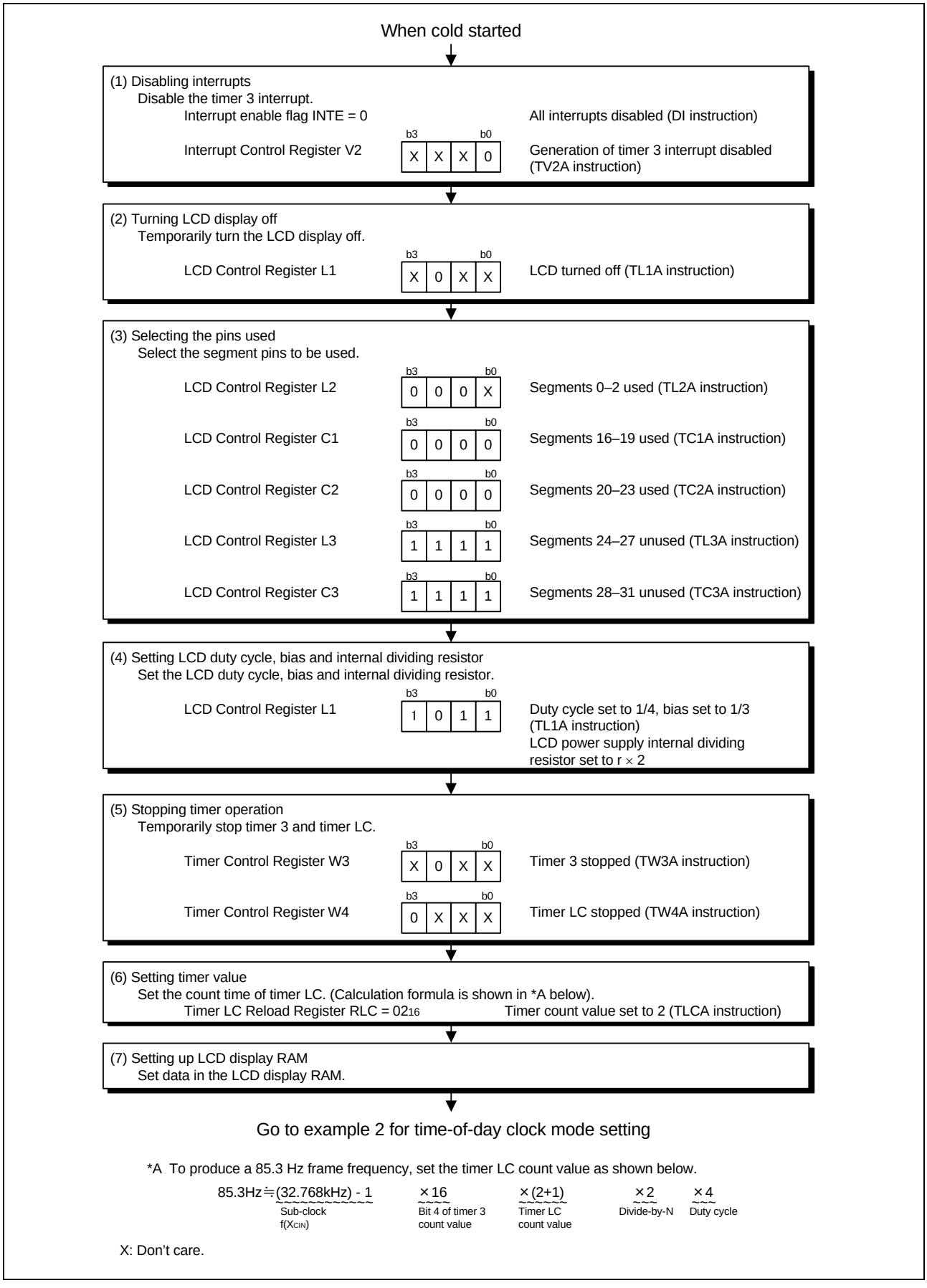


Figure 4.5 Example 1 for Time-of-Day Clock Mode Setting

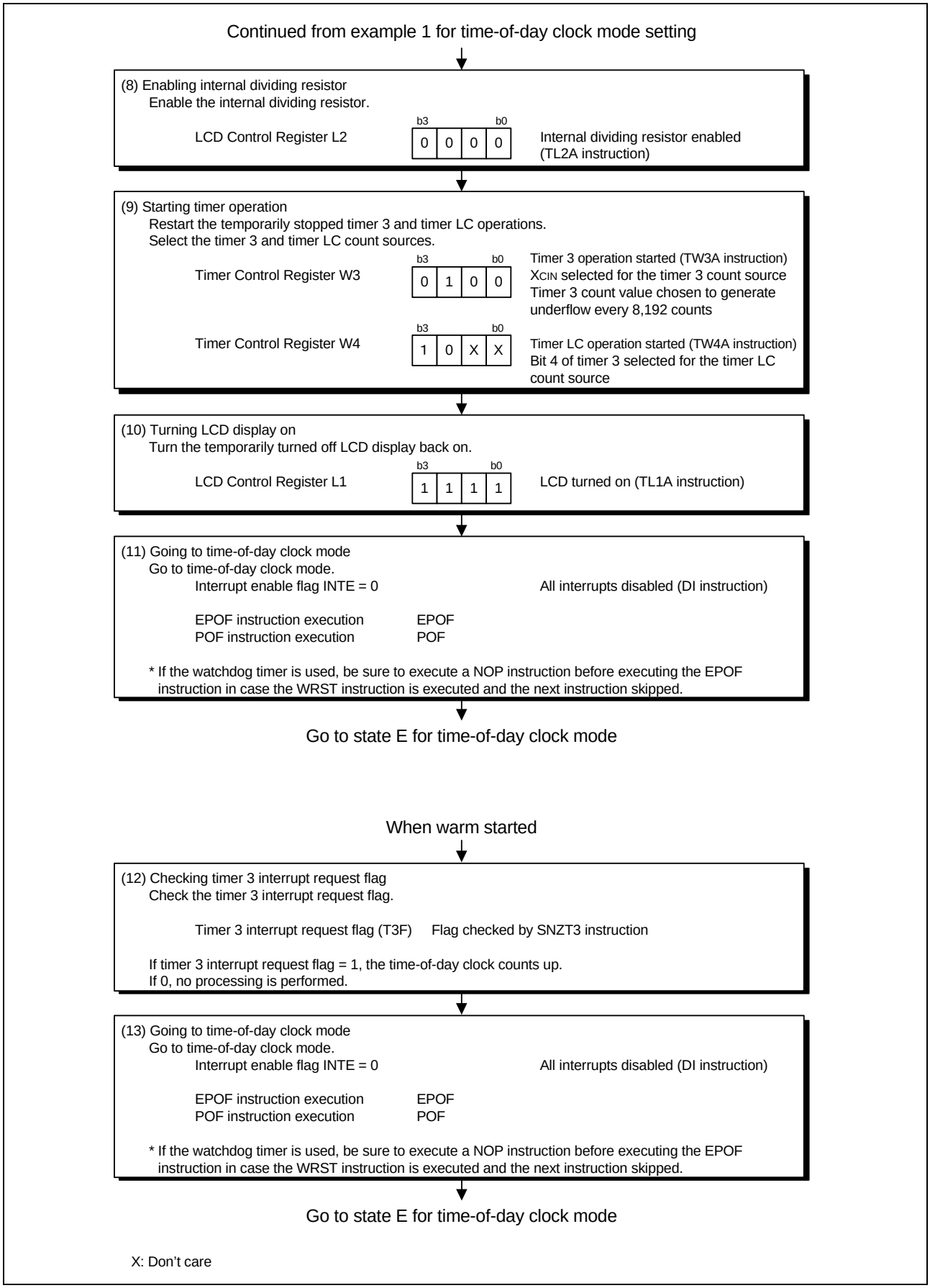


Figure 4.6 Example 2 for Time-of-Day Clock Mode Setting

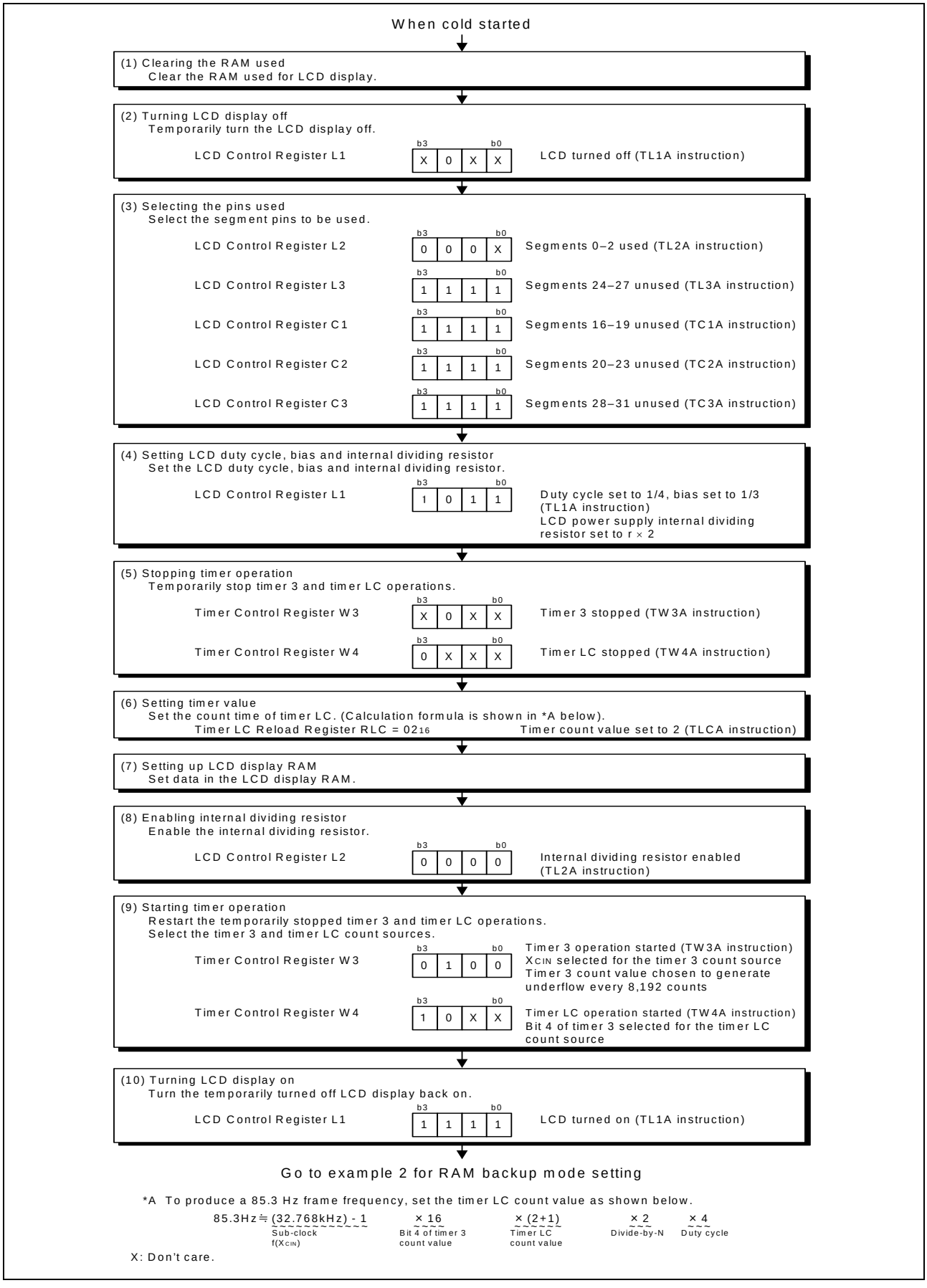


Figure 4.7 Example 1 for RAM Backup Mode Setting

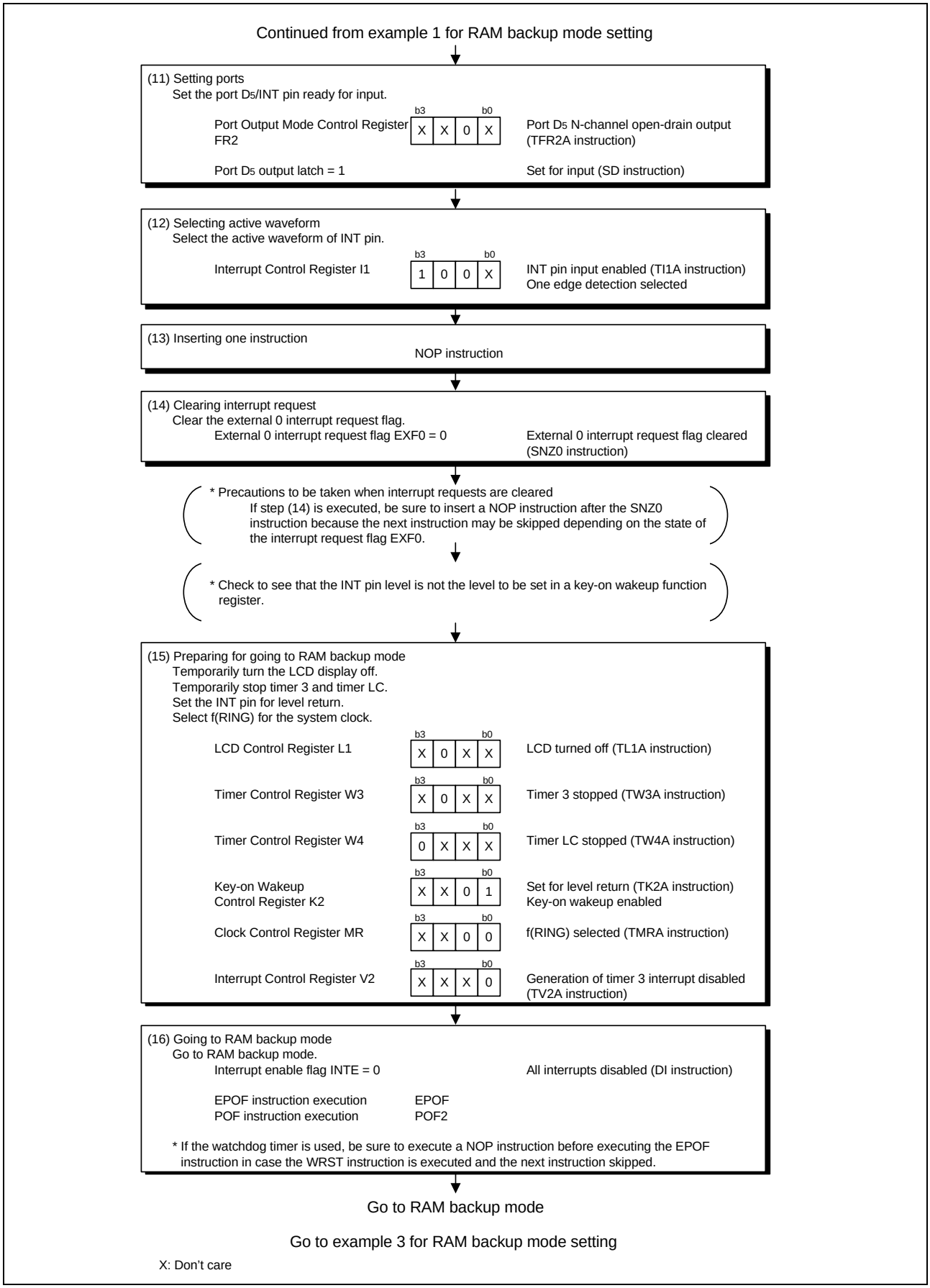


Figure 4.8 Example 2 for RAM Backup Mode Setting

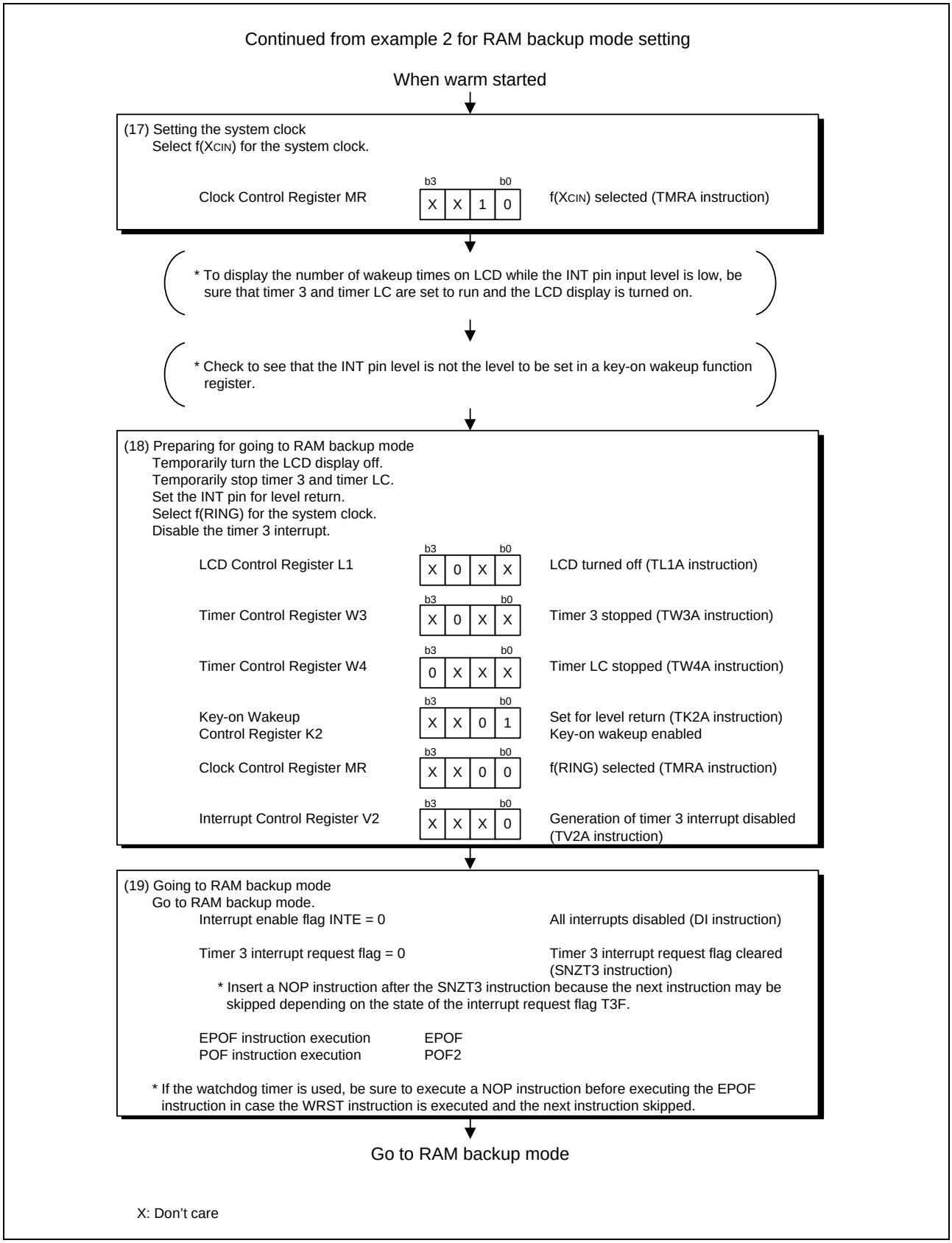


Figure 4.9 Example 3 for RAM Backup Mode Setting

5. Sample Programs

Sample programs are available from the Renesas Technology Web site. To download one, click the screen menu "Application Note" on the left side of 4559 group Web page.

6. Reference Documents

Data sheet
4559 Group Data sheet

The latest version is available from the Renesas Technology Web site.

7. Renesas Web Site and Where to Contact

Renesas Technology Web site:
http://japan.renesas.com/

Where to contact:
http://japan.renesas.com/inquiry
csc@renesas.com

Revision history	4559 Group Power-Down Function Application Note

Rev.	Date	Description	
		Page	Points
1.00	2006.11.01	–	First edition issued

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