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April 1st, 2010
Renesas Electronics Corporation

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4509 Group

Serial Interface

1. Abstract

The following article introduces application examples and setting examples of the serial interface of 4509 Group.

2. Introduction

The explanation of this issue is applied to the following condition:

- Microcomputer: 4509 Group
- Oscillation Frequency: 4 MHz
- System Clock: Through Mode (Frequency not divided)

Due to the bit location for the control register, a bit with no function may be operated in some cases. Values can be optionally set on those bits.

3. Relevant Register

3.1 Serial Interface Register SI

Register SI is the 8-bit data transferring serial-parallel conversion Register.

Writing to register SI can be accomplished by TSIAB instruction after setting values to the lower four bits of register A and the upper 4 bits of register B.

The contents of the lower four bits of register SI can be transferred to register A by TABSI instruction. Similarly, the contents of the upper four bits of register SI can be transferred to register B by TABSI instruction.

3.2 Serial Interface Transmit/Receive Completion Flag SIOF

Once the serial data transmission/reception is completed, flag SIOF turns to “1”.

The condition of flag SIOF can be confirmed by SNZSI instruction when Serial interface interrupt enable bit is set to the disable mode.

3.3 Interrupt Control Register V2

Table 3.1 shows the bit configuration for Interrupt control register V2.

Writing to register V2 can be performed by TV2A instruction after setting values to register A.

The contents of register V2 can be transferred to register A by TAV2 instruction.

Table 3.1 Bit Configuration for Interrupt Control Register V2

Interrupt control register V2		at reset: 0000 ₂	at RAM back-up: 0000 ₂	R/W TAV2/TV2A
V23	Serial interface interrupt enable bit	0	Interrupt disabled (SNZSI instruction is valid)	
		1	Interrupt enabled (SNZSI instruction is invalid)	
V22	A/D interrupt enable bit	0	Interrupt disabled (SNZAD instruction is valid)	
		1	Interrupt enablede (SNZAD instruction is invalid)	
V21	Not used	0	This bit has no function but read/write is enabled	
		1		
V20	Not used	0	This bit has no function but read/write is enabled	
		1		

Note 1: “R” represents read enabled, and “W” represents write enabled.

Note 2: Unused bits while setting the serial interface.

3.4 Serial Interface Control Register J1

Table 3.2 shows the bit configuration for Serial interface control register J1.

Writing to register J1 can be achieved by TJ1A instruction after setting values to register A.

The content of register J1 can be transferred to register A by TAJ1 instruction.

Table 3.2 Bit Configuration for Serial Interface Control Register J1.

Serial interface control register J1		at reset: 00002		at RAM back-up: Hold	R/W TAJ1/TJ1A
J13	Serial interface synchronous clock selection bits	J13	J12	Synchronous Clock	
		0	0	Instruction clock (INSTCK) divided by 8	
		0	1	Instruction clock (INSTCK) divided by 4	
		1	0	Instruction clock (INSTCK) divided by 2	
J12		1	1	External clock (SCK input)	
		J11	J10	Port Function	
J11	Serial interface port function selection bits	0	0	P00, P01, P02 selected / SIN, SOUT, SCK not selected	
		0	1	P00, SOUT, SCK selected / SIN, P01, P02 not selected	
J10		1	0	SIN, P01, SCK selected / P00, SOUT, P02 not selected	
		1	1	SIN, SOUT, SCK selected / P00, P01, P02 not selected	

Note1: "R" represents read enabled, and "W" represents write enabled.

4. Operation Procedure

Figure 4.1 depicts an example of the serial interface connection, whereas Figure 4.2 illustrates the transferring timing of the serial interface. For actual cabling, pull up each signal line via a resistor.

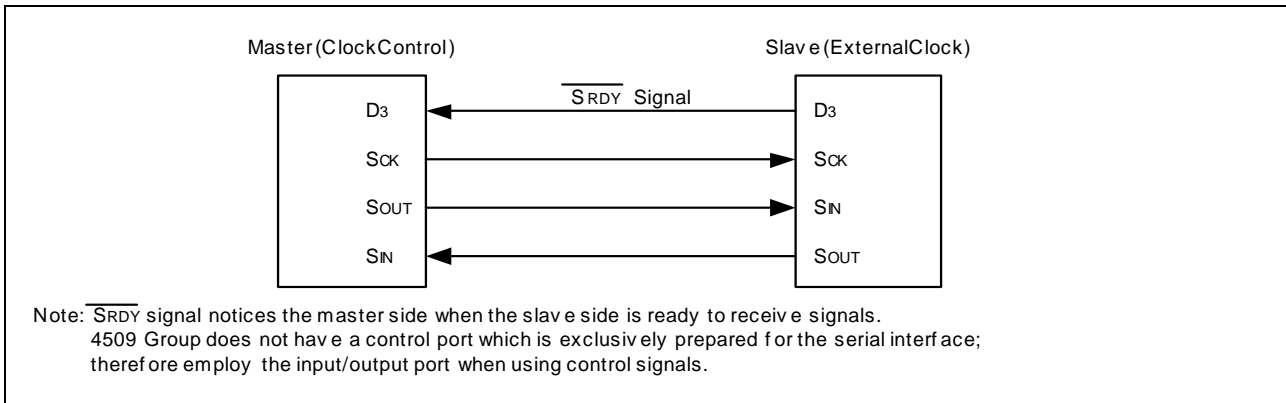


Figure 4.1 Serial Interface Connection Example

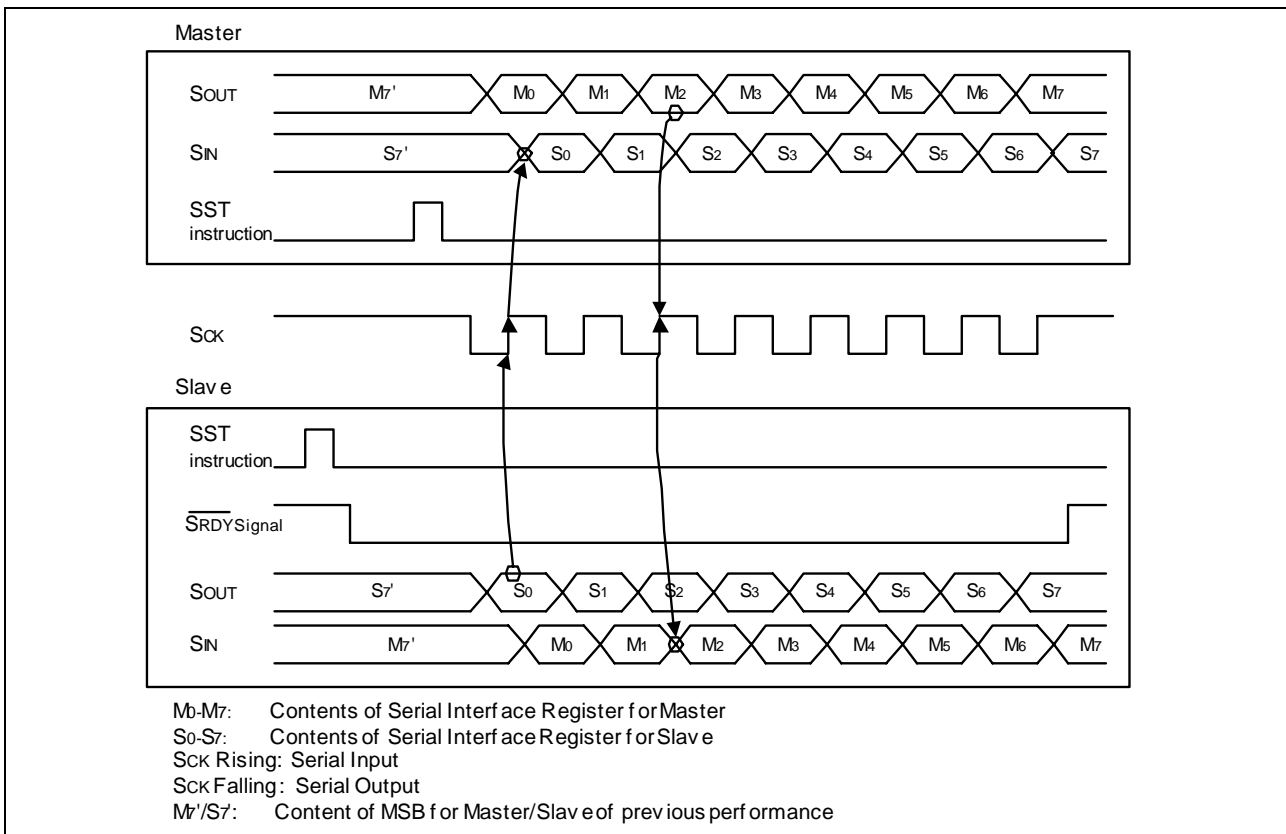


Figure 4.2 Serial Interface Transfer Timing

5. Application Example for Serial Interface

5.1 Serial Interface

Overview: Communicates with the peripheral IC

Specification: See Figure 4.1 Serial Interface Connection Example.

Figure 5.2 explains the setting procedure when using NO Serial Interface Interrupt for Master while Figure 5.2 shows the setting procedure using Serial Interface Interrupt for Slave.

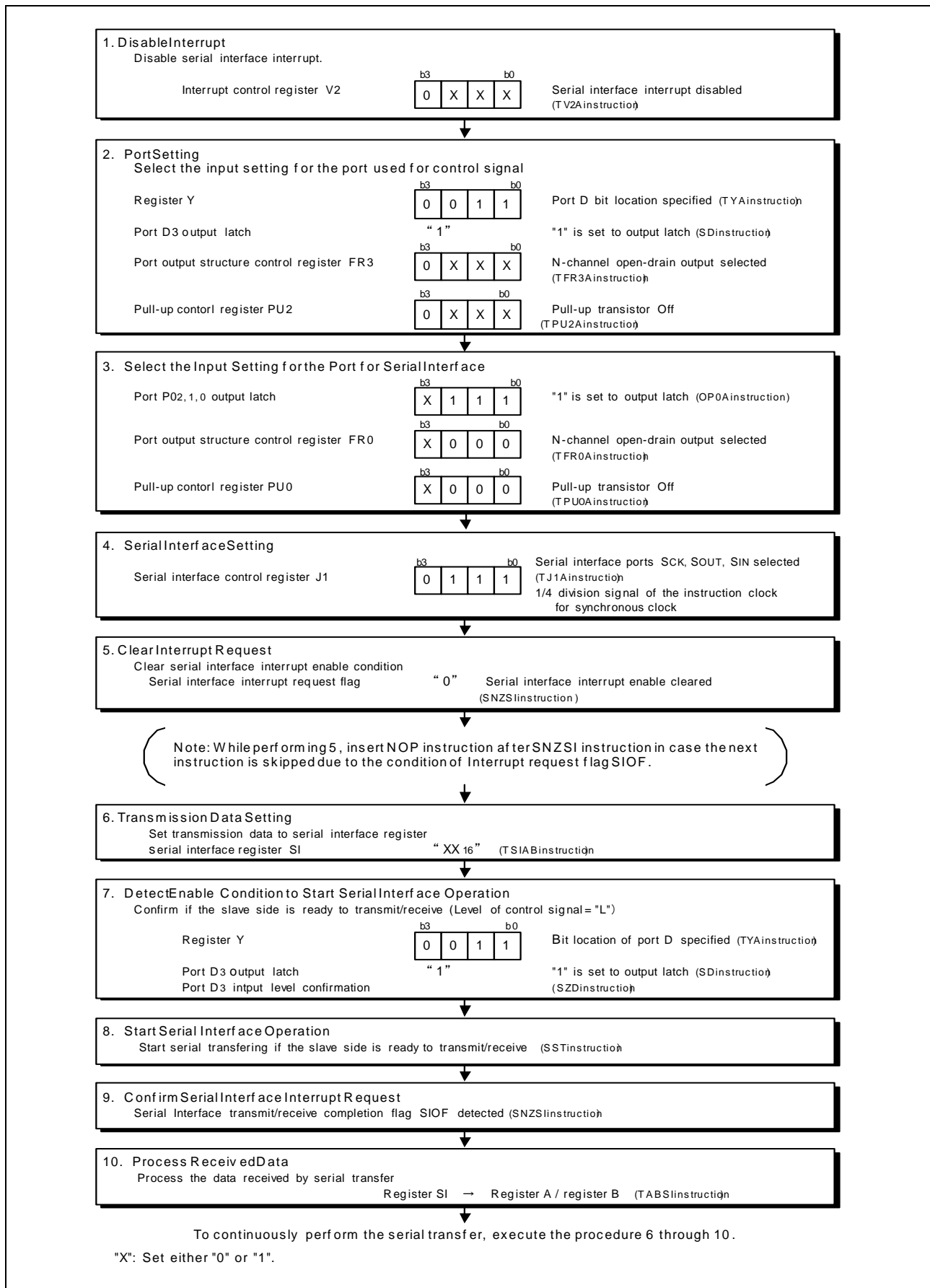


Figure 5.2 Setting Procedure with NO Serial Interface Interrupt on Master

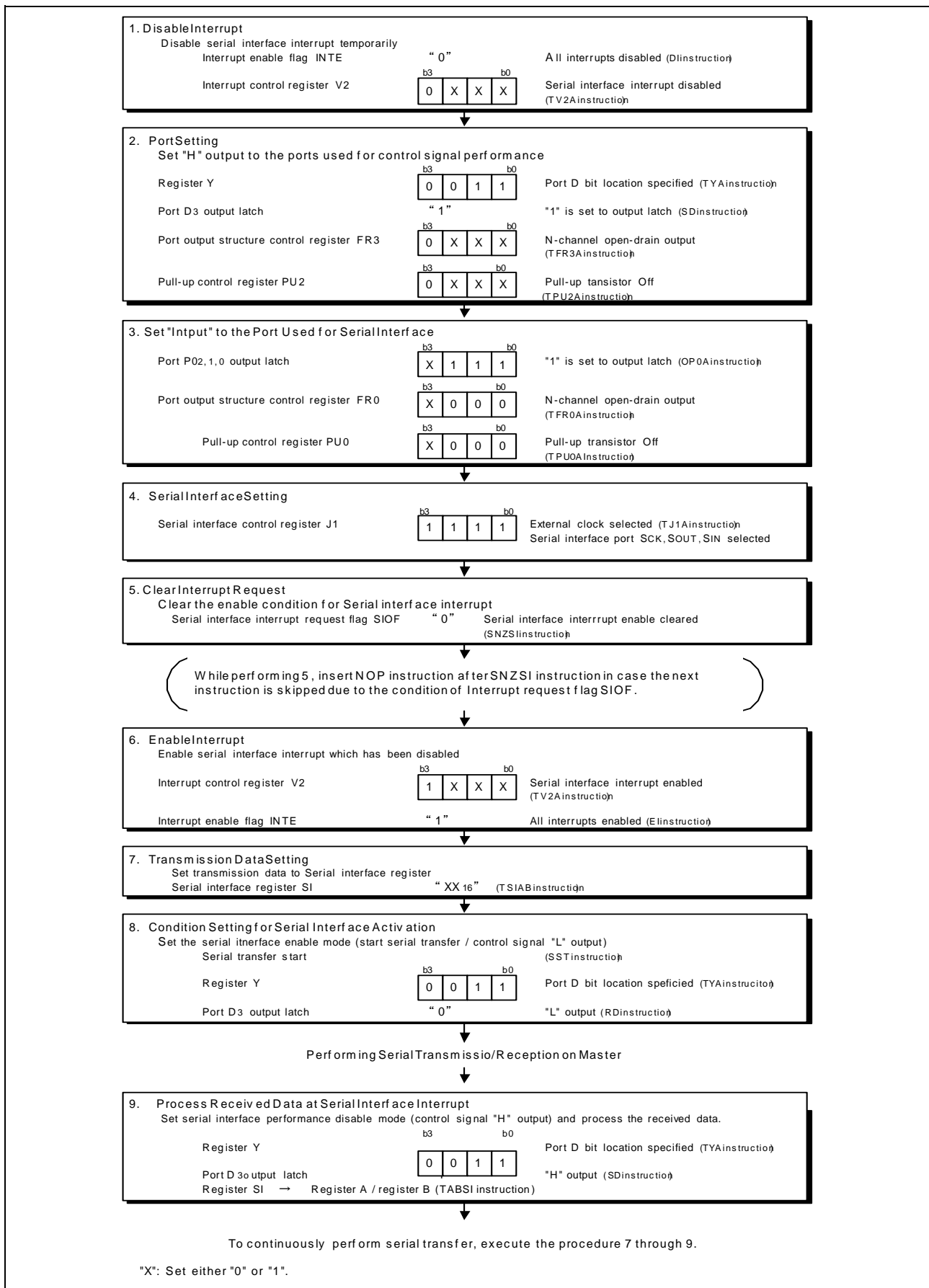


Figure 5.2 Setting Procedure with Serial Interface Interrupt on Slave

6. Reference Software Programs

Reference software programs are available on Renesas Technology Corporation Website.
To obtain the program, click “Application Note” on the left side of the 4509 Group page.

7. Reference Documents

Datasheet
4509 Group Datasheet

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Revision History	4509 GroupSerial Interface Application Note
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Rev.	Date	Description	
		Page	Summary
1.00	July 01, 2006	—	First Edition Issued

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