APPLICATION NOTE:
AN-407

1+1 HITLESS PROTECTION SWITCHING WITHOUT RELAYS FOR SHORT HAUL T1/E1/J1 USING IDT82V2081, IDT82V2082, IDT82V2084 AND IDT82V2088

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1. INTRODUCTION

In today's telecommunication systems, ensuring no traffic loss is becoming increasingly important. More and more, people are relying on internet to conduct financial transactions, make telephone calls and perform video conferencing. Loss of data could have a devastating effect including losing or delaying of a critical financial transaction, hearing annoying flickering noises on the telephone lines, or viewing lousy video clips.

To combat these problems, redundancy protection must be built into the systems carrying this traffic. Although there are many types of redundancy protection schemes, linear 1+1 hardware protection implementation with IDT82V2081/2/4/8 universal line interface units (ULIU) is the subject of this application note. As will be shown in this document, the ULIU enables system design to achieve high reliability, low switching latency and ease of service.

The forgoing sections will discuss the implementation of T1/E1/J1 1+1 relay-less hitless protection switching (HPS) implementation using the ULIU series from IDT. Section 2 will discuss how the ULIU is used in such applications begins by explaining the concept of 1+1 relay-less hitless protection. Then it describes implementation of redundancy protection using IDT82V2081/2/4/8. After describing the receive line interface design, it will detail the transmit side. For both the transmit and receive line interface, internal and external line impedance matching will be discussed in detail. Section 3 will briefly touch on the principle of hot-switch and hot-swap. Section 4 provides some general design guidelines. Following the discussion of test results using the IDT82V2088 evaluation board in section 5 is the conclusion of the report described in section 6.

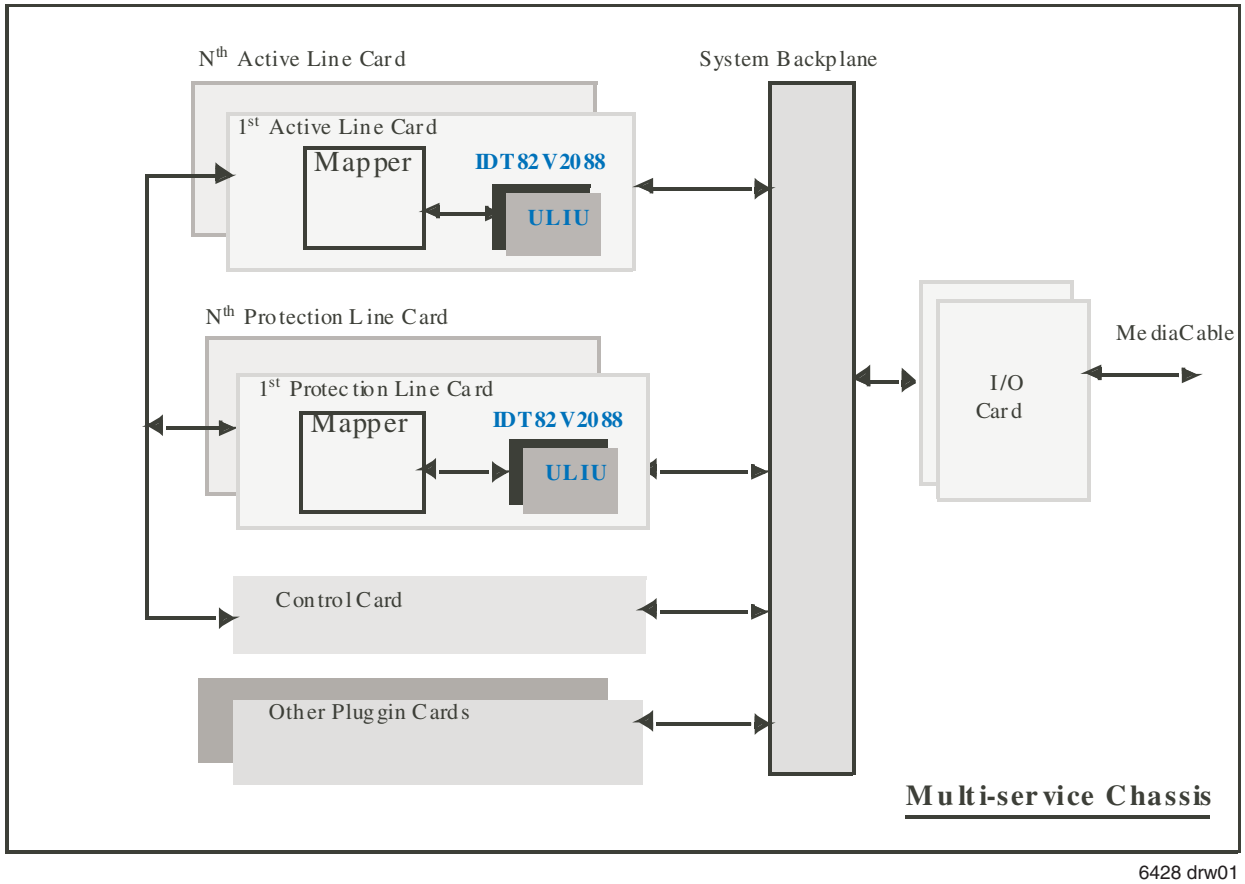

Figure 1. System Application Diagram

2. IDT82V2081/2/4/8 1+1 RELAY-LESS HITLESS PROTECTION SWITCHING

2.1. WHAT IS T1/E1/J1 1+1 RELAY-LESS HITLESS PROTECTION SWITCHING?

T1/E1/J1 1+1 relay-less hitless protection switch or relay-less HPS is a means to provide 100% linear redundancy for T1/E1/J1. In the T1/E1/J1 1+1 redundancy scheme, there are two identical cards: a primary and secondary or protection card. The primary card is the active and secondary card is always in hot standby, and are shared with the same line interface. If the primary card fails, the traffic is switched to the secondary card.

In the older generation of T1/E1/J1 line cards, the primary and secondary cards share the same line by use of multiple mechanical relays. When the primary card fails, the switching from the primary to the secondary card relies on mechanical relays. Mechanical relays are not only costly but have a lot of drawback as well. First, the relays require drivers to switch them. This implies bigger bill of materials and results higher system cost as well as potentially more reliability issues from the relays and drivers. Secondly, the relays are big and take up a lot of room on PCB. Depending on the types of relay, each could take up to an area of 10mm^2. This is almost the size of the IDT82V2088 (octal ULIU) in BGA package. As traffic volume grew, more channels or line cards are required to handle heavier traffic load, the mechanical relays result in bigger and more costly boxes. Finally, mechanical relays have higher switching latency. Depending on the relays, it could take up to tens of milliseconds to switch the relays. During this time, there are enough bits error to jeopardize mission critical traffic.

In the relay-less hitless protection switching T1/E1/J1 line cards, switching traffic from the primary to backup card is accomplished by the monolithic T1/E1/J1 line interface unit. Relays are eliminated from the system resulting in fewer components, higher reliability, better performing and cost effective system. IDT82V2081/2/4/8 is the latest T1/E1/J1 silicon from IDT to enable low latency relay-less redundancy applications.

2.2. IDT82V2081/2/4/8 UNIVERSAL LINE INTERFACE UNITS

IDT82V2081/2/4/8 T1/E1/J1 universal line interface unit products consist of IDT82V2081 (single channel), IDT82V2082 (dual), IDT82V2084 (quad), and IDT82V2088 (octal). In addition to extensive functionality, they also have fast high-impedance output line drivers, arbitrary waveform generator at the transmit output, and internal/external line impedance matching capability. The transmit high impedance driver enables 1+1 redundancy applications without extra mechanical relays and still achieve excellent analog performance. Likewise, the receiver input has high-impedance and enables parallel connection with the backup receiver input without effecting the receive traffic.

Figure 1 illustrates the implementation of IDT82V2081/2/4/8 in 1+1 relay-less hitless protection switching. It shows a typical multi-service chassis populated with T1/E1/J1 line cards. There are 2xN line cards, control card, backplane connector and I/O cards as detailed in following:

- 1st to Nth active cards – These are T1/E1/J1 primary cards populated with multiple IDT82V2088.
- 1st to Nth protection cards – These are T1/E1/J1 secondary cards populated with multiple IDT82V2088 and are in hot standby. Each line card has a backup line card and connects to the same traces to the backplane.
- I/O cards – These cards consist of transformer and metallic line protection devices, plugged into the backplane and are shared among the primary and secondary cards.
- Control card – If one of the active cards failed, the control card detects it, high-impedances the active card and turns on the backup card. The IDT82V2088 has fast high-impedance output driver to ensure hitless switching during hot-switch.
- Other Plugging Cards – These cards represent other functional cards specified by the multi-service chassis.

2.3. RECEIVE LINE SCHEMATIC

Figure 2 describes the receive line interface circuit for the IDT82V2088 in a 1+1 HPS implementation. The example shown in this figure consists of the primary, secondary and interface card all connecting to the same backplane. Only one transformer required to be shared between the working and redundant card. The recommended AC coupling capacitors are either 0.22µF or 0.47µF. The termination resistor, Rr is recommended in Table 1. The 470Ω resistors are recommended for DC current isolation. Furthermore, to meet some of the surge requirements of GR1089, a primary protection circuits with a transient voltage suppressor and secondary surge protection provided by the diodes is recommended. Table 1 provides the component values and manufacturers tested by IDT to meet the above requirements.

2.3.1. INTERNAL OR EXTERNAL LINE IMPEDANCE?

IDT82V2081/2/4/8 provides internal and external line impedance matching capability. The device integrates active components to match T1/E1/J1 and high impedance by programming R_TERM[2:0] bits. In HPS, it is recommended to use the external impedance mode of the device, where the receive input impedance is ~20kΩ. The high input impedance insures no signal degradation in hot-switch or hot-swap. With the external impedance mode, a single 120Ω resistor is sufficient to satisfy 100, 110 and 120Ω requirements for T1/E1/J1 twisted pairs applications; for coax application, the recommended termination resistor is 75Ω Although the internal impedance is an option for the receive input, it is not recommended for HPS. The internal impedance could potentially alter the input signal and result in bit error.

TABLE 1—RX COMPONENTS

COMPONENTS	VALUES	
R	470 Ω	
C	0.22µF or 0.47µF	
SD	TECCOR P0640SC	
D1, D2, D3, D4	International Rectifier, IR10BQ040	
T1	1:1 turn ratio. 0553-0013-AC (Belfuse), T1108 (Pulse)	
Rr	T1/E1/J1	Coax
	120Ω	75

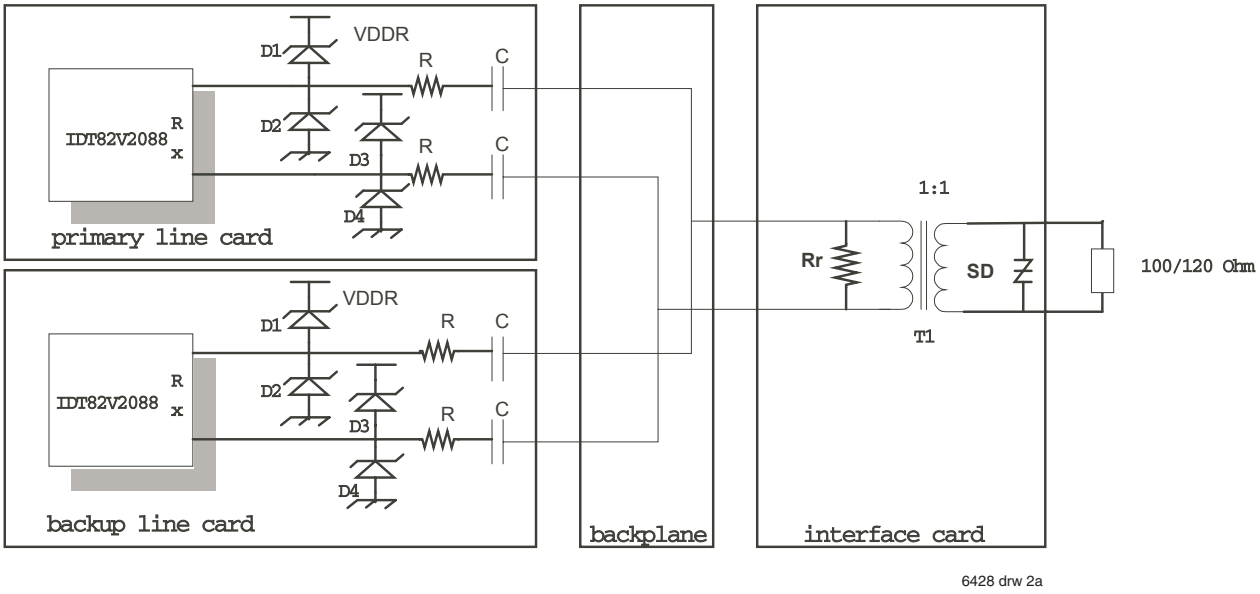

Figure 2. Receive Line Interface Schematic

2.4. TRANSMIT LINE INTERFACE SCHEMATIC

Figure 3 delineates the transmit line interface circuit for IDT82V2088 in 1+1 HPS implementation. Primary, secondary and interface cards are connected to the same backplane. Only a single 1:2 turn ratio transformer and a single Cp capacitor, is shared between the working and protect cards. The Cp value effects the pulse shape and return loss. The value can be adjusted to match different load conditions. The DC decoupling caps with a value of 0.47µF are recommended to prevent DC bias differences between cards. Table 2 provides the list of component values and manufacturers tested by IDT for above requirements.

2.4.1 INTERNAL OR EXTERNAL LINE IMPEDANCE?

Internal line impedance matching is recommended as it requires fewest components. With the internal impedance matching, the primary card is programmed to active or normal mode, while secondary card is programmed to high impedance mode.

TABLE 2—TRANSMIT CIRCUIT COMPONENTS

COMPONENTS	VALUES
C	0.47 µF
Cp	560pF, 50v (Adjustable from 0-560pF)
SD	TECCOR P0640SC
T1	1:2 turn ratio. 0553-0013-HC (Belfuse), T1108 (Pulse)
D1, D2, D3, D4	International Rectifier, IR10BQ040

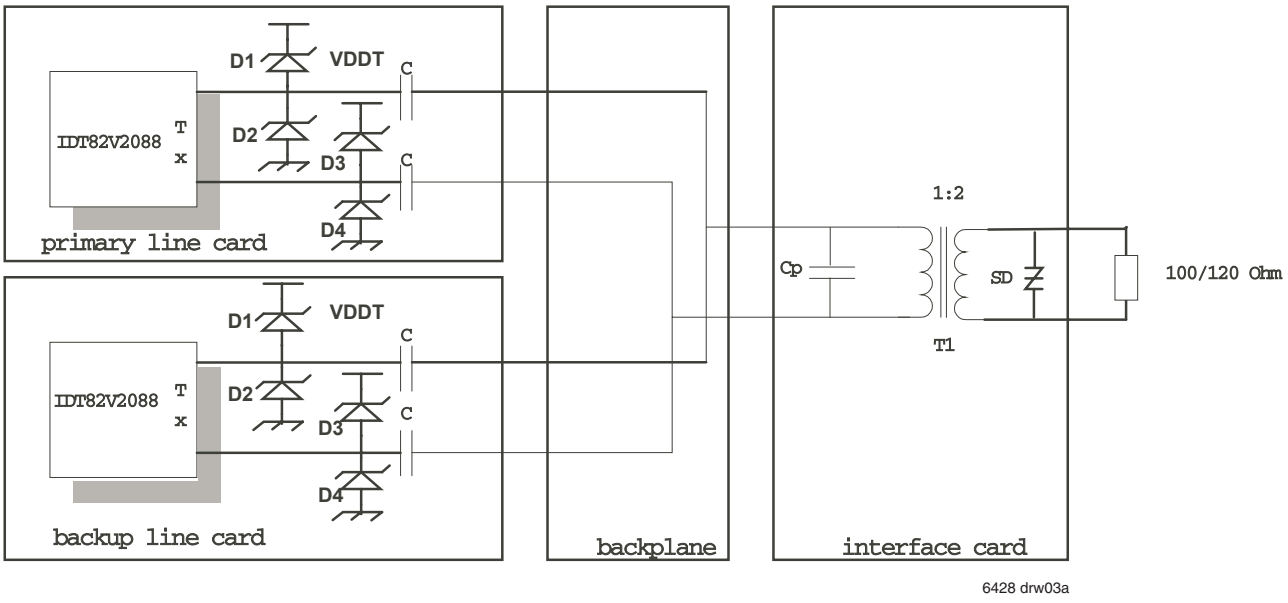

Figure 3. Transmit Line Interface Schematic

3. HOT-SWITCH AND HOT-SWAP PRINCIPLE

3.1. WHAT IS HOT-SWITCH?

Hot-switch refers to the switching from an active card to a backup card or vice versa. The critical parameter in switching is the latency. GR253 and ITU-T G.783 required the total latency of less than 60ms. IDT82V2081/2/4/8 incurs a latency no more than 10µs during hot-switch. This gives the ULIU over 100 times the required margin for system implementation.

The IDT82V2081/2/4/8 provides both hardware and software modes for hot-switch: In hardware mode, switching the THZ high and low will put the device into high-impedance and active mode, respectively. In software mode, writing a 1 and 0 to the THZ bit in the TCF1 register will put the output driver to high-impedance and active mode respectively. Lab tests show that there is less than 1 bit of error for every 20 hot-switch using the THZ pin.

3.2 WHAT IS HOT-SWAP?

Hot-swap refers to the plugging and unplugging of line cards in a powered backplane. When a card fails, a new replacement card is installed. The failed card must be removed and a new card plugged in while the system is still running. IDT82V2081/2/4/8 provides high transmit and receive impedance to enable hot-swapping where still maintaining excellent transmit output pulse templates and producing no bit error. It should be noted that to insure good system performance, the pins plugged into the backplane should be staggered as follows:

- Ground pins are first to make contact (longer pin)
- VCC pins are next to make contact
- TTIP/RING, RTIP/RING and I/O pins are last to make contact

4. GENERAL DESIGN GUIDELINES

- Surge immunity protection should be placed close to the connector, where the source of disturbance is.
- Power supply decoupling caps should be placed as close to the power and ground pins of the chip as possible.
- Simple inductor or beads and capacitors filter is recommended for power supply switching noise isolation.
- Route digital signals away from the analog signal to avoid them from crossing each other.
- Avoid power and ground planes near high voltage area as noise from high voltage area may couple noise to the power/ground planes. Recommend to void power and ground planes underneath the RJ48 or BNC connectors
- EMI filtering should currently be sufficient. However, if additional EMI requirement has to be met, common mode choke may be added near the connectors.
- Avoid long trace length as they may reduce the transmit output amplitude. For T1/E1/J1 type of signal, less than 30cm is recommended.

TABLE 3—HPS PERFORMANCE TEST RESULT

#	TEST	RESULT	DESCRIPTION
1	T1/E1 Power failure test	0 bit error/ 48 hours	2^23-1 PRBS, ESF for T1 2^23-1 PRBS, PCM32CRC for E1 Primary card transmits live traffic Secondary powered on/off Duration = 48 hr Test configuration: Test setup #1
2	T1/E1 Hot-switch Stress Test	< 1 error for every 20 switches	2^23-1PRBS, ESF for T1 2^23-1 PRBS, PCM32CRC for E1 Switch data between primary and secondary card Duration = 8 hr Test configuration: Test setup #2
3	T1/E1 power supply	0 bit error/ 8 hours	2^23-1 PRBS, ESF for T1 2^23-1 PRBS, PCM32CRC for E1 Primary card transmit live traffic Secondary card's VCC tied to GND Duration = 48 hr Test configuration: Test setup #3

5. TEST RESULT

5.1 SUMMARY OF IDT82V2088 HPS TEST RESULT

Table 3 summarizes the test result conducted by IDT Telecom Laboratory. The 1+1 Relay-less HPS was tested using modified IDT82V2088 octal ULIU evaluation board. In addition to bit error rate, pulse templates, and return loss tests, additional tests to mimic hot-switch and hot-swap conditions are also performed.

5.2 T1/E1 TRANSMIT PULSE MASKS

Figure 4a – 5b showed the captured T1 and E1 pulse masks meeting T1.102 and G.703 templates. Although only 0ft waveforms are shown, the IDT82V2081/2/4/8 passed all pulse templates LBO. User can verify the other LBO by setting bits PULSE[3:0] of register TCF1

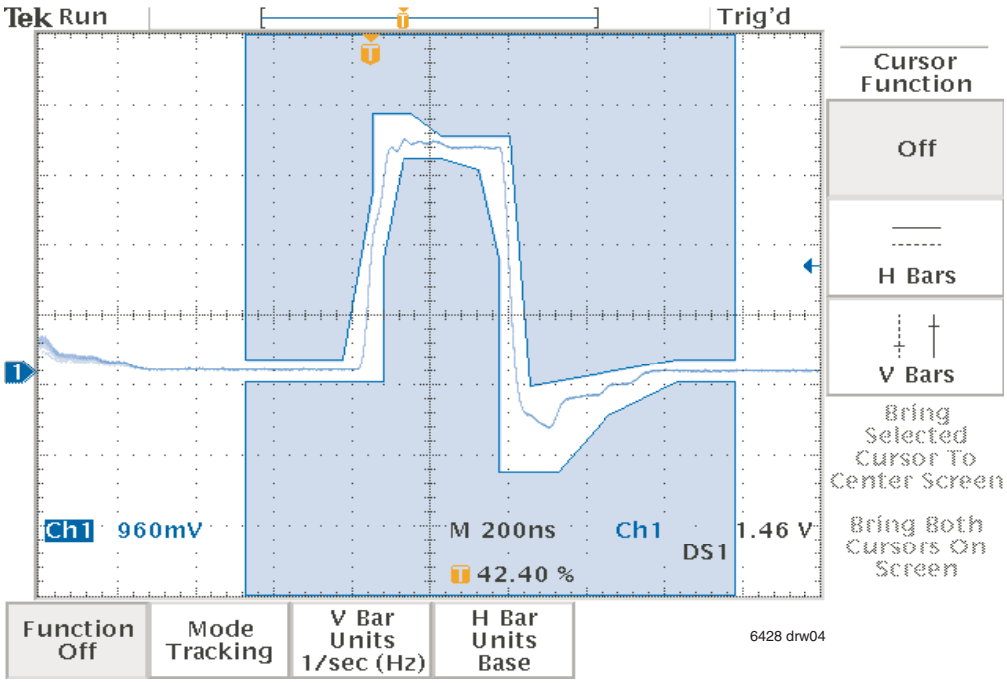

Figure 4a. T1 Pulse Mask - Primary Card Transmit Secondary Card in Stand By

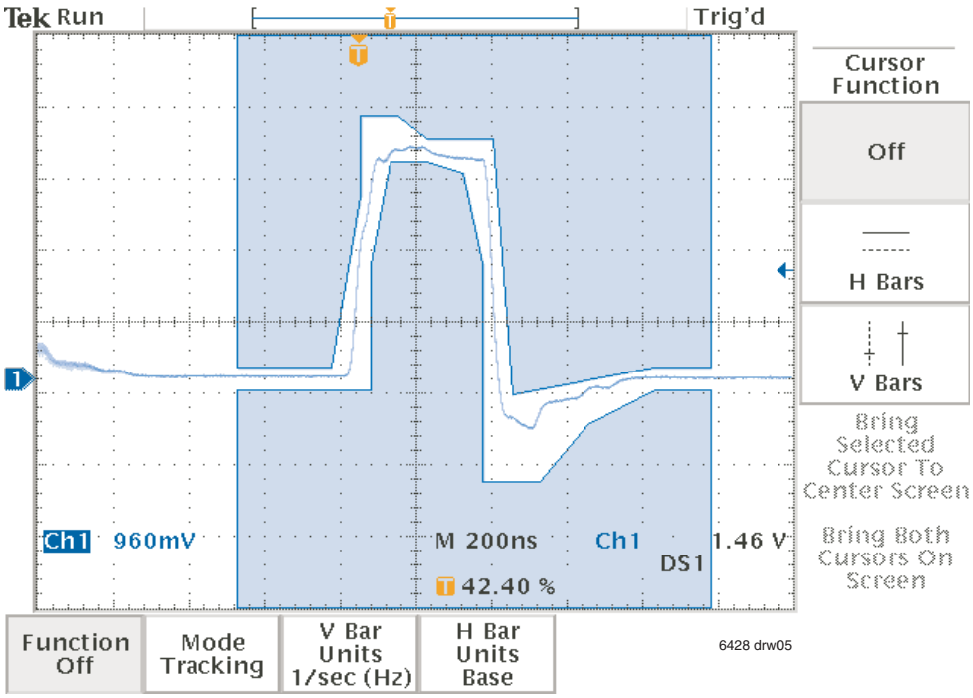

Figure 4b. T1 Pulse Mask - Primary Card Transmits, Secondary Card Powered Down

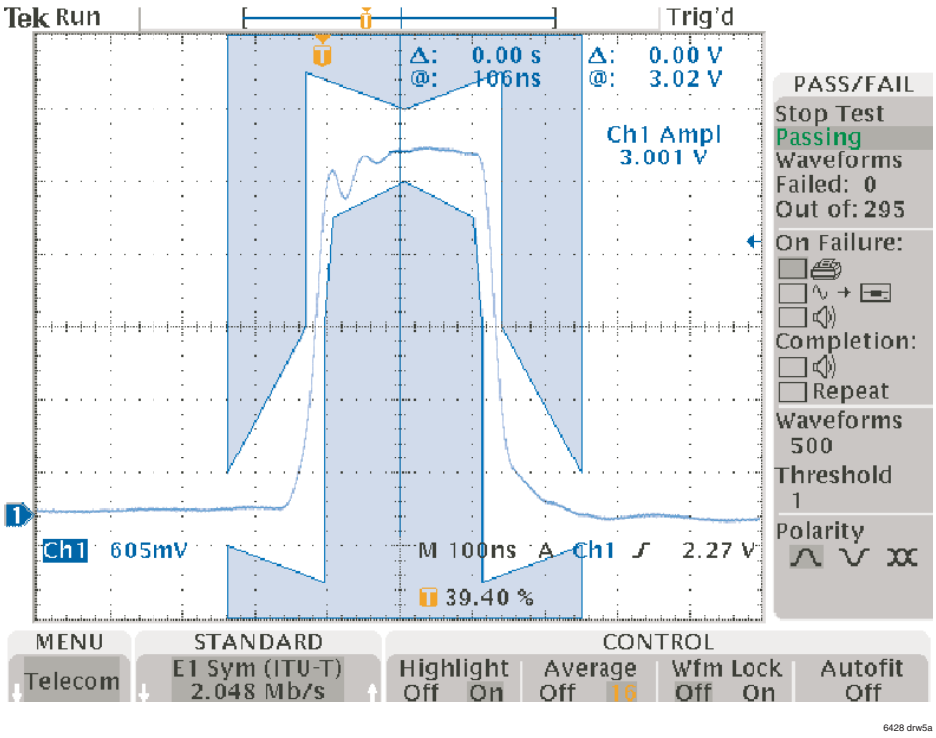

Figure 5a. E1 Pulse Mask - Primary Card Transmits, Secondary Card Standby

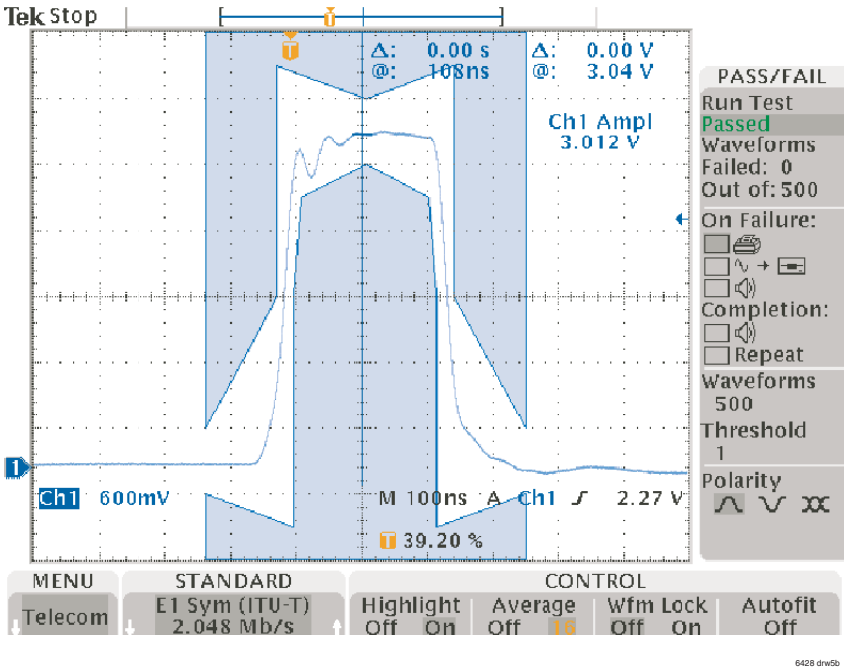

Figure 5b. E1 Pulse Mask - Primary Card Transmits, Secondary Card Powered Down

5.3 RECEIVE RETURN LOSS

TABLE 4 — E1/120Ω (IMPEDANCE - INTERNAL MODE, Rr = 120)

FREQUENCY (KHZ)	51	90	102	1000	1024	2000	2048	2500	3000
RL (DB) dual board	-27.098	-28.256	-28-657	-27.134	-24-607	-24.324	-24.613	-28-741	-29.596
RL (dB) single board	-27-192	-28-749	-28-61	-27-532	-27.634	-27-233	-27.471	-37.215	-40.202

5.4 TRANSMITTER RETURN LOSS

TABLE 5 — E1/120Ω, IMPEDANCE=INTERNAL MODE, Cp = 560pF

FREQUENCY (KHZ)	51	90	102	1000	1024	2000	2048	2500	3000
DEVICE A	-15.494	-19.736	-20.338	-22.269	-22.383	-18.591	-18.336	-16.728	-15.164
DEVICE B	-15.983	-20.678	-21.766	-25.593	-25.64	-20.541	-20.076	-18.187	-16.279

5.5.1 TEST SETUP

Figure 6 – 7 shows the test setups of different HPS tests conducted by IDT Telecom Laboratory

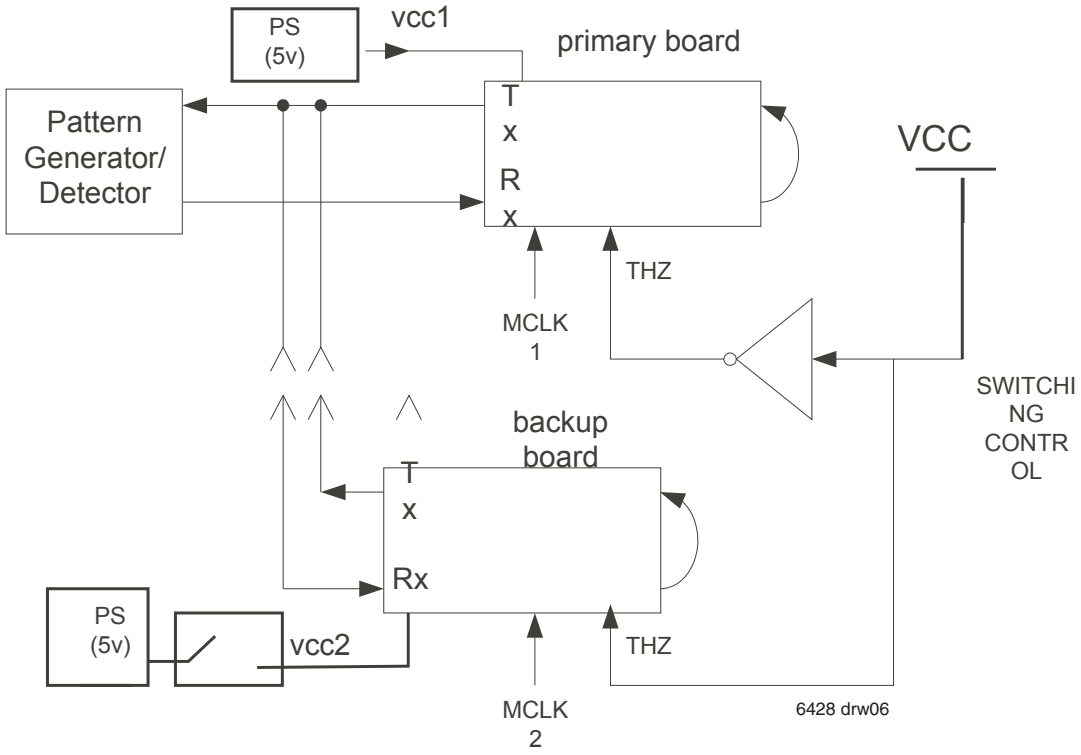

Figure 6. Test Setup #1 (Power Failure Test Setup)

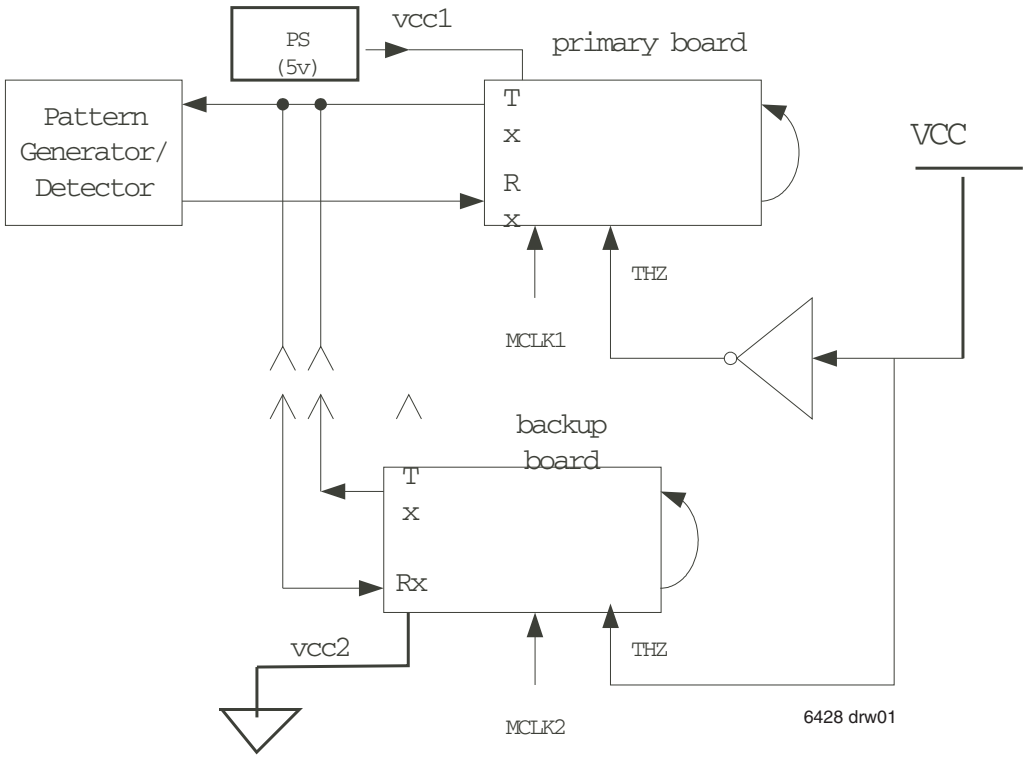

Figure 7. Test Setup #2 (Power Supply Short Test Setup)

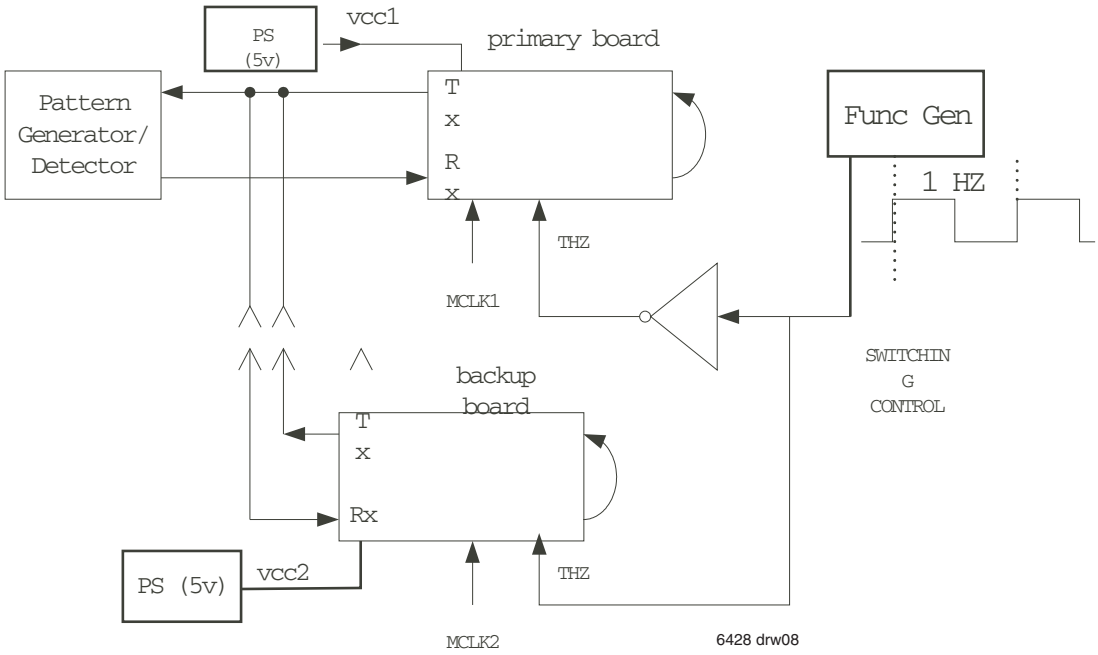

Figure 8. Test Setup #3 (Hot-Switch Test Setup)

6. CONCLUSION

IDT82V2081/2/4/8 T1/E1/J1 universal line interface units are highly integrated LIU that enables 1+1 relay-less hitless protection. As shown by IDT laboratory test result, the integrated features maintains outstanding signal integrity in HPS application and provides excellent design margin to achieve high system availability, reliability and serviceability.

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