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April 1st, 2010
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38D5 Group

LCD Drive Control Circuit (External Dividing Resister Usage)

1. Abstract

The following article introduces and shows an example of how to use the LCD Drive Control Circuit (External Dividing Resister Usage) on the 38D5 Group device.

2. Introduction

The application explained in this document applies to the following MCU and parameter(s):
Applicable MCU: 38D5 Group
Frame frequency: 8 MHz

This sample program may include operations of unused bit functions for the convenience of the SFR bit layout. Set the values according to the operational conditions of the user system.

3. Contents

3.1 LCD Panel Display

Outline: The LCD LCD drive control circuit is used for displaying the LCD panel.

Specifications:

- Segment output SEG_{16} to SEG_{35} and common COM_0 to COM_3 are used.
- Frame frequency = 61 Hz
- Duty ratio = 4, Bias value = 1/3
- Voltage multiplier is used.
- "M38d5" is displayed.

Figure 3.1 shows a Segment Allocation Example, Figure 3.2 shows the Circuit Example, Figure 3.3 shows the LCD Display RAM Map, Figure 3.4 shows as LCD Display RAM Setting Example, Figure 3.5 shows the Relevant Register Settings, and Figure 3.6 shows the Control Procedure.

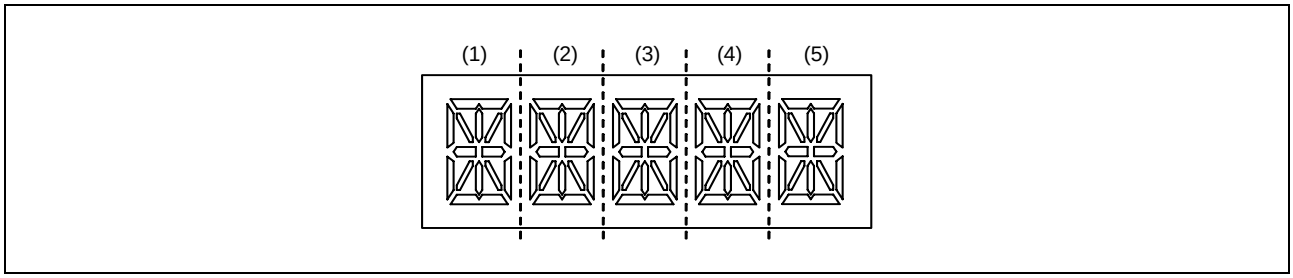

Figure 3.1 Segment Allocation Example

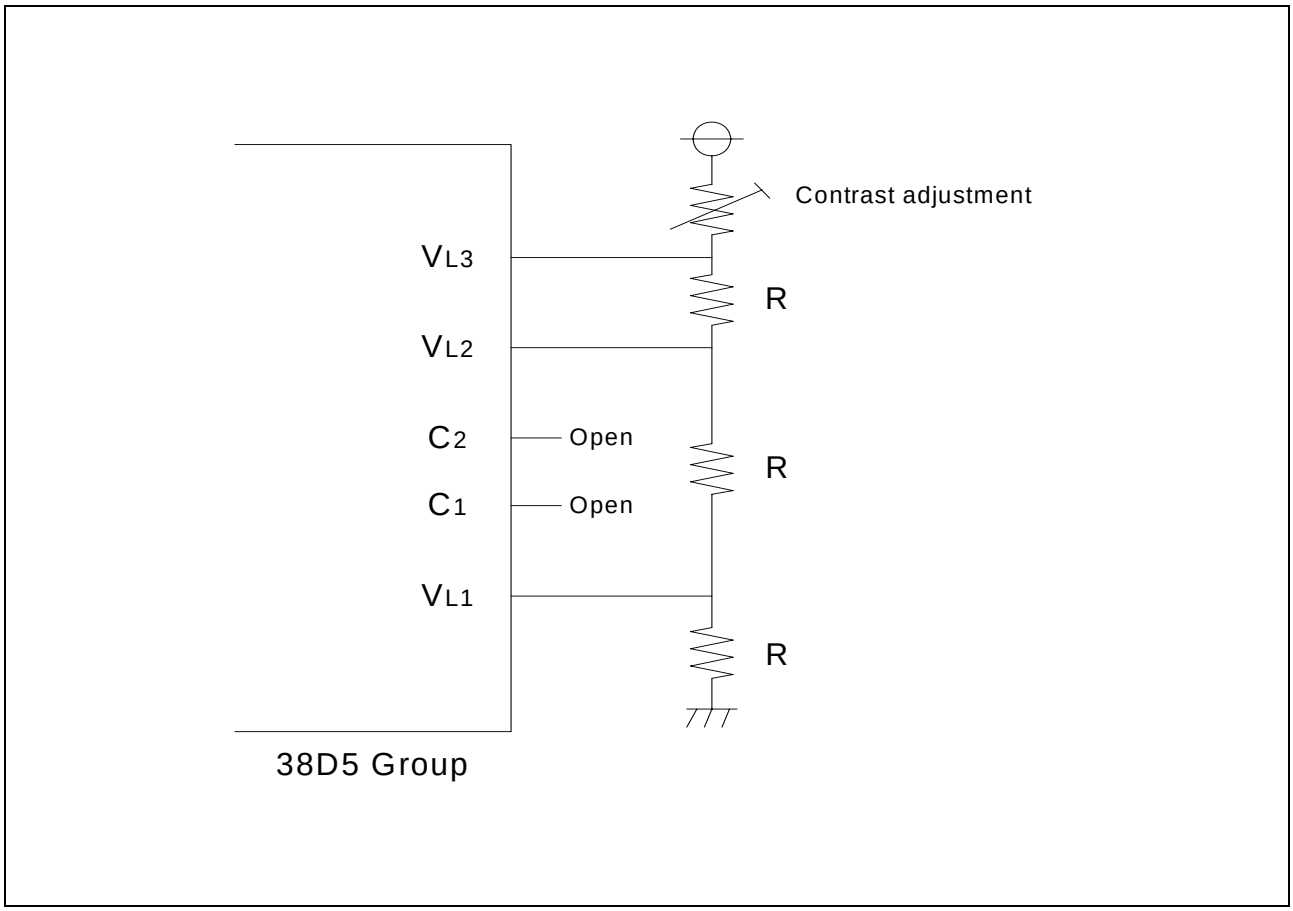

Figure 3.2 Circuit Example

4COM × 36SEG

Address	Bit	7	6	5	4	3	2	1	0
0840h	LRAM0	Not used (Can generally be used as RAM)				SEG_0			
0841h	LRAM1					SEG_1			
0842h	LRAM2					SEG_2			
0843h	LRAM3					SEG_3			
0844h	LRAM4					SEG_4			
0845h	LRAM5					SEG_5			
0846h	LRAM6					SEG_6			
0847h	LRAM7					SEG_7			
0848h	LRAM8					SEG_8			
0849h	LRAM9					SEG_9			
084Ah	LRAM10					SEG_{10}			
084Bh	LRAM11					SEG_{11}			
084Ch	LRAM12					SEG_{12}			
084Dh	LRAM13					SEG_{13}			
084Eh	LRAM14					SEG_{14}			
084Fh	LRAM15					SEG_{15}			
0850h	LRAM16					SEG_{16}			
0851h	LRAM17					SEG_{17}			
0852h	LRAM18					SEG_{18}			
0853h	LRAM19					SEG_{19}			
0854h	LRAM20					SEG_{20}			
0855h	LRAM21					SEG_{21}			
0856h	LRAM22					SEG_{22}			
0857h	LRAM23					SEG_{23}			
0858h	LRAM24					SEG_{24}			
0859h	LRAM25					SEG_{25}			
085Ah	LRAM26					SEG_{26}			
085Bh	LRAM27					SEG_{27}			
085Ch	LRAM28					SEG_{28}			
085Dh	LRAM29					SEG_{29}			
085Eh	LRAM30					SEG_{30}			
085Fh	LRAM31					SEG_{31}			
0860h	LRAM32					SEG_{32}			
0861h	LRAM33					SEG_{33}			
0862h	LRAM34					SEG_{34}			
0863h	LRAM35					SEG_{35}			
						COM3	COM2	COM1	COM0

Figure 3.3 LCD Display RAM Map

4COM × 36SEG

Address		Bit 7	6	5	4	3	2	1	0	Digit
						COM3	COM2	COM1	COM0	
0840h	LRAM0									
0841h	LRAM1									
0842h	LRAM2									
0843h	LRAM3									
0844h	LRAM4									
0845h	LRAM5									
0846h	LRAM6									
0847h	LRAM7									
0848h	LRAM8									
0849h	LRAM9									
084Ah	LRAM10									
084Bh	LRAM11									
084Ch	LRAM12									
084Dh	LRAM13									
084Eh	LRAM14									
084Fh	LRAM15									
0850h	LRAM16					d	c	b	a	→ (1)
0851h	LRAM17					h	g	f	e	→ (1)
0852h	LRAM18					k	j		i	→ (1)
0853h	LRAM19					n	m		l	→ (1)
0854h	LRAM20					d	c	b	a	→ (2)
0855h	LRAM21					h	g	f	e	→ (2)
0856h	LRAM22					k	j		i	→ (2)
0857h	LRAM23					n	m		l	→ (2)
0858h	LRAM24					d	c	b	a	→ (3)
0859h	LRAM25					h	g	f	e	→ (3)
085Ah	LRAM26					k	j		i	→ (3)
085Bh	LRAM27					n	m		l	→ (3)
085Ch	LRAM28					d	c	b	a	→ (4)
085Dh	LRAM29					h	g	f	e	→ (4)
085Eh	LRAM30					k	j		i	→ (4)
085Fh	LRAM31					n	m		l	→ (4)
0860h	LRAM32					d	c	b	a	→ (5)
0861h	LRAM33					h	g	f	e	→ (5)
0862h	LRAM34					k	j		i	→ (5)
0863h	LRAM35					n	m		l	→ (5)

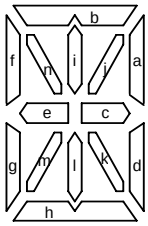

Figure 3.4 LCD Display RAM Setting Example

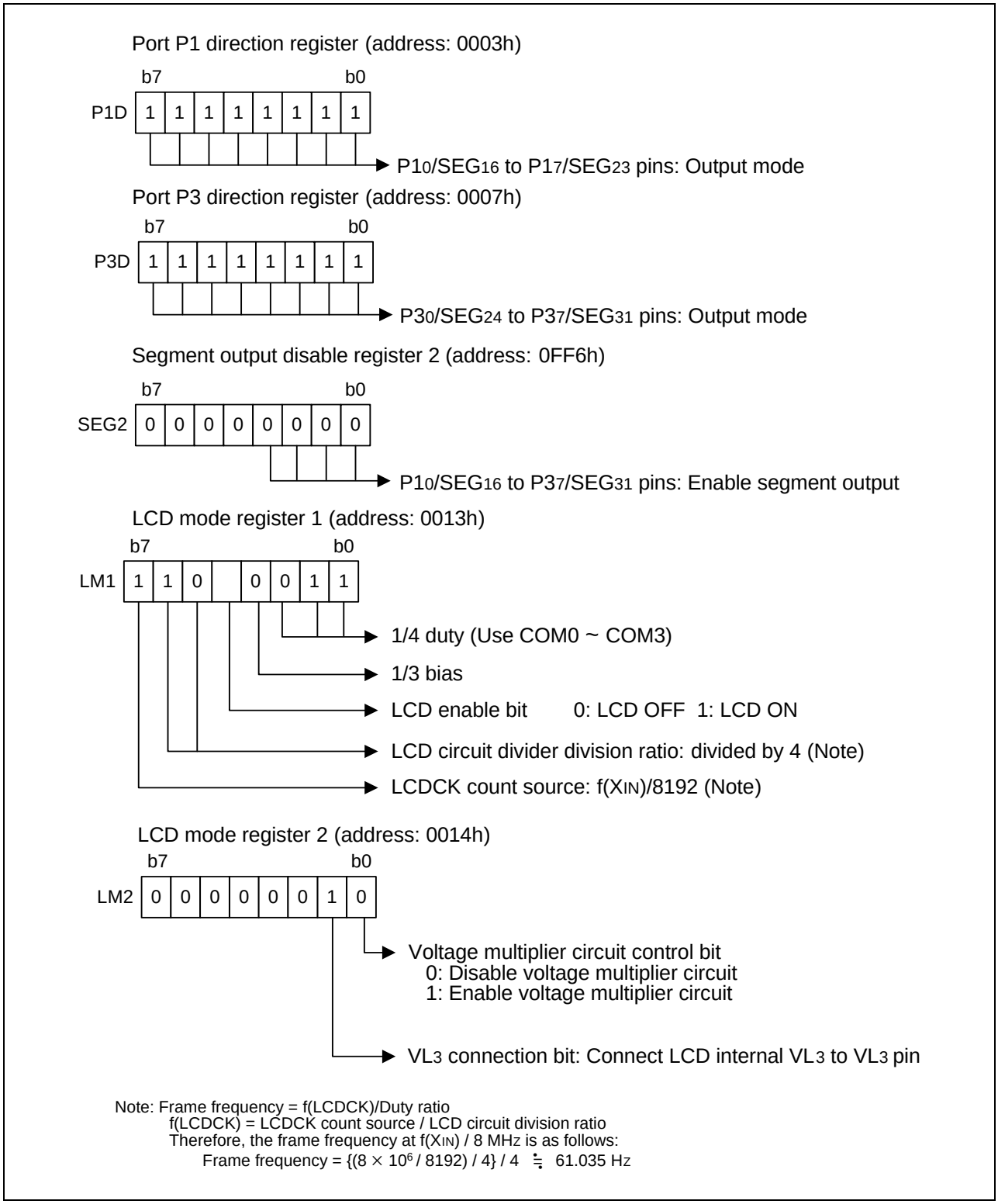

Figure 3.5 Relevant Register Settings

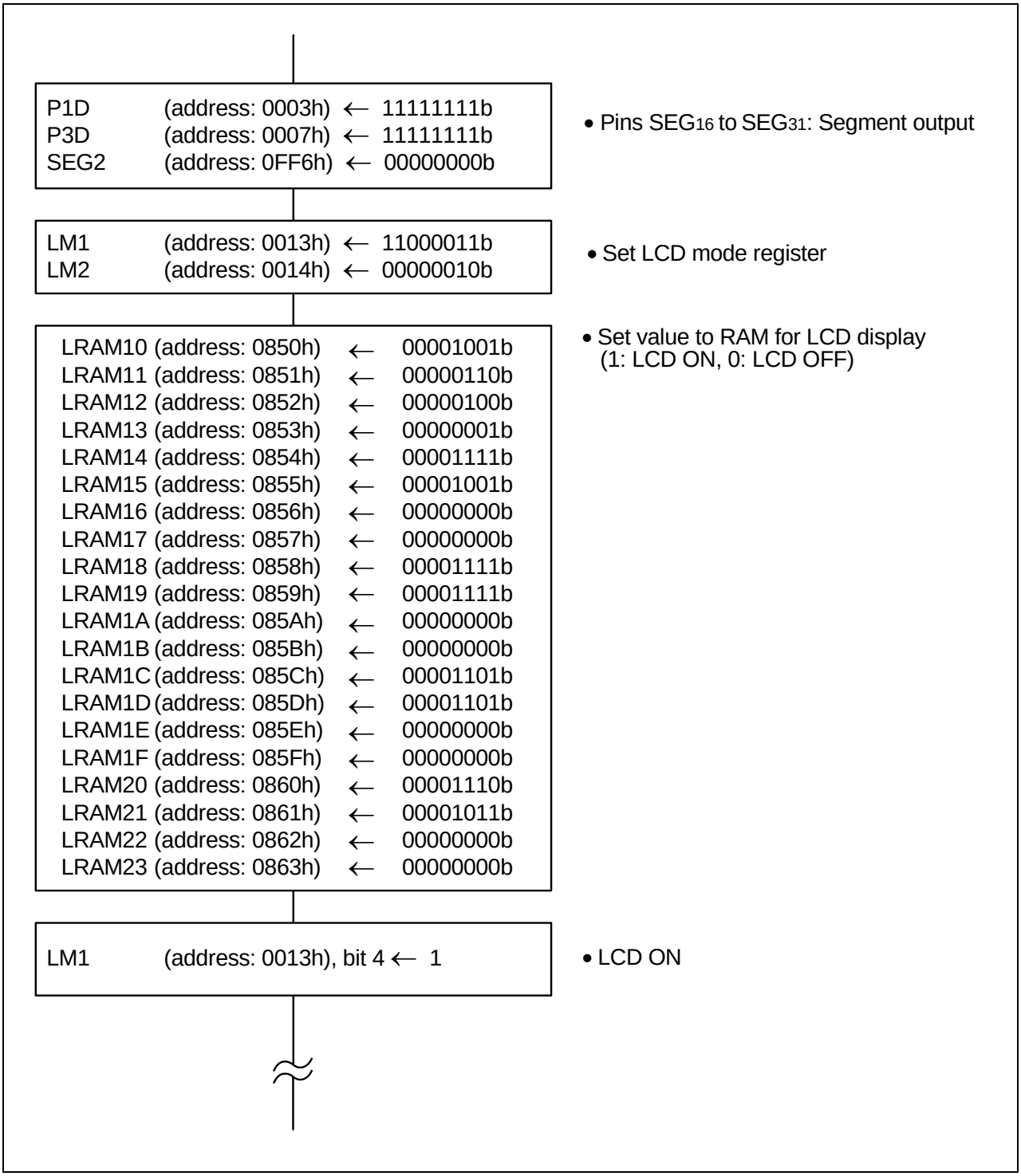

Figure 3.6 Control Procedure

4. Sample Programming Code

Download a sample program from the Renesas Technology website.
To download, click “Application Notes” in the left side menu on the page of the 38D5 Group.

5. Reference Document

Datasheet
38D5 Group Datasheet
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REVISION HISTORY	38D5 Group LCD Drive Control Circuit (External Dividing Resister Usage)

Rev.	Date	Description	
		Page	Summary
1.00	Sep 15, 2006	–	First Edition issued
2.00	Jan 21, 2008	5	V_{L3} connection bit revised
		–	Sample programming code changed

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