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38D2 Group

Serial I/O

1. Abstract

This document describes serial I/O for 38D2 Group.

2. Introduction

The application explained in this document applies to the following MCU.

- Applicable MCU: 38D2 Group

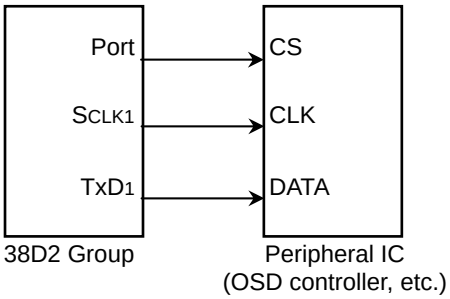
3. Description

3.1 Serial I/O Connection Examples

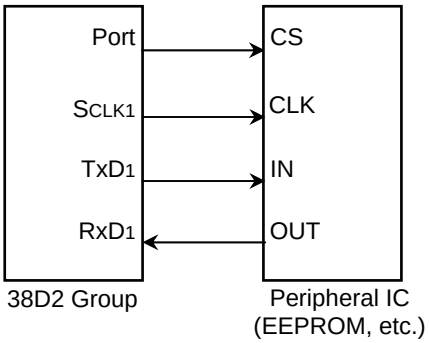
3.1.1 Controlling Peripheral IC Equipped with CS Pins

Figure 3.1 shows a connection example of serial I/O. This example is a connection with a peripheral IC equipped with a CS pin in clock synchronous serial I/O mode.

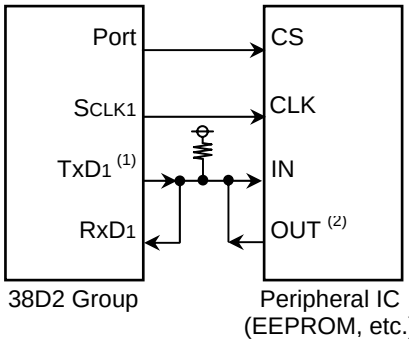
1. Transmission only
(Using the RxD1 pin as an I/O port)



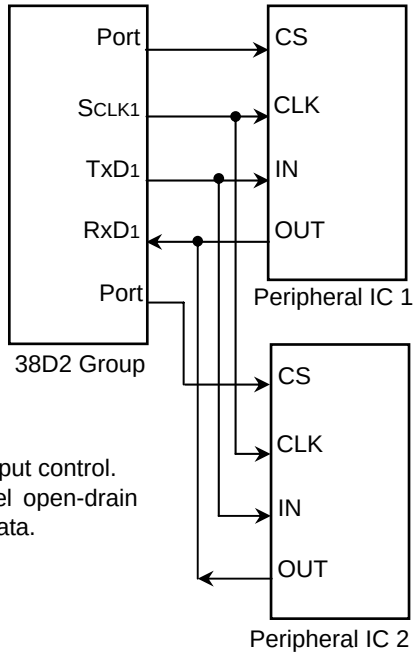
2. Transmission and reception



3. Transmission and reception
(When connecting RxD1 with TxD1)



4. Connecting multiple ICs



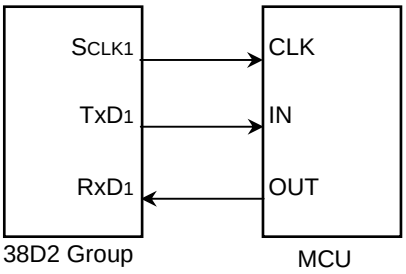
Notes:
1. Select an N-channel open-drain output for TxD1 pin output control.
2. Use the peripheral IC OUT pin which is an N-channel open-drain output and becomes high impedance while receiving data.
3. "Port" means an output port controlled by software.
4. This is a connection example for serial I/O1.
Use following pins for serial I/O2:
TxD1 → TxD2
RxD1 → RxD2
SCLK1 → SCLK2

Figure 3.1 Serial I/O Connection Examples (1/2)

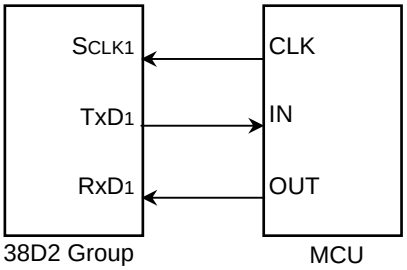
3.1.2 Connection with MCU

Figure 3.2 shows a connection example of serial I/O. This example shows a connection with another MCU.

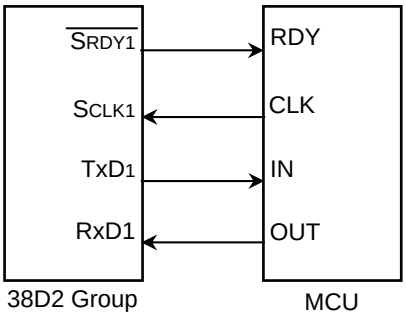
1. Selecting an internal clock in clock synchronous serial I/O mode



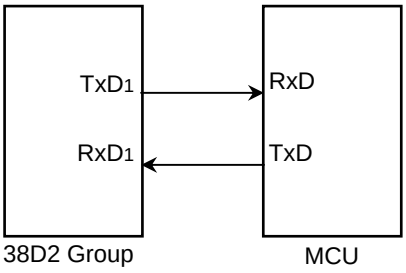
2. Selecting an external clock in clock synchronous serial I/O mode



3. Using the $\overline{\text{SRDY1}}$ signal output function in clock synchronous serial I/O mode (selecting an external clock)



4. In UART mode



Note

1. This is a connection example for serial I/O1.
   Use the following pins for serial I/O2:
   TxD1 → TxD2
   RxD1 → RxD2
   SCLK1 → SCLK2
   $\overline{\text{SRDY1}}$ → $\overline{\text{SRDY2}}$

Figure 3.2 Serial I/O Connection Examples (2/2)

3.2 Serial I/O Transfer Data Format

Clock synchronous or clock asynchronous (UART) can be selected for serial I/O1 and serial I/O2. Figure 3.3 shows the serial I/O transfer data format.

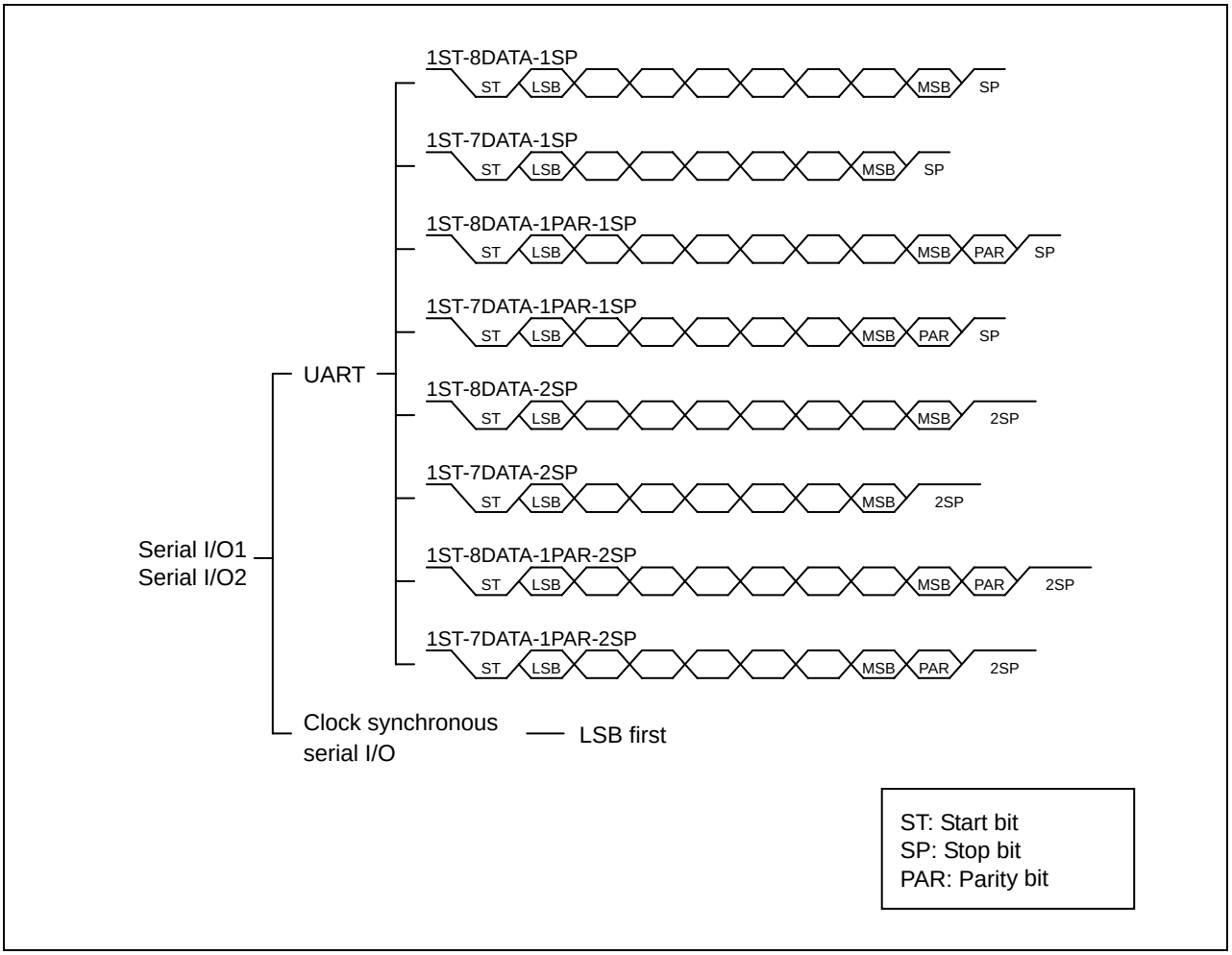


Figure 3.3 Serial I/O Transfer Data Format

3.3 Serial I/O1 Operation: Stop and Initialize

3.3.1 Clock Synchronous Serial I/O Mode

■ Stop/initialize transmit operation only when transmitting
Set the transmit enable bit to 0.

By setting the transmit enable bit to 0, the transmit operations listed below will be stopped and initialized:
- Stop supply of shift clock to transmit shift register
- Initialize transmit clock control circuit
- Transmit buffer empty flag becomes 0
- Transmit shift register shift complete flag becomes 0
- P55/TxD1 pin: I/O port P55

By setting the serial I/O1 enable bit to 0, pins P54/RxD1, P55/TxD1, P56/SCLK1, and P57/$\overline{\text{SRDY1}}$ all become I/O ports.

■ Stop/initialize receive operation only when receiving
Set the receive enable bit or serial I/O1 enable bit to 0.

By setting the receive enable bit to 0, the receive operations listed below will be stopped and initialized.
- Stop supply of shift clock to receive shift register
- Initialize receive clock control circuit
- Error flags (over-run, parity, framing, and summing error flags) become 0
- Receive buffer full flag becomes 0
- P54/RxD1 pin: I/O port P54

By setting the serial I/O1 enable bit to 0, the receive operations listed below will be stopped and initialized.
- Stop supply of shift clock to receive shift register
- Initialize receive clock control circuit
- Error flags (over-run, parity, framing, and summing error flags) become 0
- Receive buffer full flag becomes 0
- P54/RxD1, P55/TxD1, P56/SCLK1, and P57/$\overline{\text{SRDY1}}$ pins: I/O ports P54, P55, P56, and P57

■ Stop/initialize receive/transmit operation when both transmitting and receiving
Set the transmit enable bit and receive enable bit to 0 simultaneously.

3.3.2 UART Mode

■ Stop/initialize transmit operation
Set the transmit enable bit to 0.

■ Stop/initialize receive operation
Set the receive enable bit to 0.

3.4 Serial I/O2 Operation: Stop and Initialize

3.4.1 Clock Synchronous Serial I/O Mode

■ Stop/initialize transmit operation only when transmitting
Set the transmit enable bit to 0.

By setting the transmit enable bit to 0, the transmit operations listed below will be stopped and initialized.
- Stop supply of shift clock to transmit shift register
- Initialize transmit clock control circuit
- Transmit buffer empty flag becomes 0
- Transmit shift register shift complete flag becomes 0
- $P3_2$/TxD_2 pin: I/O port $P3_2$

By setting the serial I/O2 enable bit to 0, pins $P3_3$/RxD_2, $P3_2$/TxD_2, $P3_1$/$SCLK_2$, and $P3_0$/$\overline{SRDY_2}$ all become I/O ports.

■ Stop/initialize receive operation only when receiving
Set the receive enable bit or serial I/O2 enable bit to 0.

By setting the receive enable bit to 0, the receive operations listed below will be stopped and initialized.
- Stop supply of shift clock to receive shift register
- Initialize receive clock control circuit
- Error flags (over-run, parity, framing, and summing error flags) become 0
- Receive buffer full flag becomes 0
- $P3_3$/ RxD_2 pin: I/O port $P3_3$

By setting the serial I/O2 enable bit to 0, the receive operations listed below will be stopped and initialized.
- Stop supply of shift clock to receive shift register
- Initialize receive clock control circuit
- Error flags (over-run, parity, framing, and summing error flags) become 0
- Receive buffer full flag becomes 0
- $P3_3$/RxD_2, $P3_2$/TxD_2, $P3_1$/$SCLK_2$, and $P3_0$/$\overline{SRDY_2}$ pins: I/O ports $P3_3$, $P3_2$, $P3_1$, and $P3_0$

■ Stop/initialize receive/transmit operation when both transmitting and receiving
Set the transmit enable bit and receive enable bit to 0 simultaneously.

3.4.2 UART Mode

■ Stop/initialize transmit operation
Set the transmit enable bit to 0.

■ Stop/initialize receive operation
Set the receive enable bit to 0.

3.5 Serial I/O Pin Function and Selection Method

3.5.1 Serial I/O1

Table 3.1 shows the pin functions in clock synchronous serial I/O mode, and Table 3.2 shows the pin functions in UART mode.

Table 3.1 Pin Functions in Clock Synchronous Serial I/O Mode

Pin Name	Function	Serial I/O1 Control Register (Address 1A16)								Corresponding Direction Register
		b7	b6	b5	b4	b3	b2	b1	b0	
		SIOE	SIOM	RE	TE	TIC	SRDY	SCS	CSS	
P54/RxD1	RxD1	1	1	1	×	×	×	×	×	×
	P54	1	1	0	×	×	×	×	×	0/1
P55/TxD1	TxD1	1	1	×	1	×	×	×	×	×
	P55	1	1	×	0	×	×	×	×	0/1
P56/SCLK1	SCLK1 (external clock input)	1	1	×	×	×	×	1	×	×
	SCLK1 (internal clock output)	1	1	×	1	×	×	0	×	×
P57/$\overline{\text{SRDY1}}$	$\overline{\text{SRDY1}}$	1	1	×	×	×	1	×	×	×
	P57	1	1	×	×	×	0	×	×	0/1

Note: When SIOE is 0, all pins become I/O ports regardless of the values set to b6 to b0.
×: This is not used for the pin's function setting.

Table 3.2 Pin Functions in UART Mode

Pin Name	Function	Serial I/O1 Control Register (Address 1A16)								Corresponding Direction Register
		b7	b6	b5	b4	b3	b2	b1	b0	
		SIOE	SIOM	RE	TE	TIC	SRDY	SCS	CSS	
P54/RxD1	RxD1	1	0	1	×	×	×	×	×	×
	P54	1	0	0	×	×	×	×	×	0/1
P55/TxD1	TxD1	1	0	×	1	×	×	×	×	×
	P55	1	0	×	0	×	×	×	×	0/1
P56/SCLK1	SCLK1 (external clock input)	1	0	×	×	×	×	1	×	×
	P56	1	0	×	×	×	×	0	×	0/1
P57/$\overline{\text{SRDY1}}$	P57	1	0	×	×	×	×	×	×	0/1

Note: When SIOE is 0, all pins become I/O ports regardless of the values set to b6 to b0.
×: This is not used for the pin's function setting.

3.5.2 Serial I/O2

Table 3.3 shows the pin functions in clock synchronous serial I/O mode, and Table 3.4 shows the pin functions in the UART mode.

Table 3.3 Pin Functions in Clock Synchronous Serial I/O Mode

Pin Name	Function	Serial I/O2 Control Register (Address $1F_{16}$)								Corresponding Direction Register
		b7	b6	b5	b4	b3	b2	b1	b0	
		SIOE	SIOM	RE	TE	TIC	SRDY	SCS	CSS	
$P3_3/RxD_2$	RxD_2	1	1	1	×	×	×	×	×	×
	$P3_3$	1	1	0	×	×	×	×	×	0/1
$P3_2/TxD_2$	TxD_2	1	1	×	1	×	×	×	×	×
	$P3_2$	1	1	×	0	×	×	×	×	0/1
$P3_1/SCLK_2$	$SCLK_2$ (external clock input)	1	1	×	×	×	×	1	×	×
	$SCLK_2$ (internal clock output)	1	1	×	1	×	×	0	×	×
$P3_0/\overline{SRDY_2}$	$\overline{SRDY_2}$	1	1	×	×	×	1	×	×	×
	$P3_0$	1	1	×	×	×	0	×	×	0/1

Note: When SIOE is 0, all pins become I/O ports regardless of the values set to b6 to b0.
×: This is not used for the pin's function setting.

Table 3.4 Pin Function in UART Mode

Pin Name	Function	Serial I/O2 Control Register (Address $1F_{16}$)								Corresponding Direction Register
		b7	b6	b5	b4	b3	b2	b1	b0	
		SIOE	SIOM	RE	TE	TIC	SRDY	SCS	CSS	
$P3_3/RxD_2$	RxD_2	1	0	1	×	×	×	×	×	×
	$P3_3$	1	0	0	×	×	×	×	×	0/1
$P3_2/TxD_2$	TxD_2	1	0	×	1	×	×	×	×	×
	$P3_2$	1	0	×	0	×	×	×	×	0/1
$P3_1/SCLK_2$	$SCLK_2$ (external clock input)	1	0	×	×	×	×	1	×	×
	$P3_1$	1	0	×	×	×	×	0	×	0/1
$P3_0/\overline{SRDY_2}$	$P3_0$	1	0	×	×	×	×	×	×	0/1

Note: When SIOE is 0, all pins become I/O ports regardless of the values set to b6 to b0.
×: This is not used for the pin's function setting.

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38D2 Group Datasheet

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