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April 1<sup>st</sup>, 2010  
Renesas Electronics Corporation

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# 3850 Group (Spec.A)

## List of Registers

### 1. Abstract

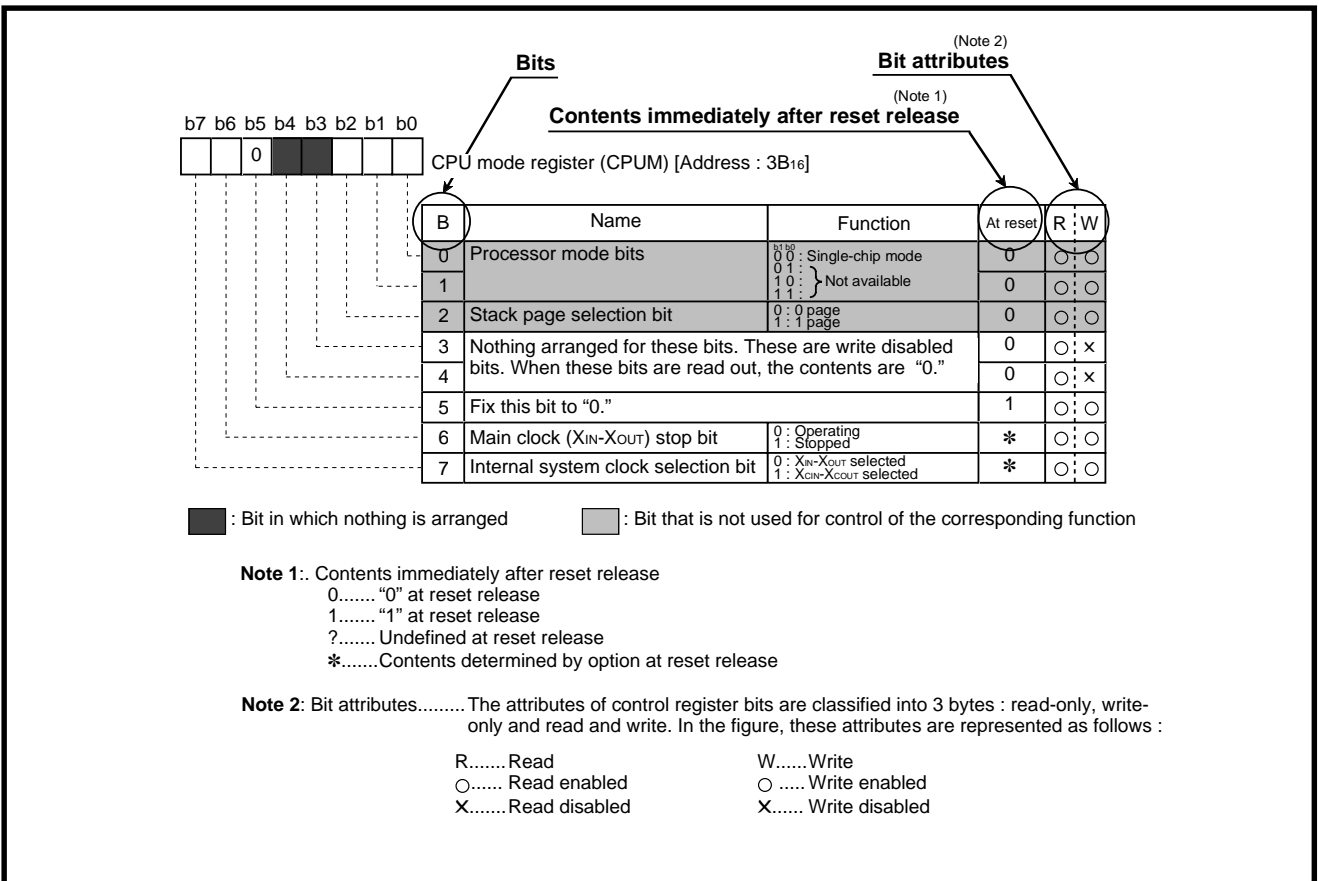
The following article describes the control registers of the 3850 Group (Spec.A).

### 2. Introduction

The explanation of this issue is applied to the following condition:  
Applicable MCU: 3850 Group (Spec.A)

### 3. Structure of Register

The figure of each register structure describes its functions, contents at reset, and attributes as follows:



4 List of registers

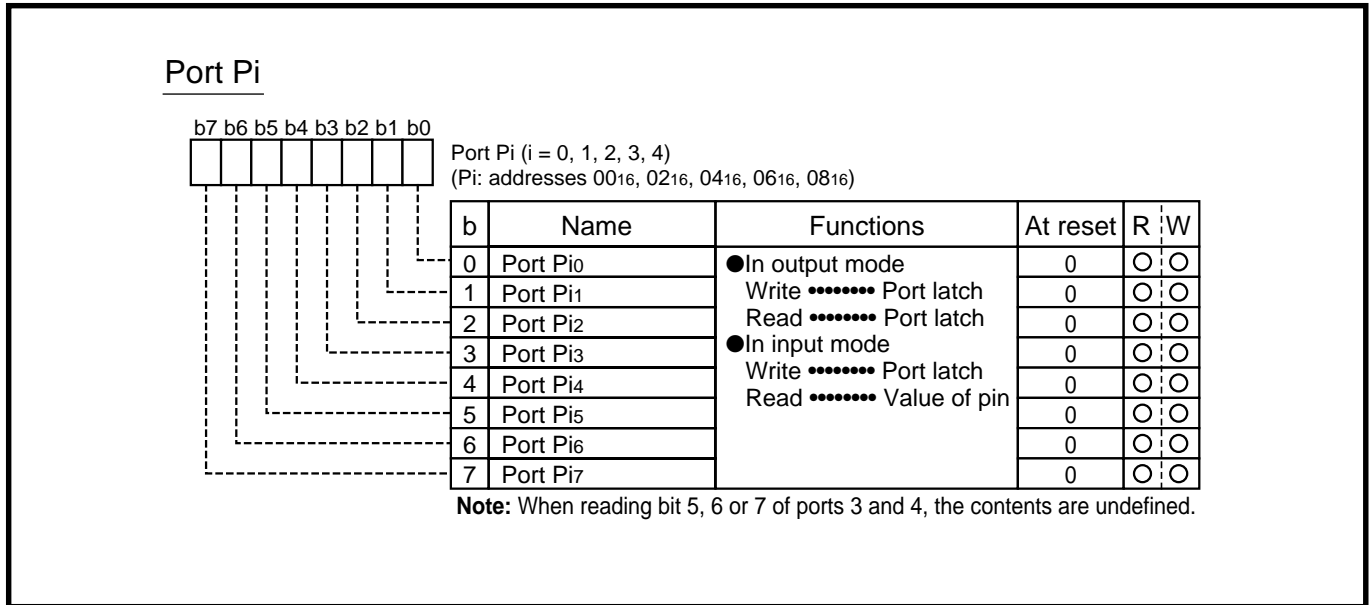


Fig. 4.1 Structure of Port Pi

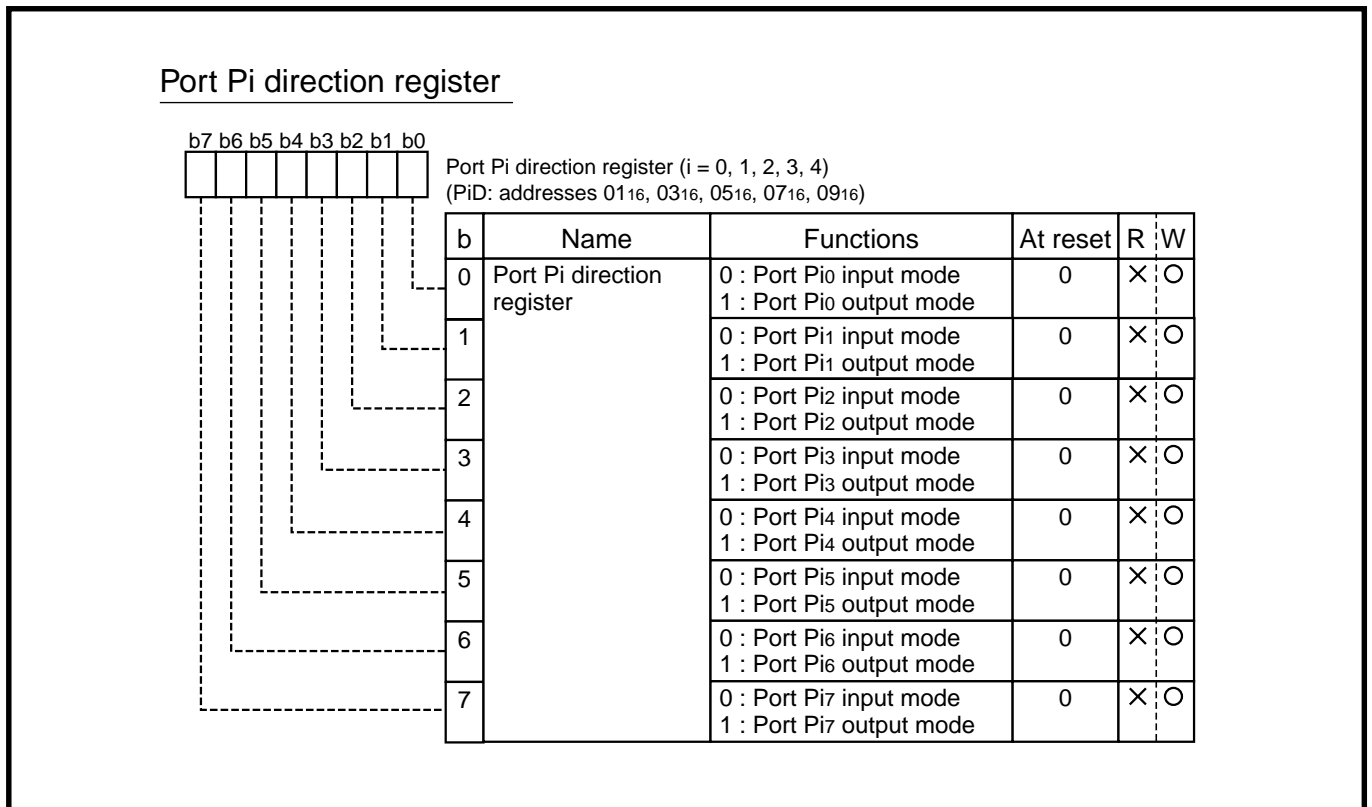


Fig. 4.2 Structure of Port Pi direction register

Port P0, P1, P2 pull-up control register

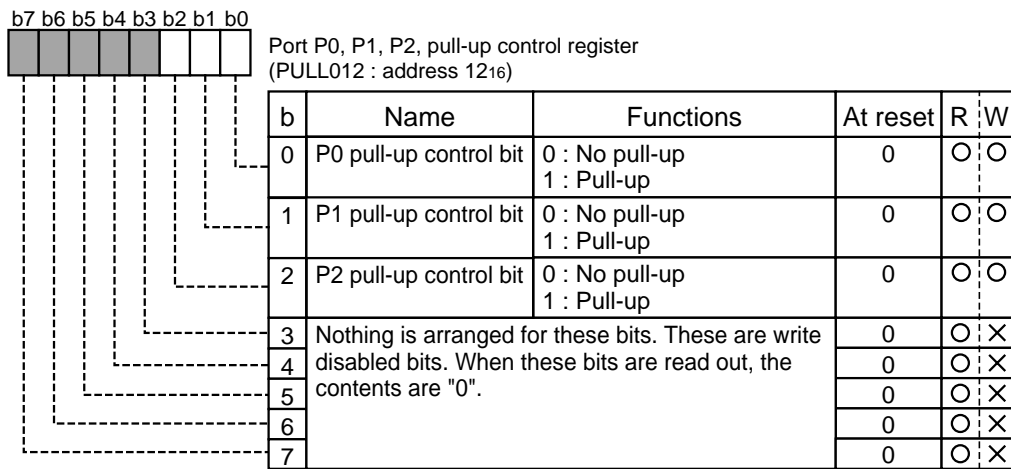


Fig. 4.3 Structure of Port P0, P1, P2 pull-up control register

Port P3 pull-up control register

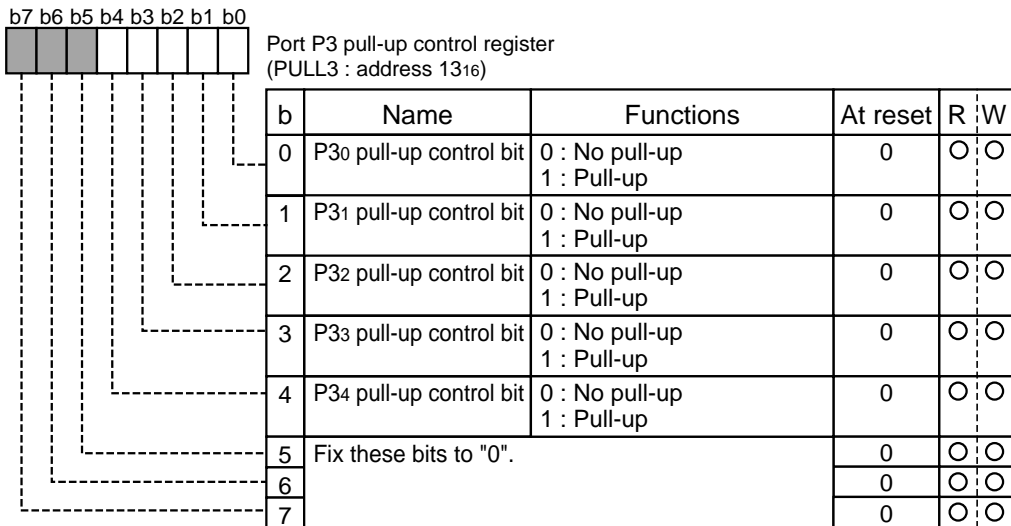


Fig. 4.4 Structure of Port P3 pull-up control register

Port P4 pull-up control register

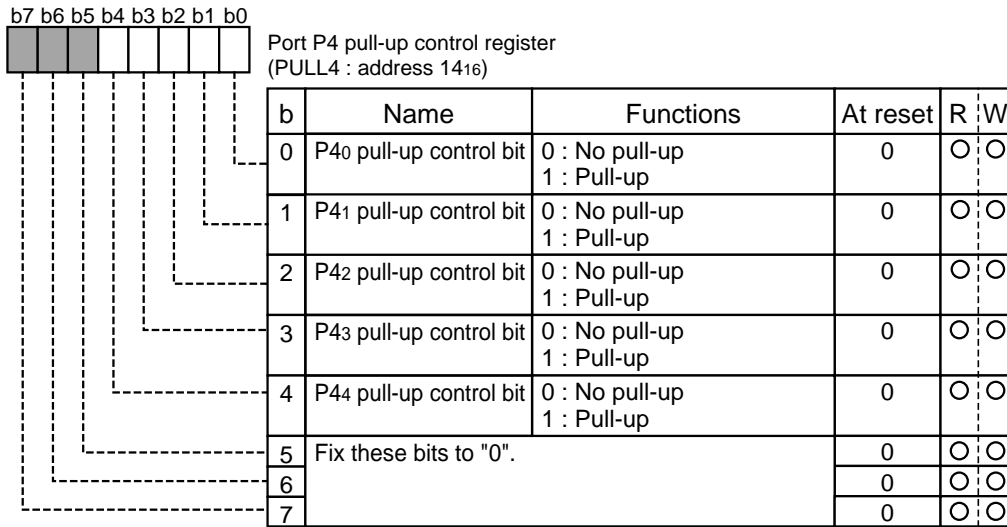


Fig. 4.5 Structure of Port P4 pull-up control register

Serial I/O2 control register 1

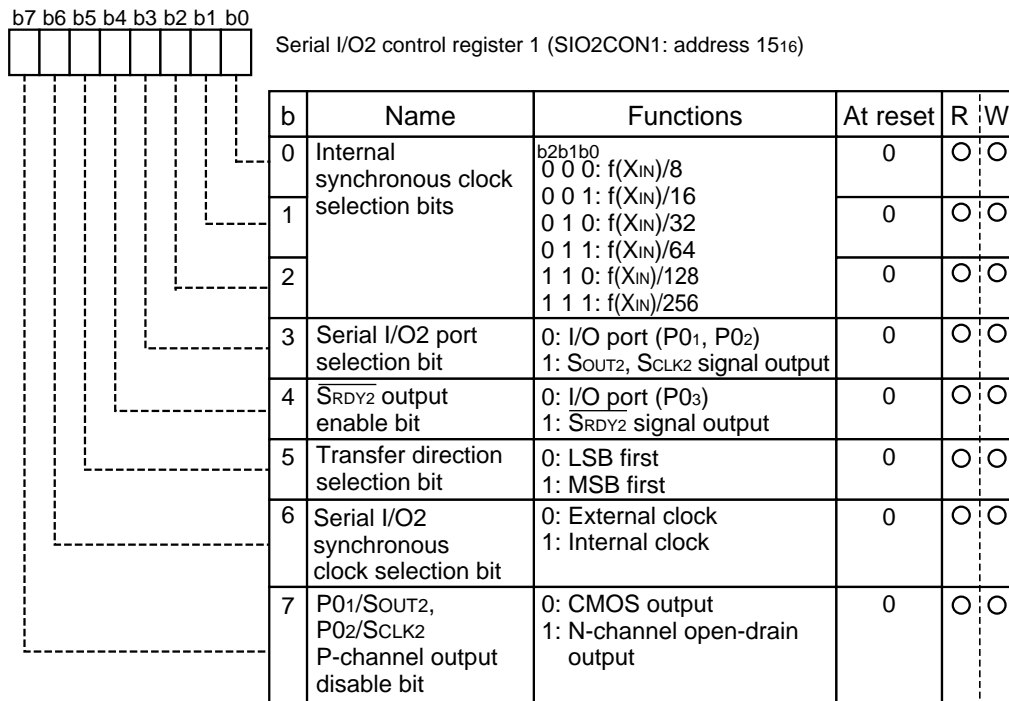


Fig. 4.6 Structure of Serial I/O2 control register 1

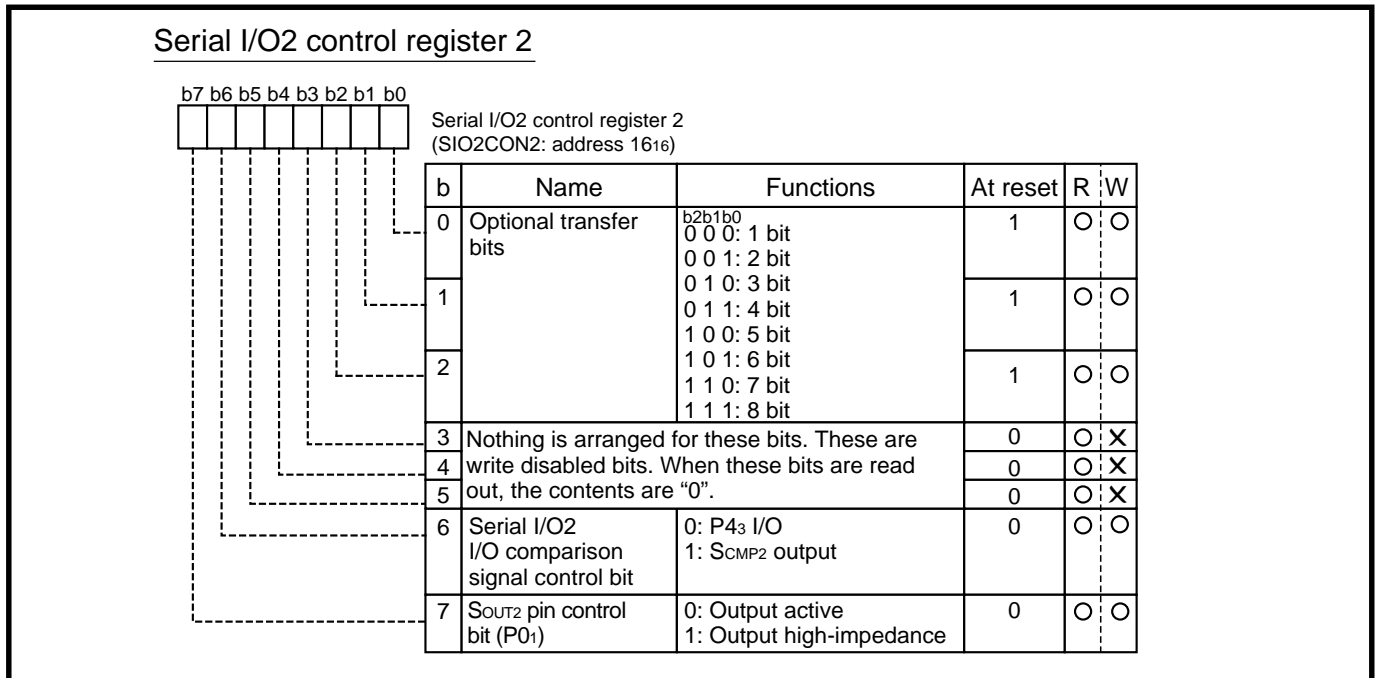


Fig. 4.7 Structure of Serial I/O2 control register 2

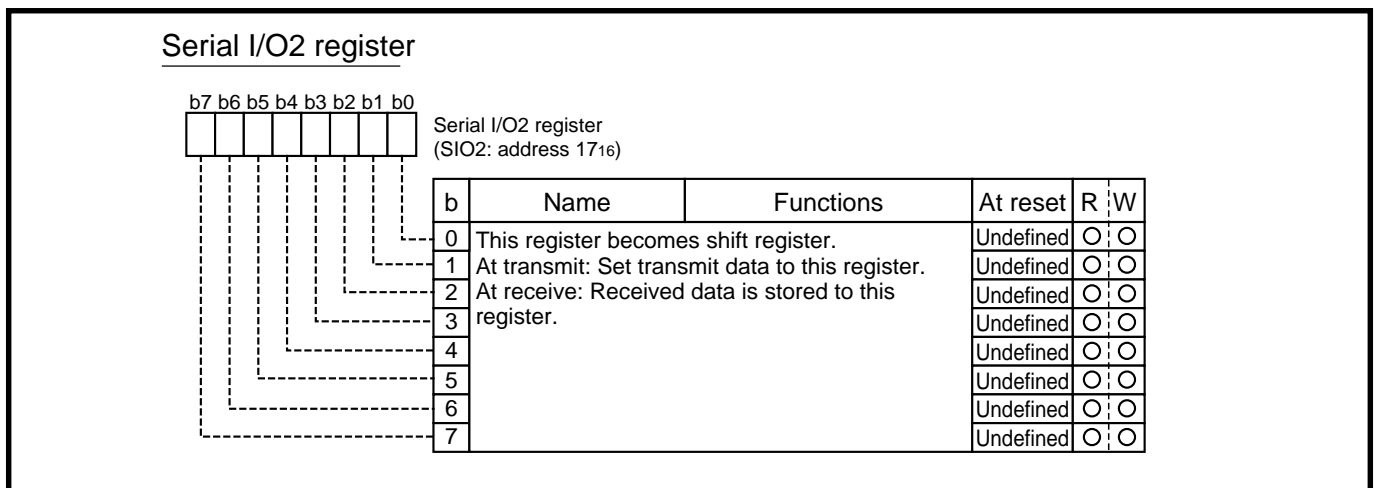


Fig. 4.8 Structure of Serial I/O2 register

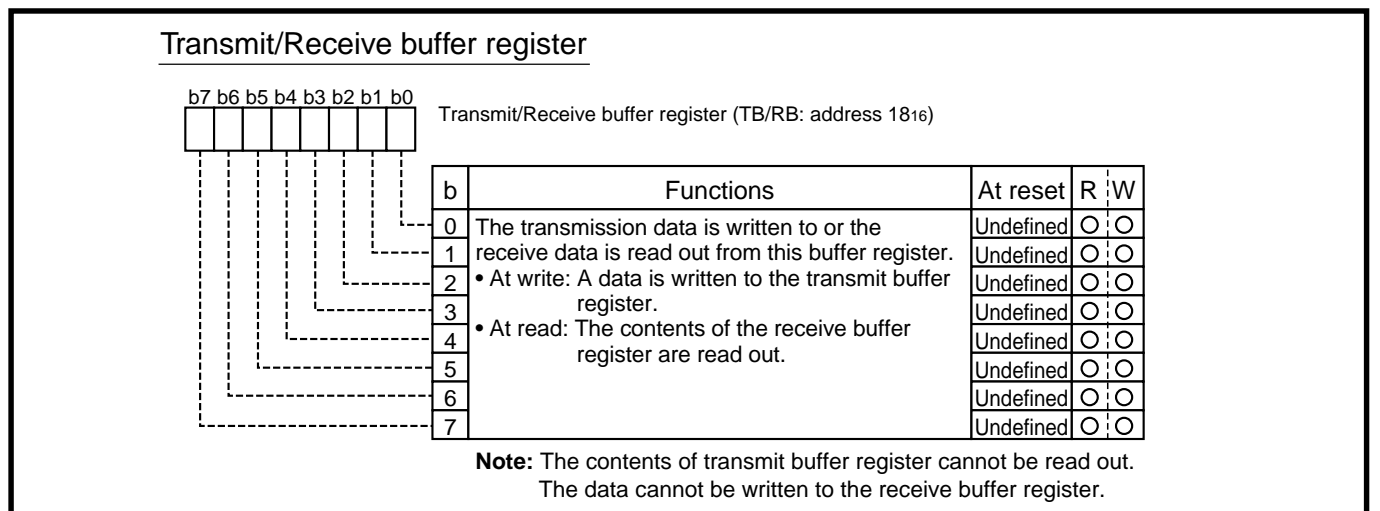


Fig. 4.9 Structure of Transmit/Receive buffer register

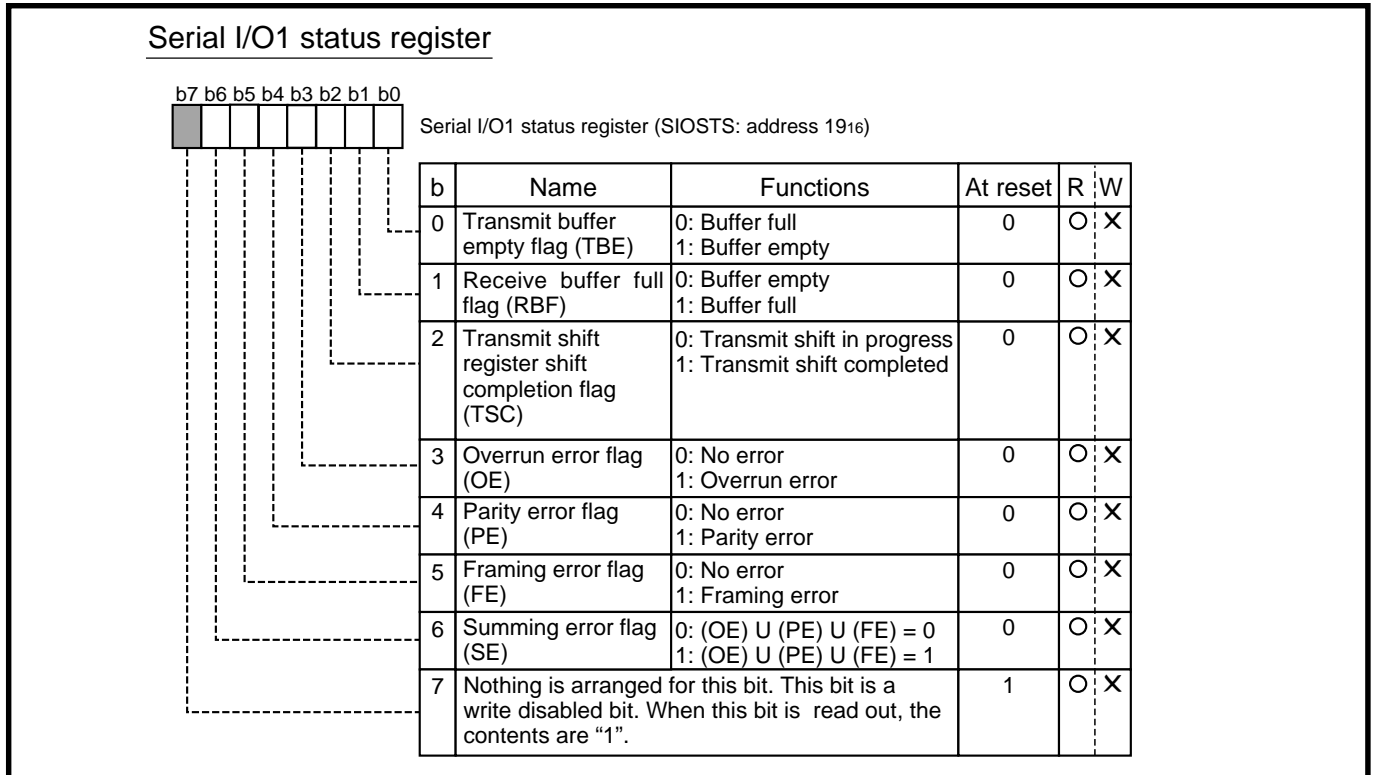


Fig. 4.10 Structure of Serial I/O1 status register

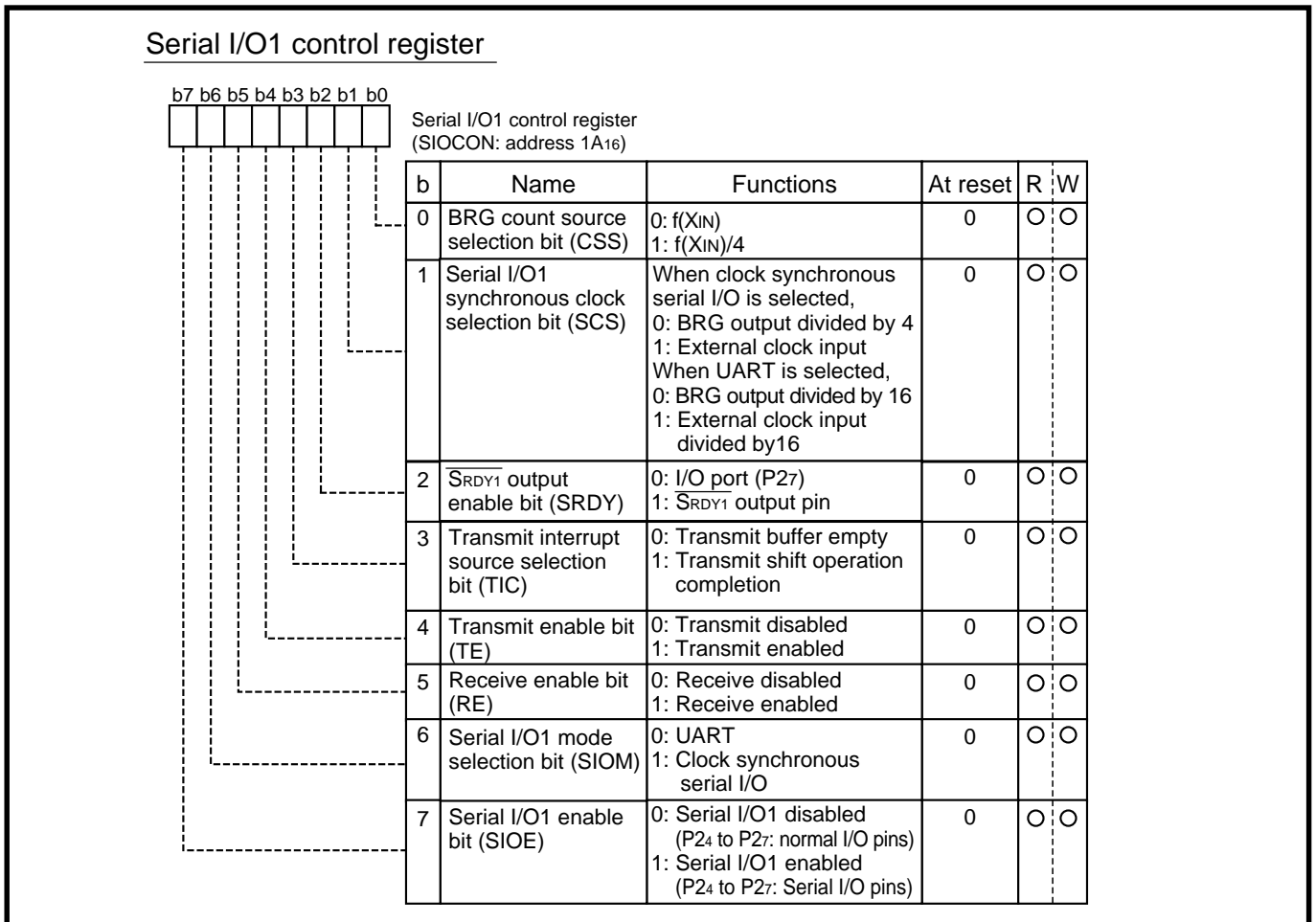


Fig. 4.11 Structure of Serial I/O1 control register



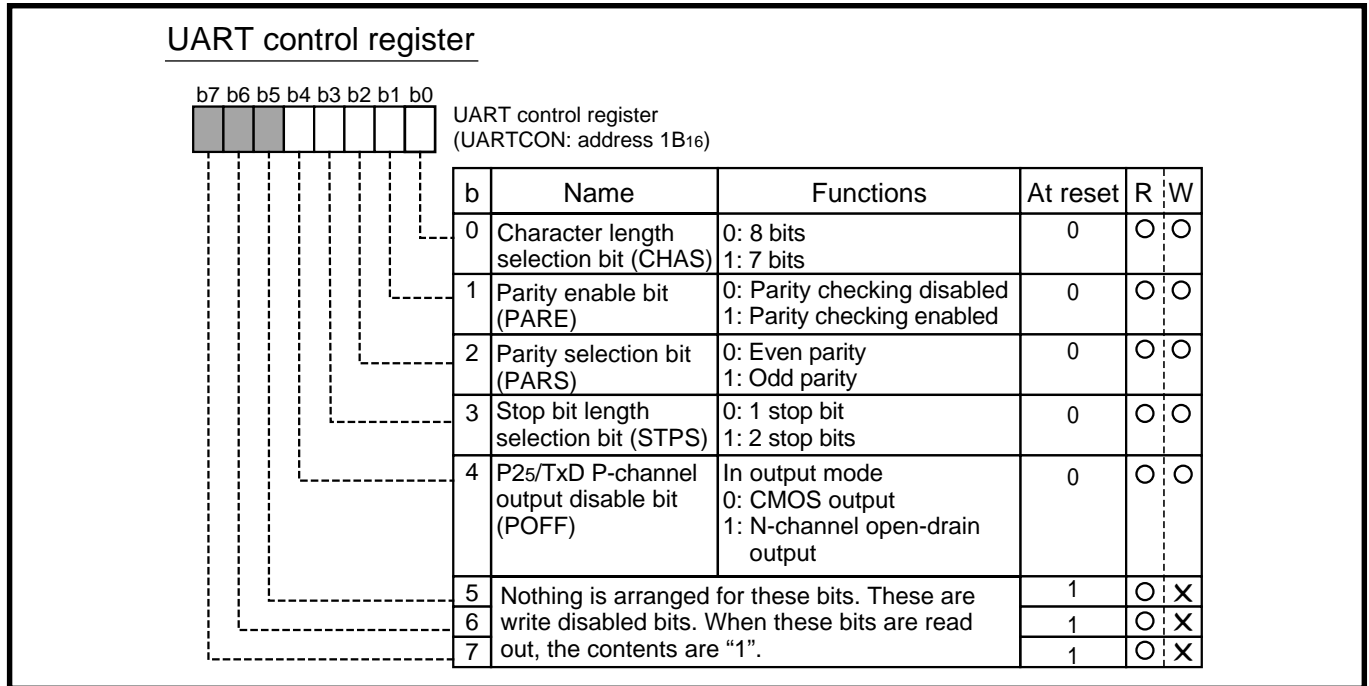


Fig. 4.12 Structure of UART control register

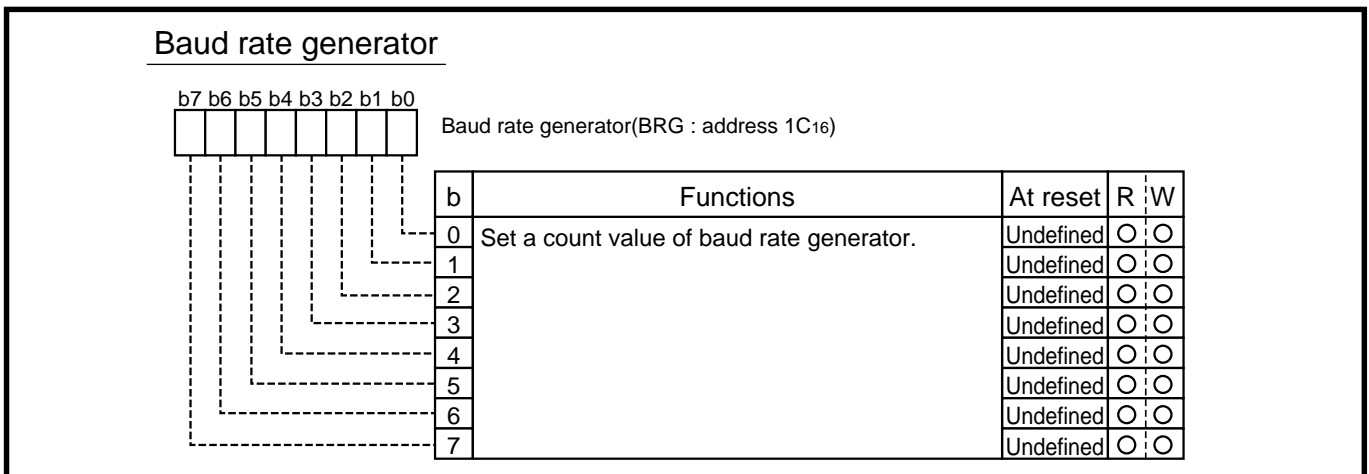


Fig. 4.13 Structure of Baud rate generator

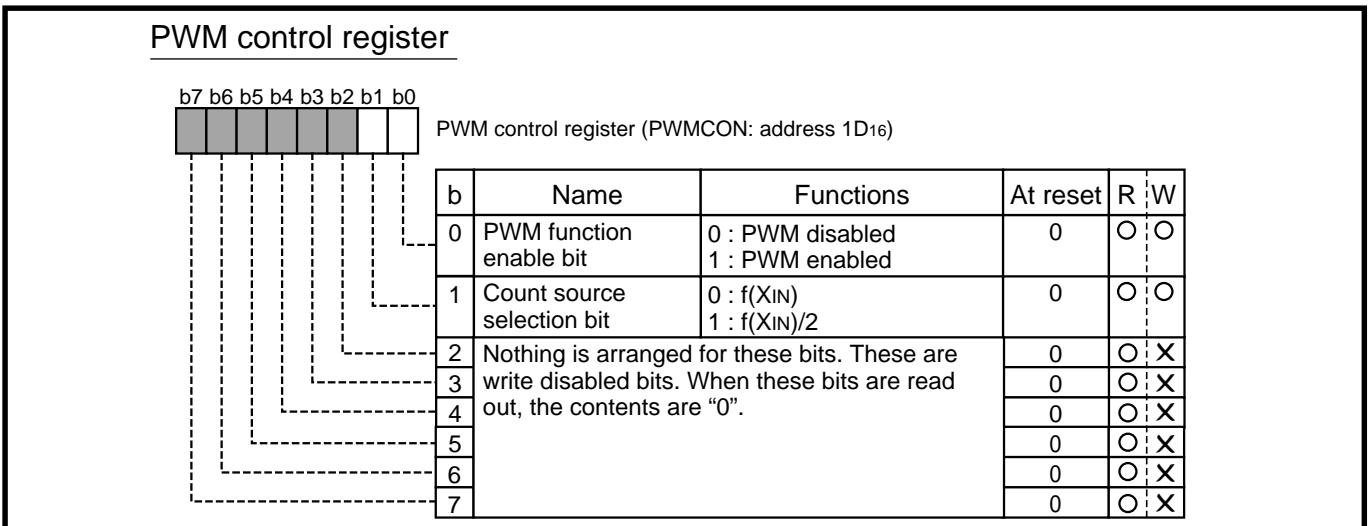


Fig. 4.14 Structure of PWM control register

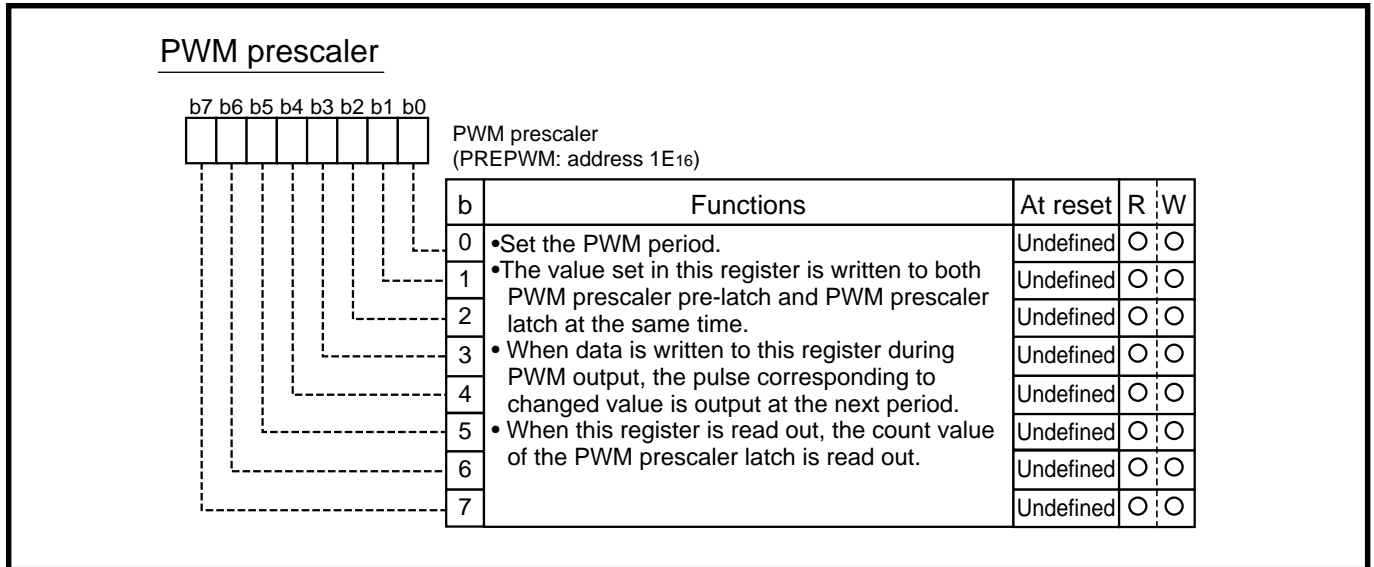


Fig. 4.15 Structure of PWM prescaler

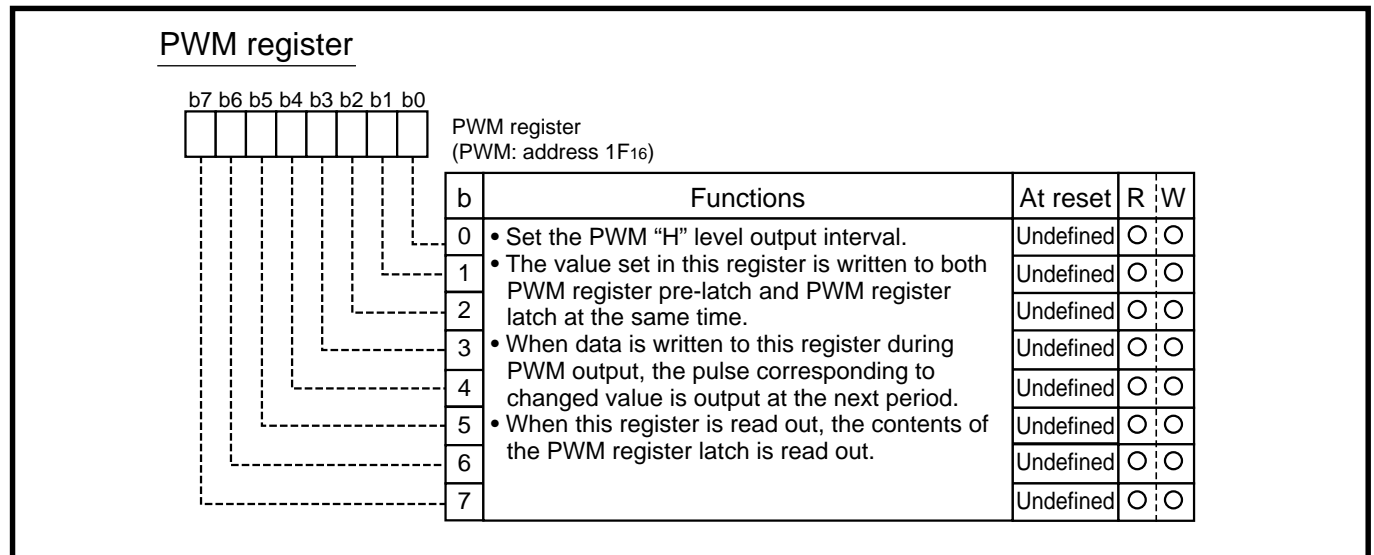


Fig. 4.16 Structure of PWM register

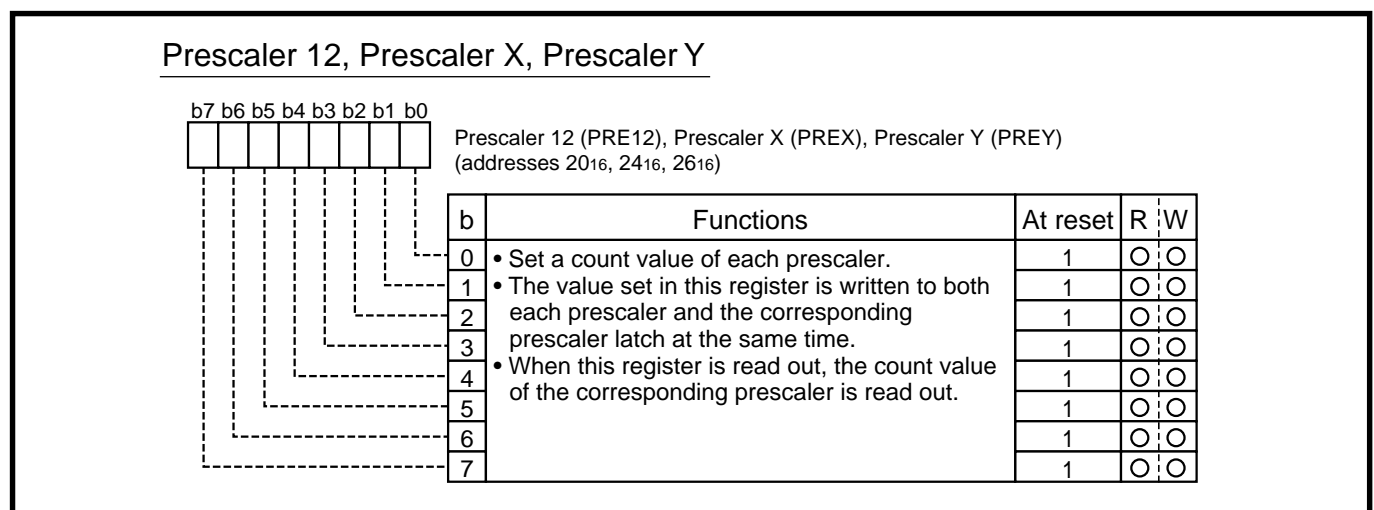


Fig. 4.17 Structure of Prescaler 12, Prescaler X, Prescaler Y

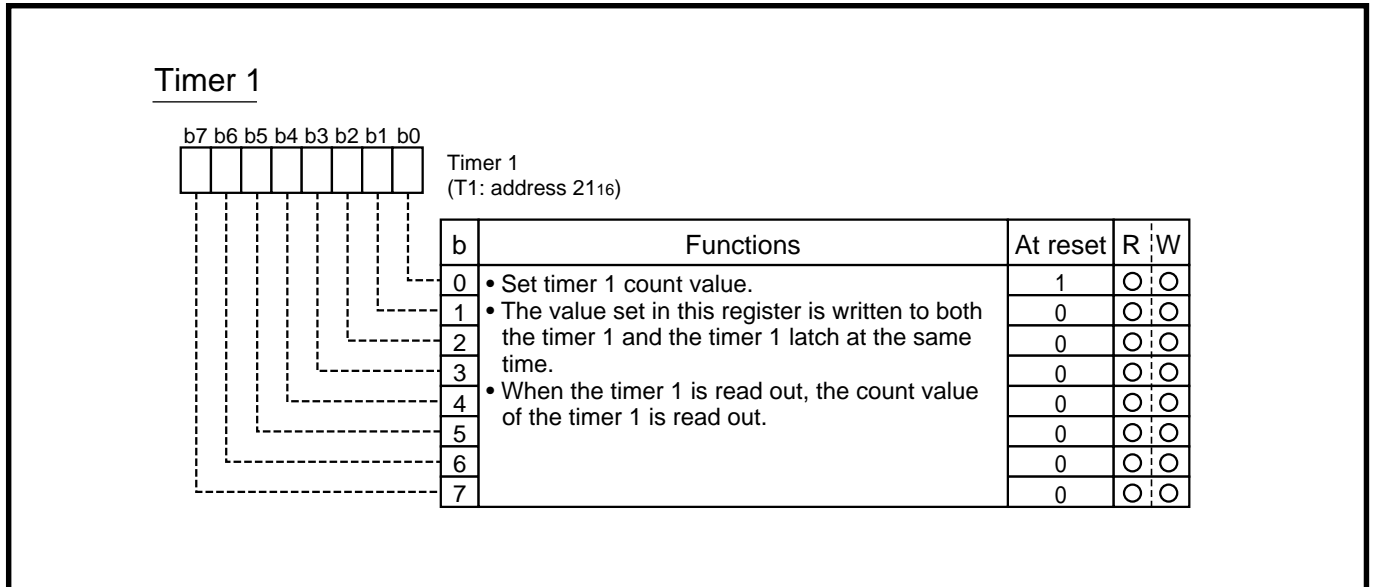


Fig. 4.18 Structure of Timer 1

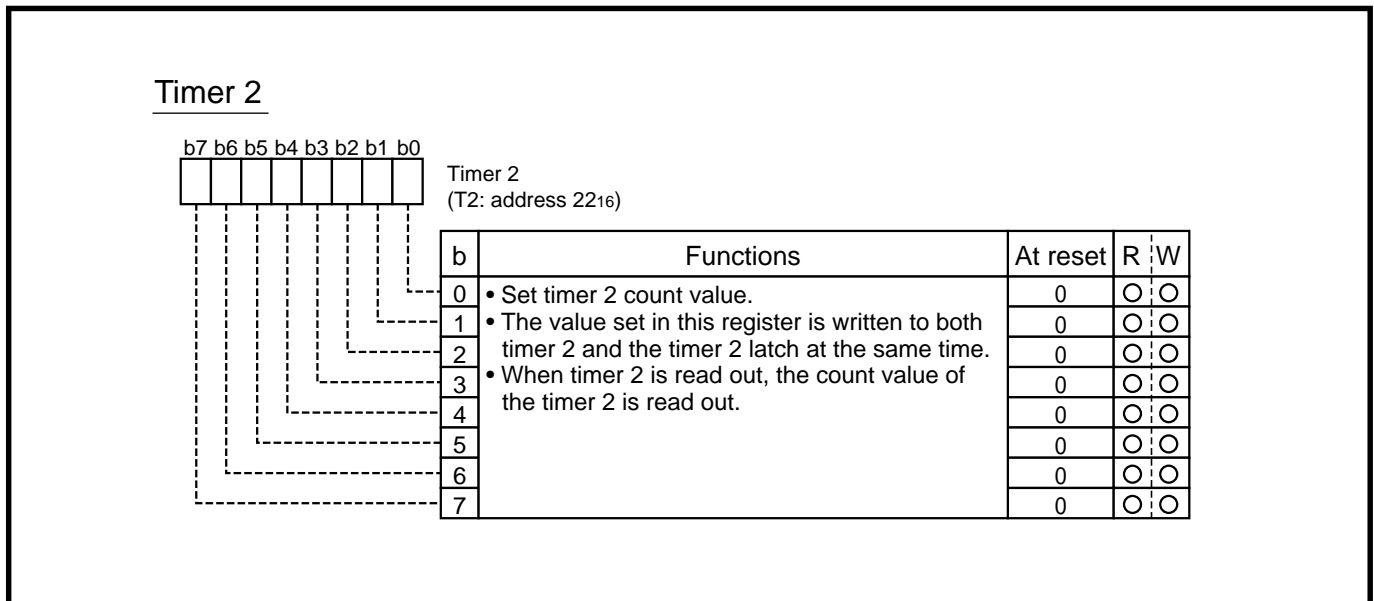


Fig. 4.19 Structure of Timer 2

Timer XY mode register

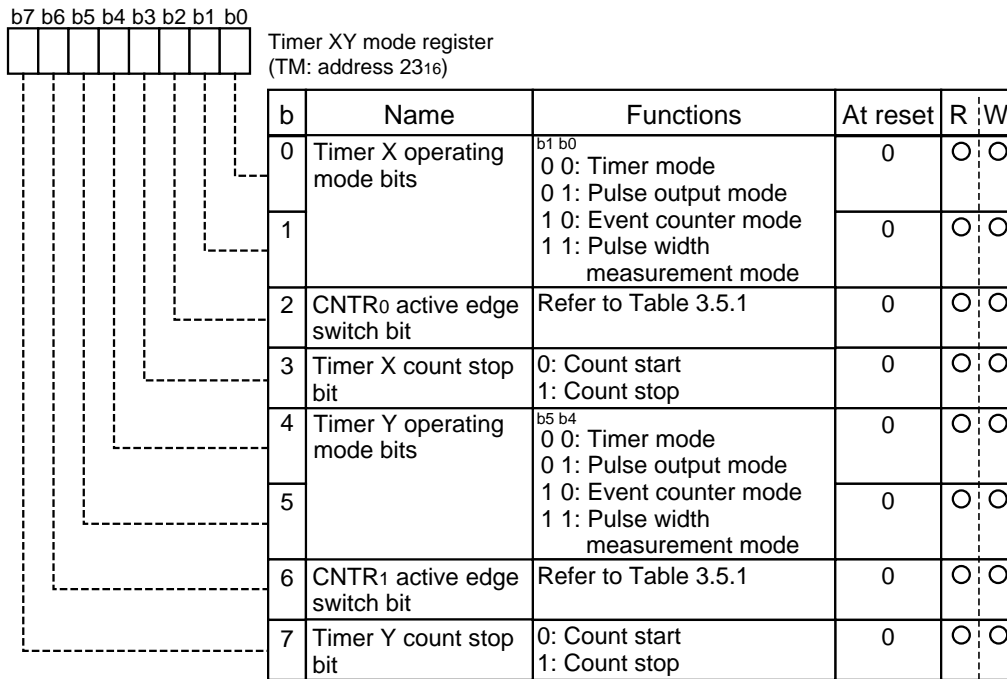


Fig. 4.20 Structure of Timer XY mode register

Table 4.1 CNTR<sub>0</sub>/CNTR<sub>1</sub> active edge switch bit function

Timer X /Timer Y operation modes	Set value	Timer function	CNTR <sub>0</sub> / CNTR <sub>1</sub> interrupt request occurrence source
Timer mode	“0”	No influence to timer count	CNTR <sub>0</sub> /CNTR <sub>1</sub> input signal falling edge
	“1”	No influence to timer count	CNTR <sub>0</sub> /CNTR <sub>1</sub> input signal rising edge
Pulse output mode	“0”	Pulse output start: Beginning at “H” level	Output signal falling edge count
	“1”	Pulse output start: Beginning at “L” level	Output signal rising edge count
Event counter mode	“0”	Rising edge count	Input signal falling edge count
	“1”	Falling edge count	Input signal rising edge count
Pulse width measurement mode	“0”	“H” level width measurement	Input signal falling edge count
	“1”	“L” level width measurement	Input signal rising edge count

Timer X, Timer Y

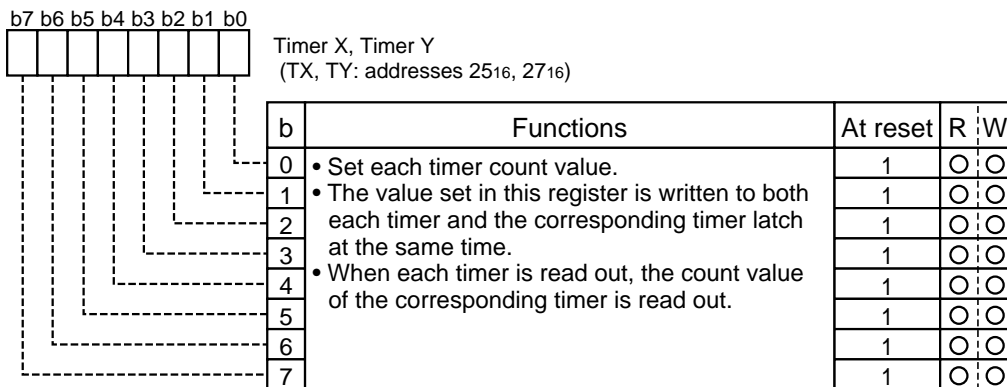


Fig. 4.21 Structure of Timer X, Timer Y

Timer count source selection register

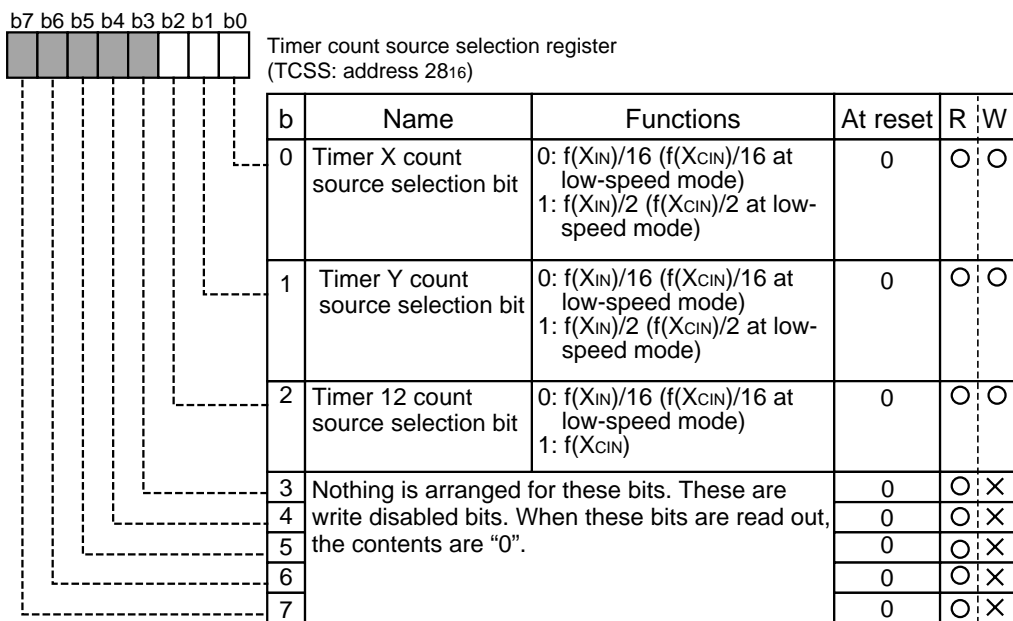


Fig. 4.22 Structure of Timer count source selection register

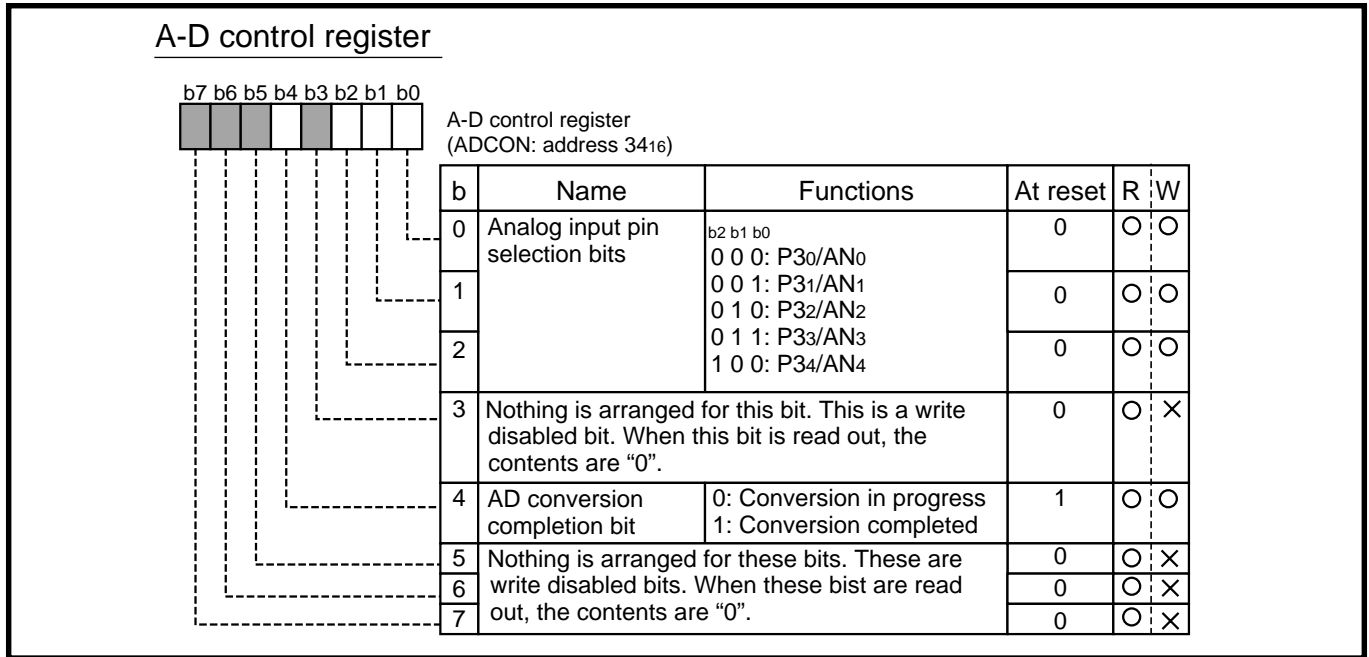


Fig. 4.23 Structure of A-D control register

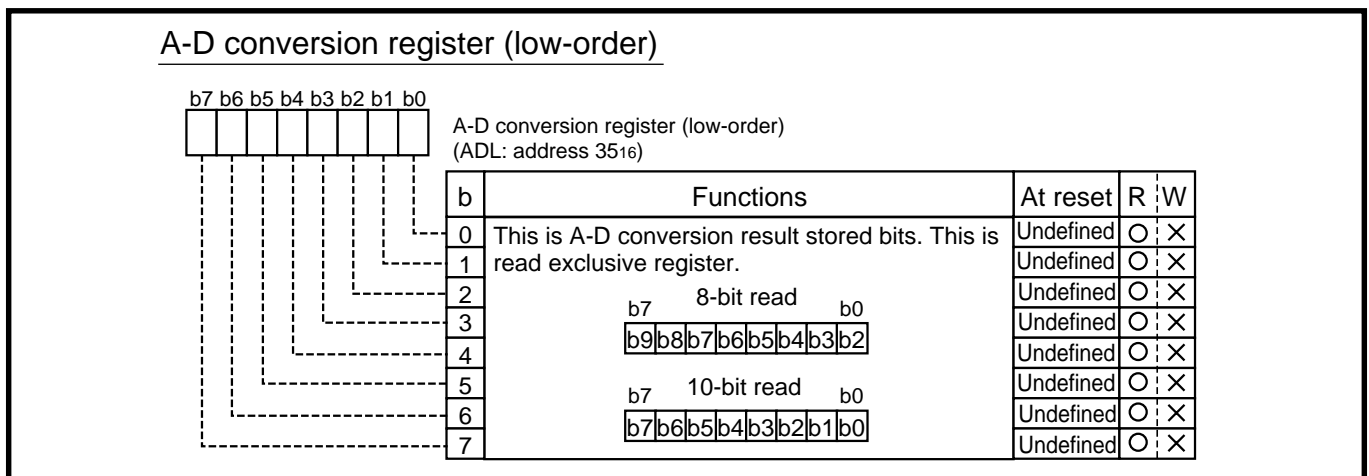


Fig. 4.24 Structure of A-D conversion low-order register

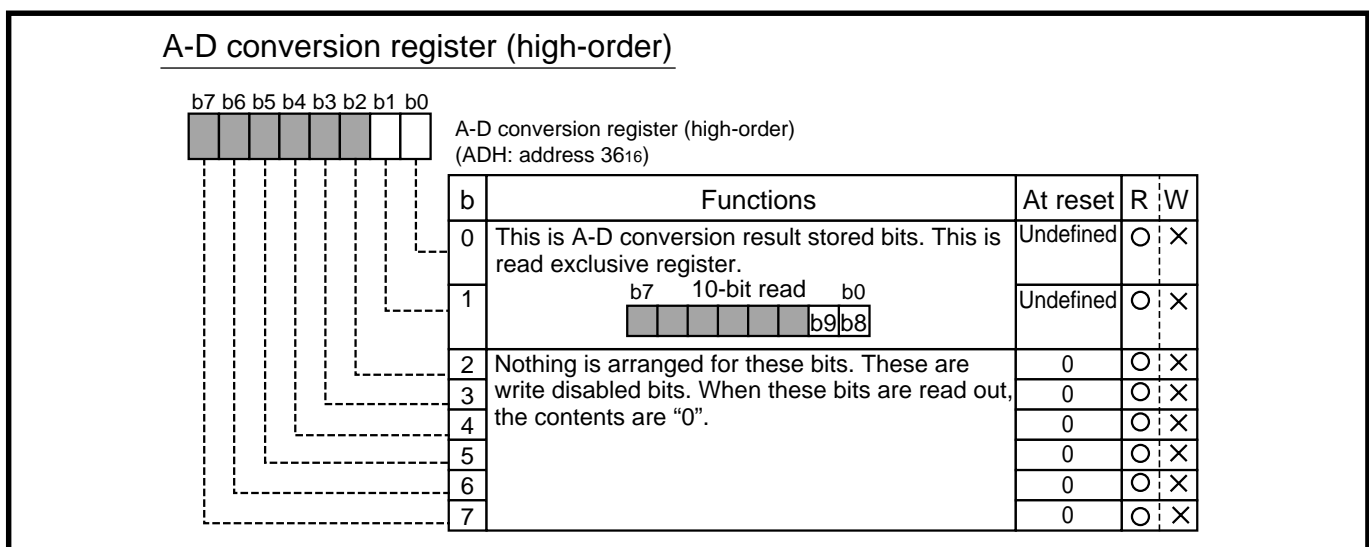


Fig. 4.25 Structure of A-D conversion high-order register

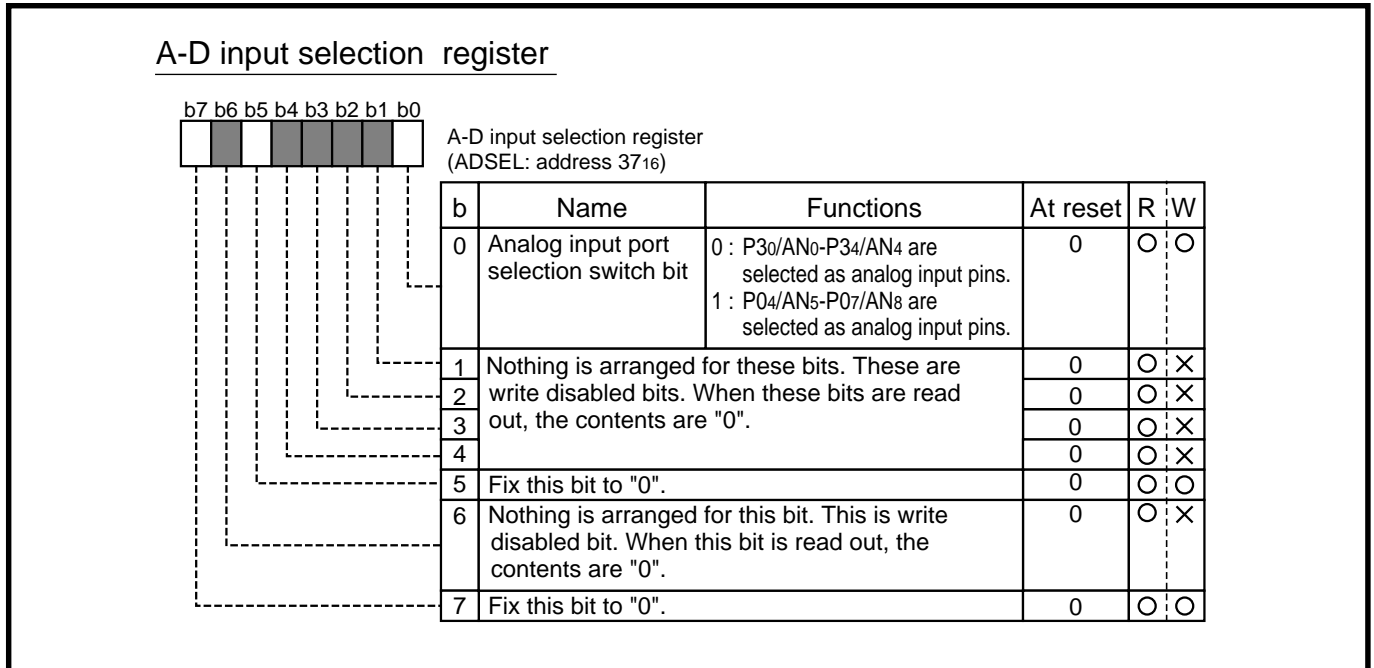


Fig. 4.26 Structure of A-D input selection register

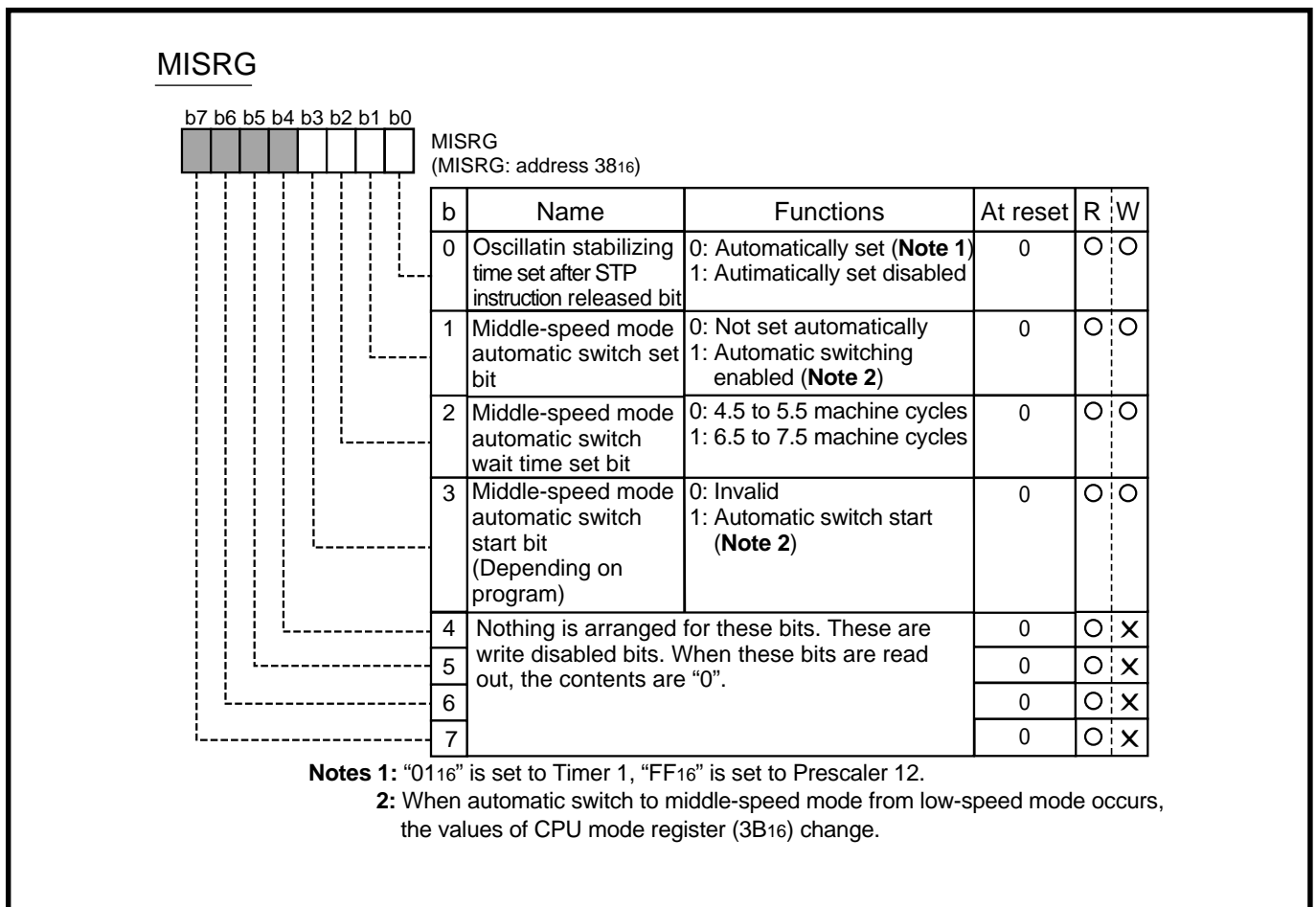


Fig. 4.27 Structure of MISRG

Watchdog timer control register

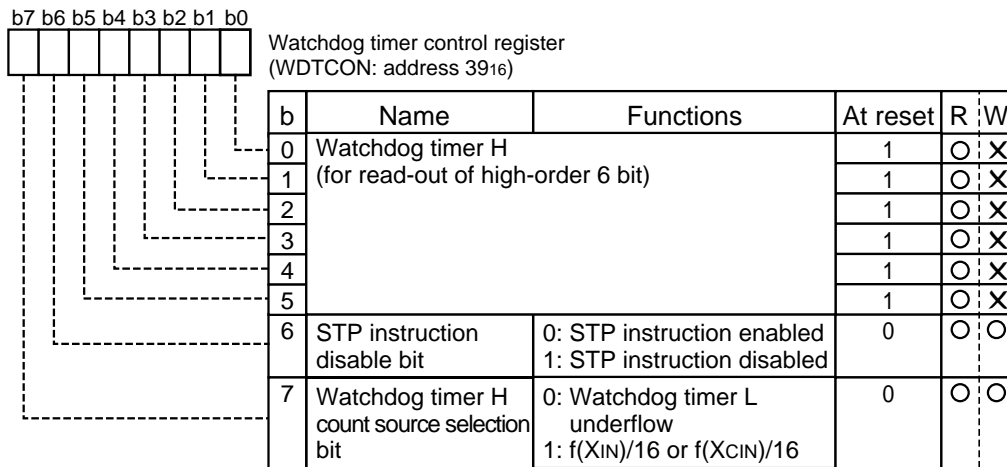


Fig. 4.28 Structure of Watchdog timer control register

Interrupt edge selection register

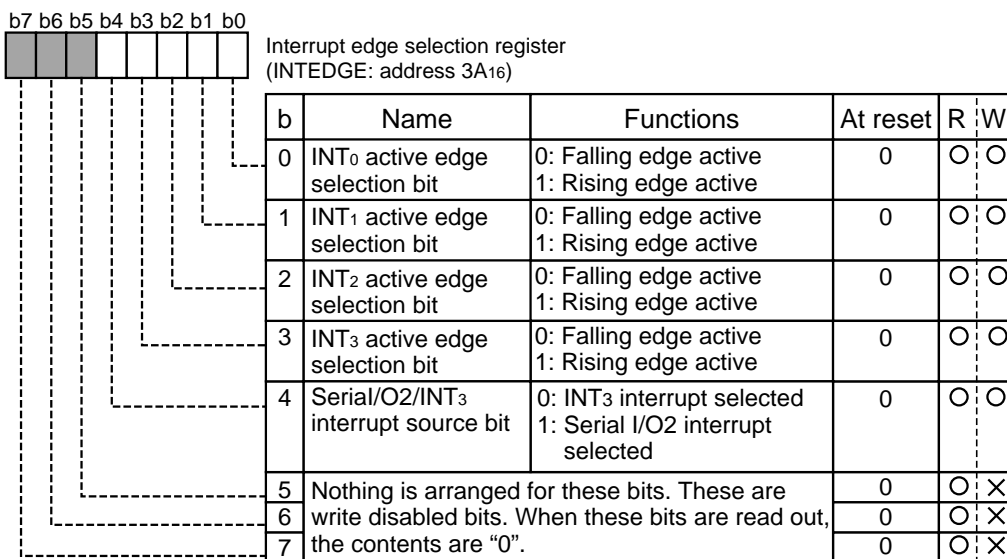


Fig. 4.29 Structure of Interrupt edge selection register



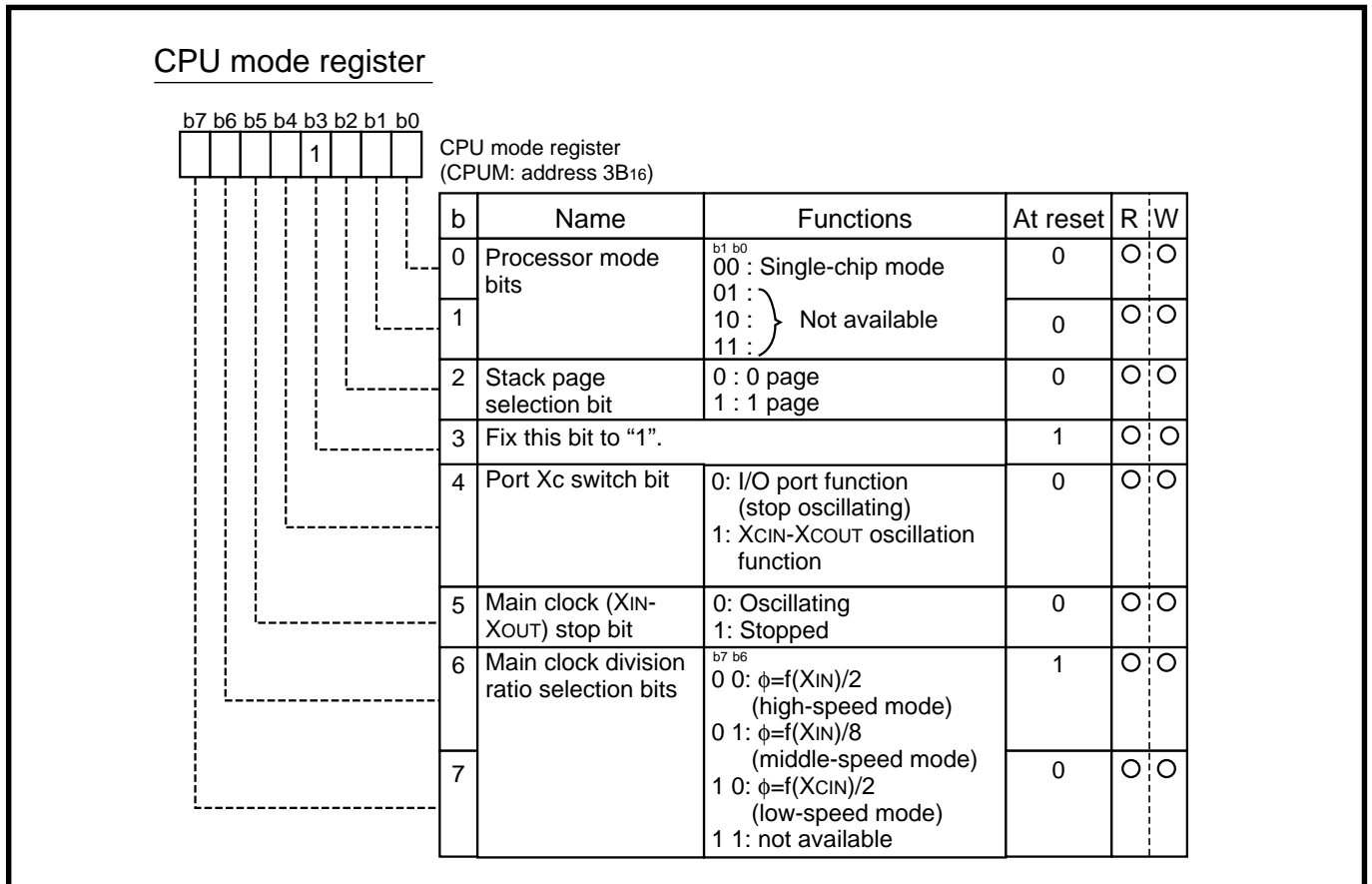


Fig. 4.30 Structure of CPU mode register

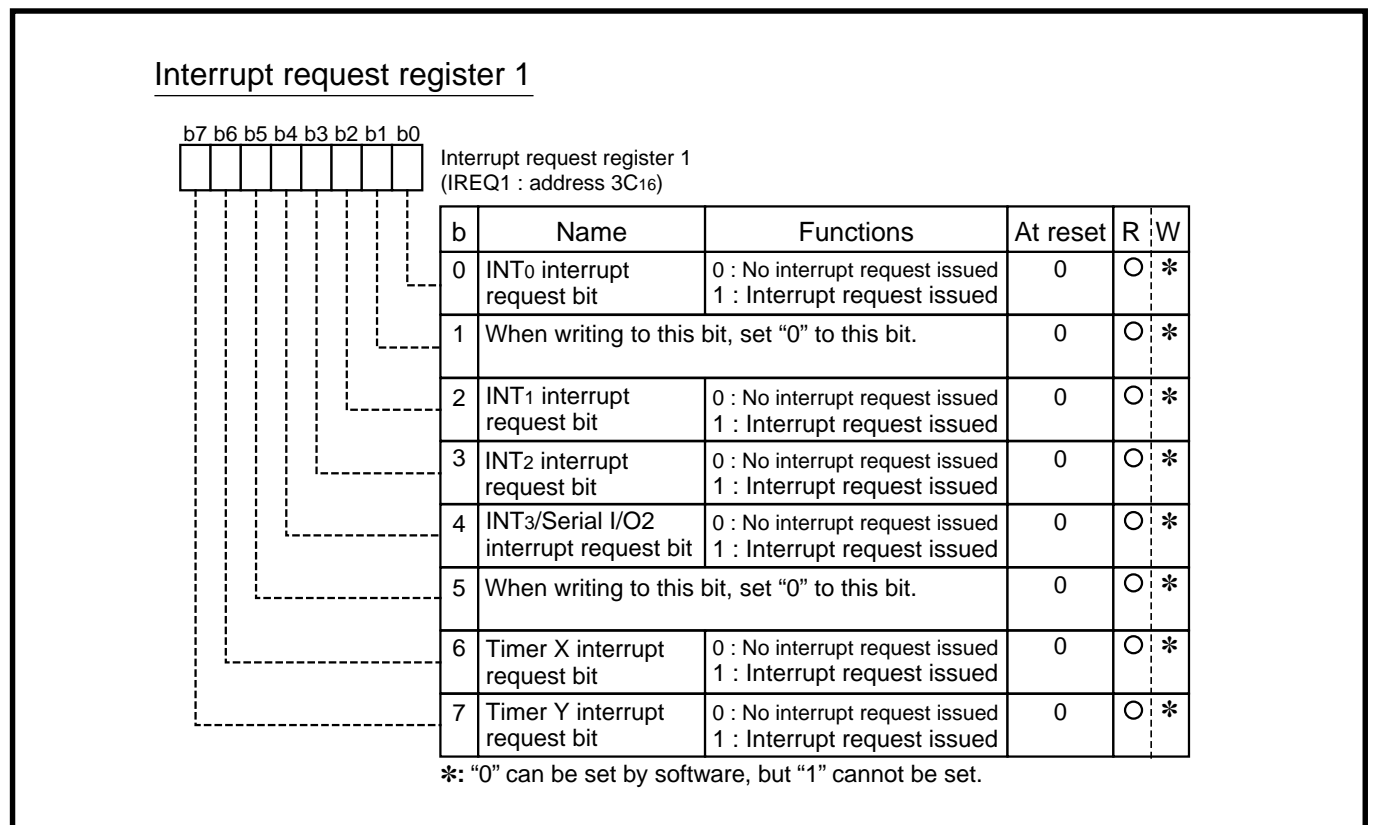


Fig. 4.31 Structure of Interrupt request register 1

Interrupt request register 2

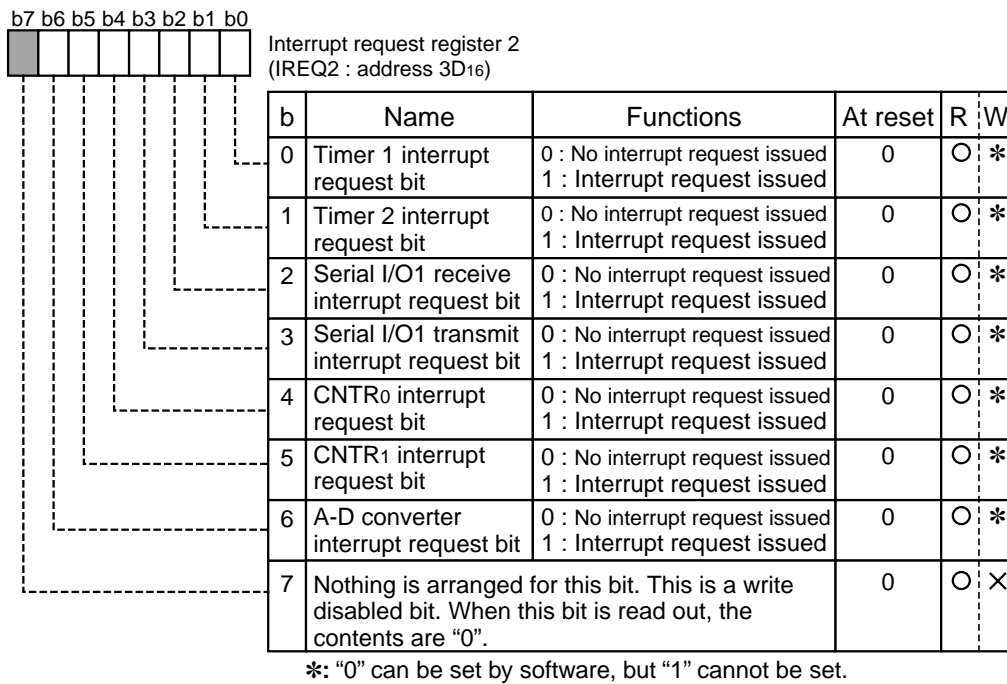


Fig. 4.32 Structure of Interrupt request register 2

Interrupt control register 1

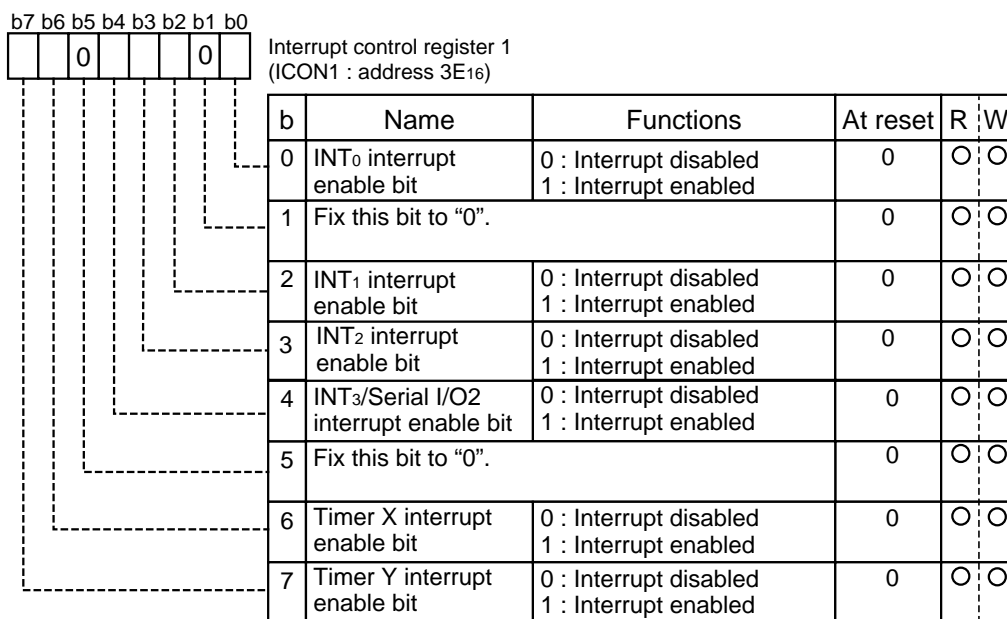


Fig. 4.33 Structure of Interrupt control register 1

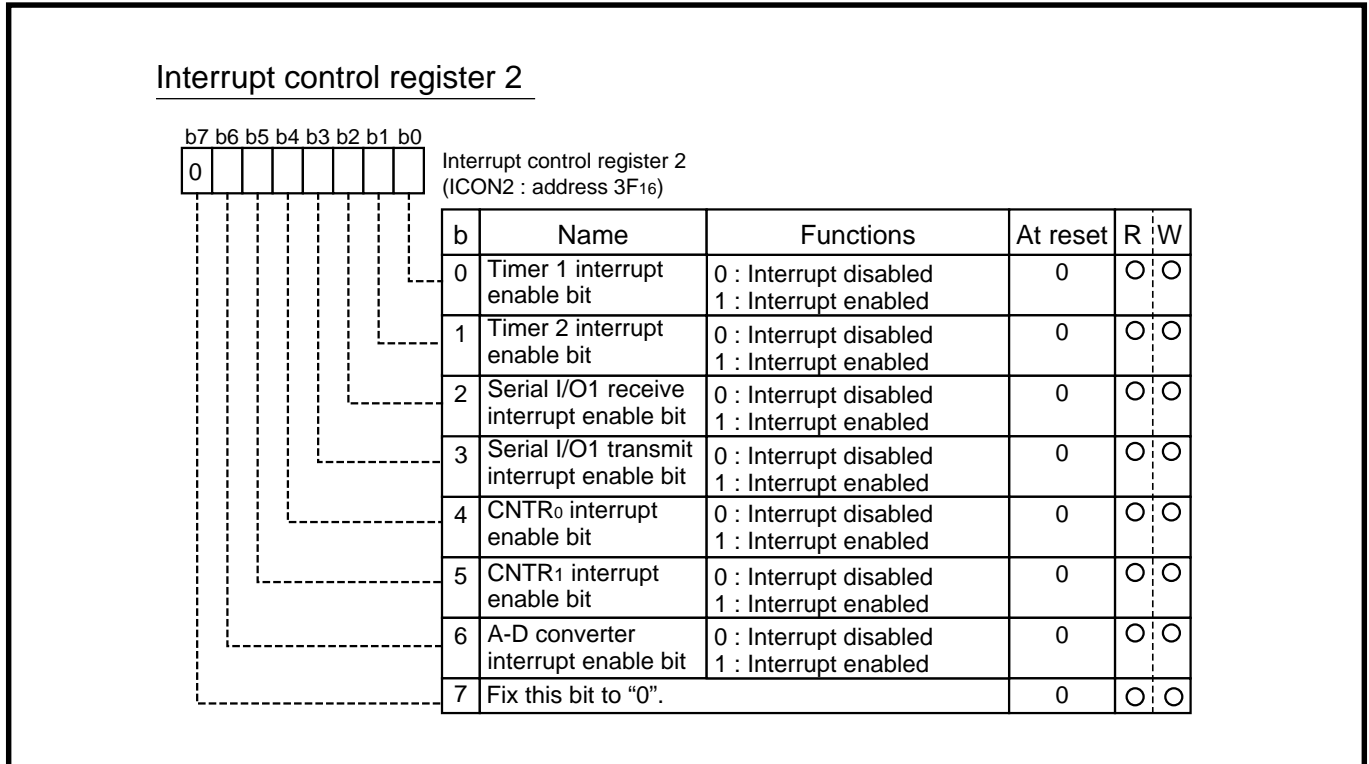


Fig. 4.34 Structure of Interrupt control register 2

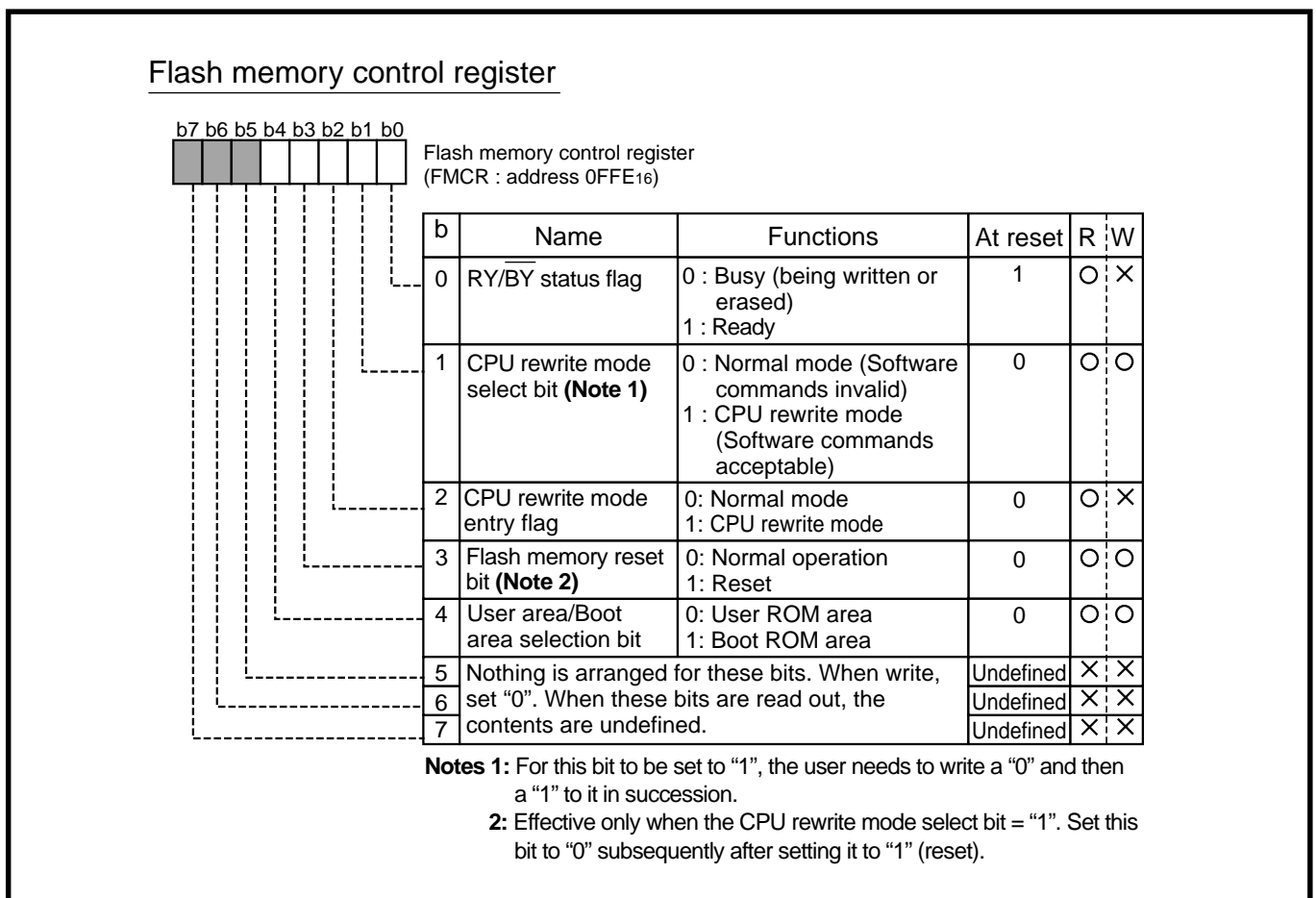


Fig. 4.35 Structure of Flash memory control register (Flash memory version only)

## 5. Reference Program Example

Please find the reference program on the Renesas Technology website.  
Click the upper left menu of the screen "Application Notes" on the 740 family.

## 6. Reference

Data Sheet  
3850 Group (Spec.A) Data Sheet

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REVISION HISTORY	3850 Group (Spec.A) List of registers
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Rev.	Date	Description	
		Page	Summary
1.00	Nov 14, 2005	-	This application note is issued using the information of "Chapter 3.5 List of registers" in the 3850 Group (Spec.A) User's Manual Rev.1.00.

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