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Serial I/O (Clock Synchronous Serial I/O Mode: Example 1)

#### 1. Abstract

The following article introduces and shows an example of how to use the Serial I/O (Clock Synchronous Serial I/O Mode: Example 1) on the 3823 group device.

### 2. Introduction

The explanation of this issue is applied to the following conditions:

Applicable MCU: 3823 Group Oscillation frequency: 4 MHz

This sample program may include operations of unused bit functions for the convenience of the SFR bit layout. Set the values according to the operational conditions of the user system.

#### 3. Contents

## 3.1 Communication Using Clock Synchronous Serial I/O (Transmit/Receive)

Outline: 2-byte data is transmitted and received, using the clock synchronous serial I/O.

SRDY signal is used for communication control.

Specifications:

- •Serial I/O is used (clock synchronous serial I/O mode is selected).
- •Synchronous clock frequency: 125kHz (f(XIN) = 4MHz is divided by 32)
- •SRDY signal (receivable signal) is used.
- •The receiving side outputs the SRDY signal at intervals of 2 ms (generated by the timer), and 2-byte data is received.
- •The transmitting side confirms the SRDY signal by INT1 interrupt request and transmits 2-byte data.

Figure 3.1 shows the Connection Diagram, Figure 3.2 shows the Timing Chart, Figure 3.3 shows the Register Settings Relevant to the Transmitting Side, Figure 3.4 shows the Register Settings Relevant to the Receiving Side, Figure 3.5 shows the Control Procedure of Transmitting Side, and Figure 3.6 shows the Control Procedure of Receiving Side.

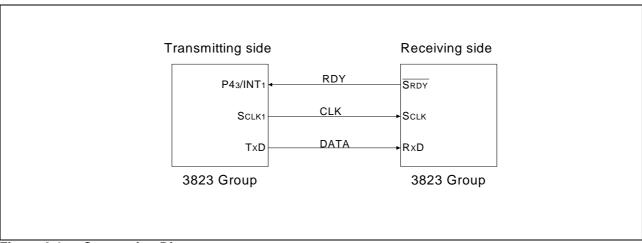


Figure 3.1 Connection Diagram

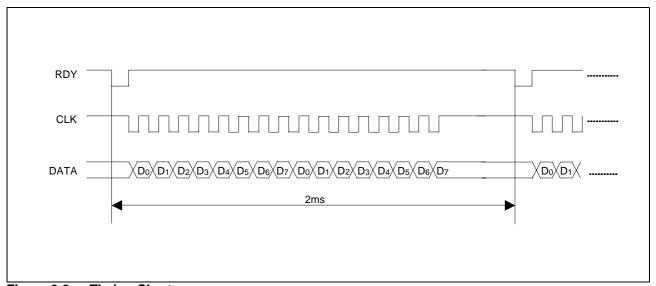
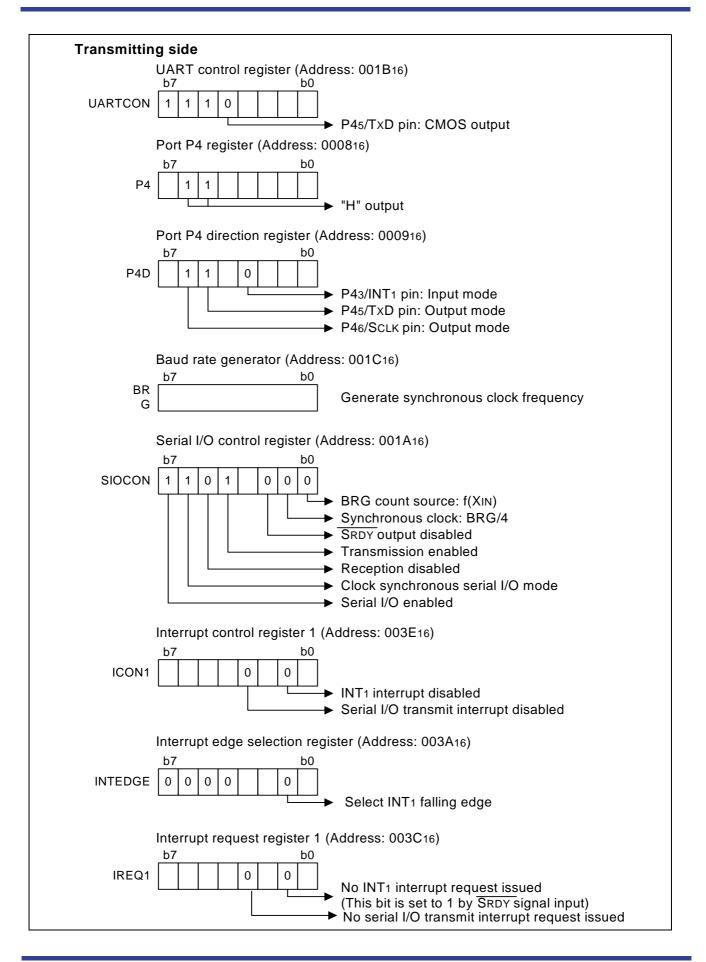


Figure 3.2 Timing Chart



Transmit buffer register (Address: 001816) b0 Write transmission data after confirming TB the previous data transmission is completed (TSC = 1) Serial I/O status register (Address: 001916) SIOSTS Transmit buffer empty flag (TBE) Confirm data transfer from transmit buffer register to transmit shift register • When this bit is set to 1, the next transmission data writing to transmit buffer register is enabled Transmit shift register completion flag (TSC) Confirm 1-byte data transmission is completed • 1: Transmit shift completed

Figure 3.3 Register Settings Relevant to the Transmitting Side

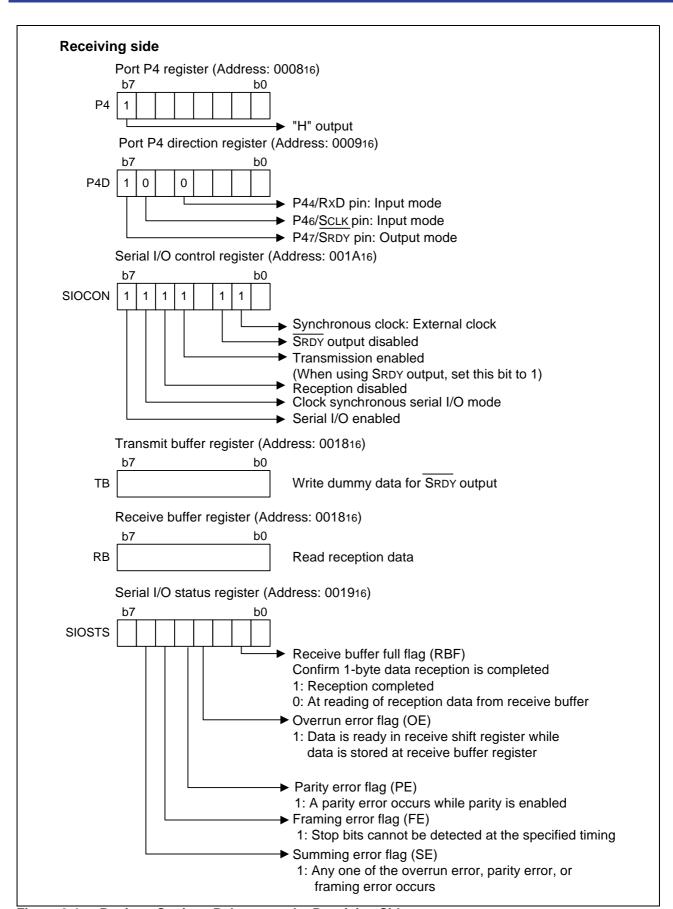


Figure 3.4 Register Settings Relevant to the Receiving Side



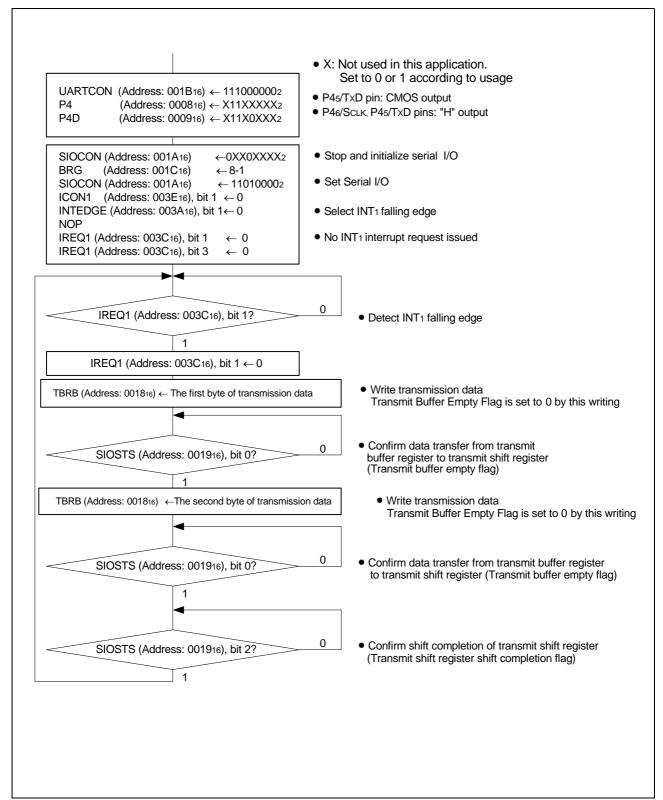


Figure 3.5 **Control Procedure of Transmitting Side** 



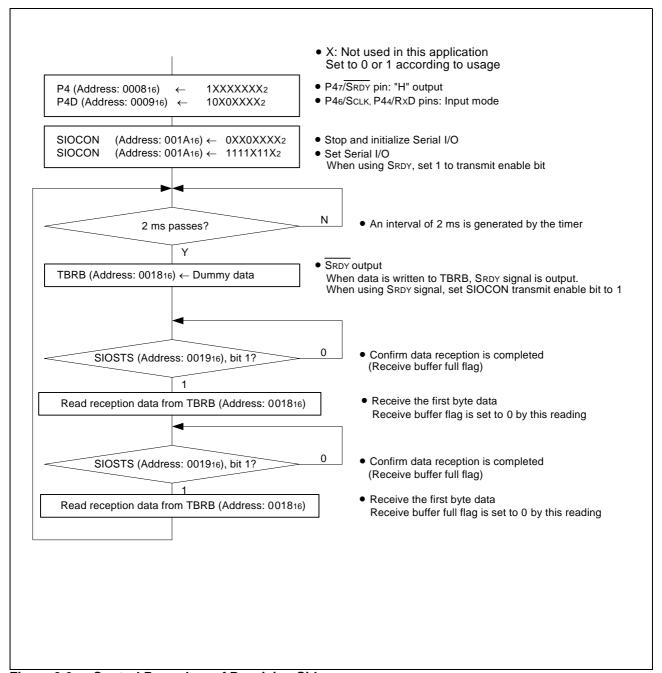


Figure 3.6 **Control Procedure of Receiving Side** 

## 4. Sample Programming Code

Download a sample program from the Renesas Technology website. To download, click "Application Notes" in the left side menu on the page of the 3823 Group.

#### 5. Reference Document

Datasheet

3823 Group Data sheet

Download the latest version from the Renesas Technology website.

Technical News/Technical Update

Download the latest information from the Renesas Technology website.

## 6. Website and Support

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REVISION HISTORY	3823 Group Serial I/O (Clock Synchronous Serial I/O Mode:
	Example 1)

Rev.	Date	Description	
		Page	Summary
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