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# 3823 Group

## Serial I/O (Clock Asynchronous Serial I/O (UART) Mode)

## 1. Abstract

The following article introduces and shows an example of how to use the Serial I/O (Clock Asynchronous Serial I/O (UART) Mode) on the 3823 group device.

## 2. Introduction

The explanation of this issue is applied to the following conditions:

Applicable MCU: 3823 Group Oscillation frequency: 4.9152 MHz

This sample program may include operations of unused bit functions for the convenience of the SFR bit layout. Set the values according to the operational conditions of the user system.



#### 3. Contents

## 3.1 Communication Using Asynchronous Serial I/O (UART) (Transmit/Receive)

Outline: 2-byte data is transmitted and received using UART

Port P41 is used for communication control

Specifications:

- •Serial I/O (UART mode) is used.
- •Transfer bit rate: 9600 bps (f(XIN) = 4.9152 MHz divided by 512)
- •Communication is controlled by port P41 (output level of P41 is controlled by a program).
- •2-byte data is transferred from the transmitting side to the receiving side at 10 ms intervals (generated by a timer).

Figure 3.1 shows the Connection Diagram and Figure 3.2 shows the Timing Chart

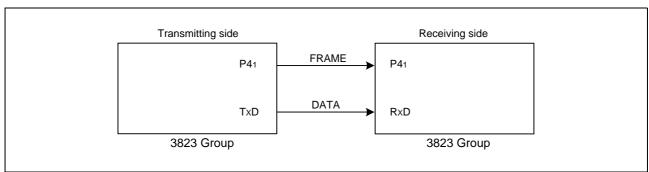


Figure 3.1 Connection Diagram

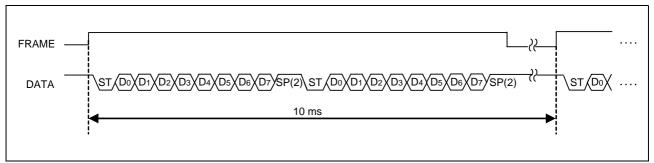


Figure 3.2 Timing Chart



Table 3.1 lists an Example of Baud Rate Generator Set Value and Transfer Bit Rate Selection, Figure 3.3 shows the Transmission Related Register Settings, Figure 3.4 shows the Reception Related Register Settings, Figure 3.5 shows the Transmitting Side Control Procedure, and Figure 3.6 shows the Receiving Side Control Procedure.

Table 3.1 Example of Baud Rate Generator Set Value and Transfer Bit Rate Selection

BRG Count Source (Note 1)	BRG Setting Value	Transfer Bit Rate (bps) (Note 2)	
		f(XIN) = 4.9152MHz	f(XIN) = 8MHz
f(XIN)/4	255(FF16)	300	488.28125
f(XIN)/4	127(7F <sub>16</sub> )	600	976.5625
f(XIN)/4	63(3F16)	1200	1953.125
f(XIN)/4	31(1F16)	2400	3906.25
f(XIN)/4	15(0F16)	4800	7812.5
f(XIN)/4	7(0716)	9600	15625
f(XIN)/4	3(0316)	19200	31250
f(XIN)/4	1(0116)	38400	62500
f(XIN)	3(0316)	76800	125000
f(XIN)	(IN) 1(0116) 153600 250000		250000
f(XIN)	0(0016)	307200	500000

#### Notes:

- 1. The BRG count source is selected by bit 0 at the serial I/O control register.
- 2. Calculating formula of the transfer bit rate

Transfer bit rate (bps) = 
$$\frac{f(XIN)}{(BRG \text{ set value} + 1) \times 16 \times m}$$

m: When bit 0 at the serial I/O control register = 0, m = 1When bit 0 at the serial I/O control register = 1, m = 4



## **Transmitting Side** Port P4 register (Address: 000816) 0 Set to 1 when transmitting data "H" output (initial state) Port P4 direction register (Address: 000916) P4D P43/INT1 pin: Output mode ▶ P45/TxD pin: Output mode Baud rate generator (Address: 001C<sub>16</sub>) Set 4.9152 x 10<sup>6</sup> -1 BRG 8-1 Serial I/O control register (Address: 001A<sub>16</sub>) SIOCON 0 0 0 1 BRG count source: f(XIN)/4 Synchronous clock: BRG/16 Transmission enabled Reception disabled **UART** mode Serial I/O enabled UART control register (Address: 001B<sub>16</sub>) UARTCON 0 0 Character length: 8 bits Parity disabled 2 stop bits P45/TxD pin: CMOS output Transmit buffer register (Address: 001816) Write transmission data **TBRB** Write data after confirming transmission of the previous data is completed (TSC = 1) Serial I/O Status Register (Address: 001916) SIOSTS Transmit buffer empty flag (TBE) • Confirm data transfer from transmit buffer register to transmit shift register • When this bit is set to 1, writing the next transmission data to transmit buffer register is enabled Transmit shift register completion flag (TSC) • Confirm 1-byte data transmission is completed • 1 : Transmit shift completed

Figure 3.3 Transmission Related Register Settings



## Receiving Side Port P4 direction register (Address: 000916) P4D 0 P41 pin: Input mode P44/RxD pin: Input mode Baud rate generator (Address: 001C<sub>16</sub>) BRG 8-1 Serial I/O control register (Address: 001A<sub>16</sub>) SIOCON 1 0 0 1 1 BRG count source: f(XIN)/4 Synchronous clock: BRG/16 Transmission disabled Reception enabled **UART** mode Serial I/O enabled UART control register (Address: 001B<sub>16</sub>) UARTCON 0 Character length: 8 bits Parity disabled 2 stop bits Serial I/O status register (Address: 001916) SIOSTS Receive buffer full flag (RBF) Confirm 1-byte data reception is completed 1: Reception completed 0: Reading reception data from receive buffer Overrun error flag (OE) 1: Data is ready in receive shift register while data is stored at receive buffer register Framing error flag (FE) 1: Stop bits cannot be detected at the specified timing Summing error flag (SE) 1: Any one of the following errors occurs: Overrun error, parity error, or framing error Receive buffer register (Address: 001816) TBRB Read reception data

Figure 3.4 Reception Related Register Settings



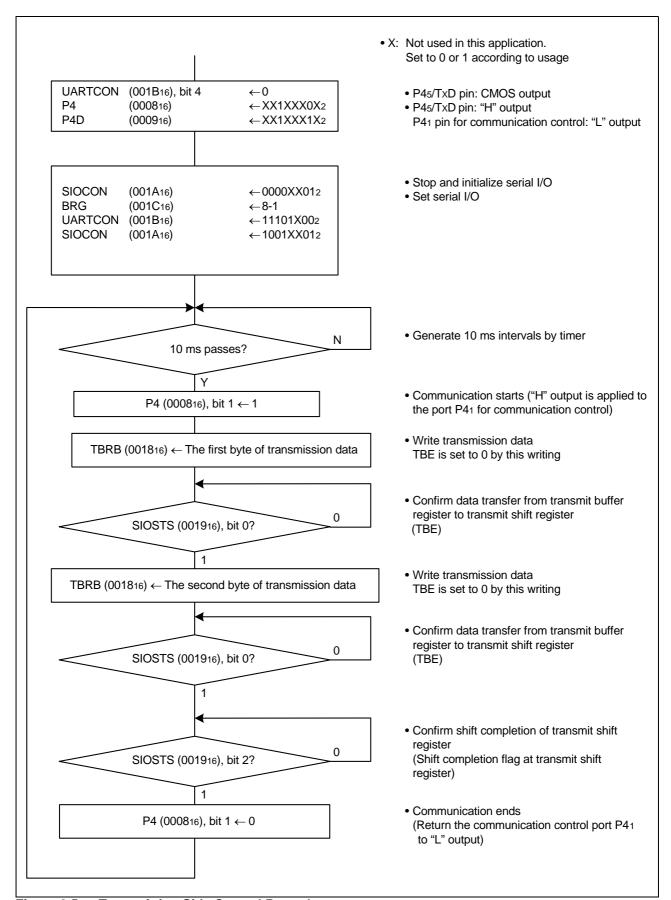


Figure 3.5 Transmitting Side Control Procedure



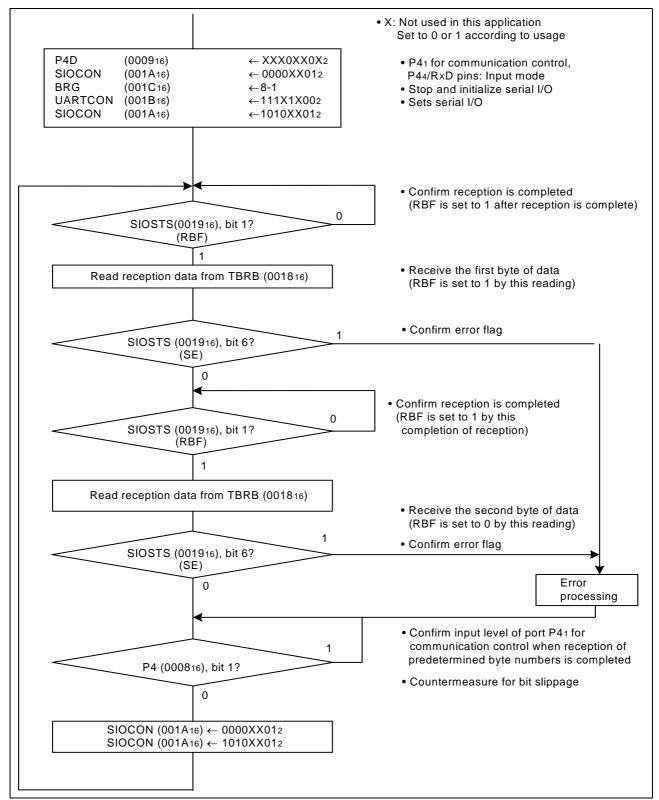


Figure 3.6 Receiving Side Control Procedure



## 4. Sample Programming Code

Download a sample program from the Renesas Technology website. To download, click "Application Notes" in the left side menu on the page of the 3823 Group.

## 5. Reference Document

Datasheet 3823 Group Data sheet

Download the latest version from the Renesas Technology website.

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REVISION HISTORY (UART) Mode)	REVISION HISTORY	3823 Group Serial I/O (Clock Asynchronous Serial I/O (UART) Mode)
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