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April 1st, 2010
Renesas Electronics Corporation

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3823 Group

ROM Correction Function

1. Abstract

The following article introduces and shows an example of how to use the ROM Correction Function on the 3823 Group device.

2. Introduction

The application explained in this document applies to the following MCU:

Applicable MCU: 3823 Group

This sample program may include operations of unused bit functions for the convenience of the SFR bit layout. Set the values according to the operational conditions of the user system.

3. Contents

3.1 ROM Correction Function

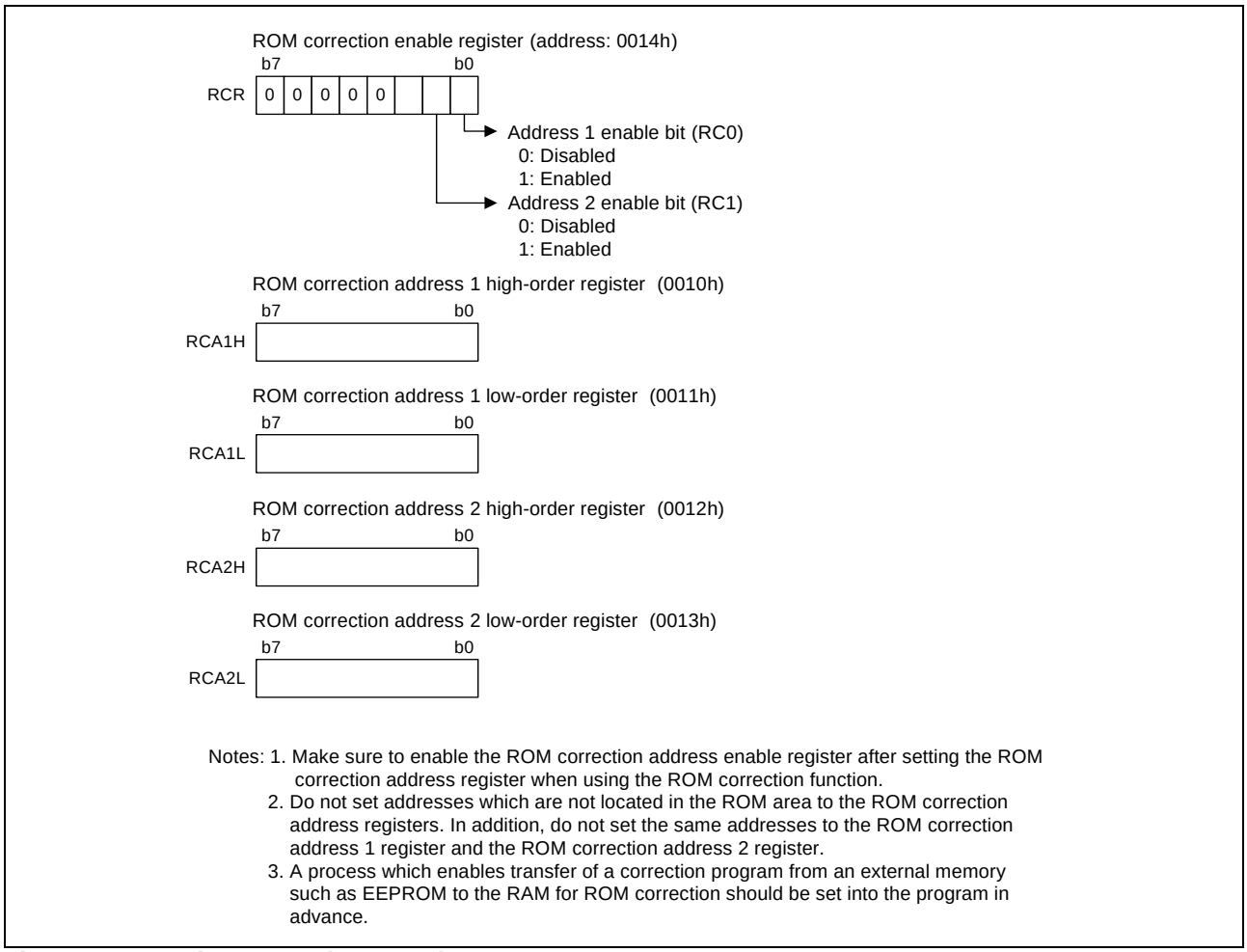
The program in the ROM can be partially corrected. Set the start address of the instruction to be corrected (Op code address of the start instruction) to the ROM correction address high-order register and low-order register. The correction program is stored in the RAM for ROM correction. When executing the program, if the value of the program counter corresponds with the value set to the ROM correction address registers, the program branches to the start address of the RAM for ROM correction and the correction program is executed. Use the JMP instruction (three-byte instruction) when returning from the correction program to the main processing.

A maximum of two parts can be corrected and two blocks can be used as the RAM for ROM correction.

	address
Block 1	0A00h
Block 2	0A20h

The ROM correction function is controlled by the ROM correction enable register.

Figure 3.1 shows the Relevant Register Settings, and Figure 3.2 shows the ROM Correction Function Operation Example (ROM correction 1).



Notes: 1. Make sure to enable the ROM correction address enable register after setting the ROM correction address register when using the ROM correction function.
2. Do not set addresses which are not located in the ROM area to the ROM correction address registers. In addition, do not set the same addresses to the ROM correction address 1 register and the ROM correction address 2 register.
3. A process which enables transfer of a correction program from an external memory such as EEPROM to the RAM for ROM correction should be set into the program in advance.

Figure 3.1 Relevant Register Settings

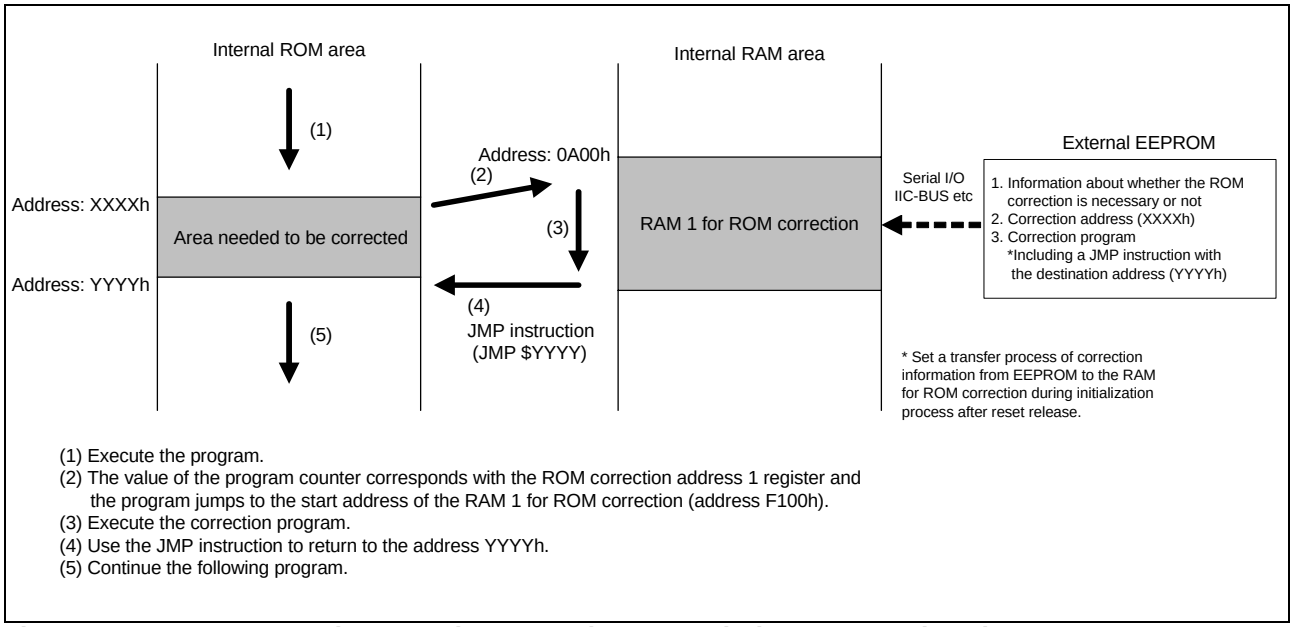


Figure 3.2 ROM Correction Function Operation Example (ROM correction 1)

3.2 Specification

The operation procedure for the ROM correction function setting is explained below.

(1) The setting process of the ROM correction function is executed as the initial setting process before executing the main processing.
(2) The ROM correction data (64 bytes) is read from EEPROM by the ROM correction program. (Valid when corresponding three times). Data read from EEPROM is stored into the RAM 1 for ROM correction (0A00h to 0A1Fh) and the RAM 2 for ROM correction (0020h to 0A3Fh). Write the OP code and the operand of the JMP instruction to return to the main processing at the end of each ROM correction program data.
(3)The set value to the ROM correction address 1, 2 registers is read from EEPROM. (Valid when corresponding three times). Data read from EEPROM is stored in the ROM correction address 1 register (0010h to 0011h) and the ROM correction address 2 register (0012h to 0013h). Conditions for ROM correction address 1, 2 register settings are as follows.
· The start address (Op code address) of each instruction is specified.
· Same addresses are not set to the ROM correction address 1 register and 2 register.
(4)The set value of the ROM correction enable register is read from EEPROM. (Valid when corresponding three times). Data read from EEPROM is set to the ROM correction enable register (0014h).
(5)After the above procedures (1) to (4) are complete, the program transfers to the main processing. (The setting process of the ROM correction function is complete).

By executing the above procedures, when the value of the program counter corresponds with the ROM correction address 1 (or 2), the program jumps to the RAM 1 (or 2) for ROM correction and the correction prgram stored in the RAM is executed. Then, by executing the JMP instruction set at the end of the correction program, the program returns to the main processing.

The jump instruction to the RAM for ROM correction is executed also in interrupt disabled (i = 1) status. In addition, note that only instructions can be corrected and others such as a data table can not be corrected by the ROM correction function.

Figure 3.3 shows the Relation between Allocation of Internal RAM for ROM Correction and ROM Correction Data.

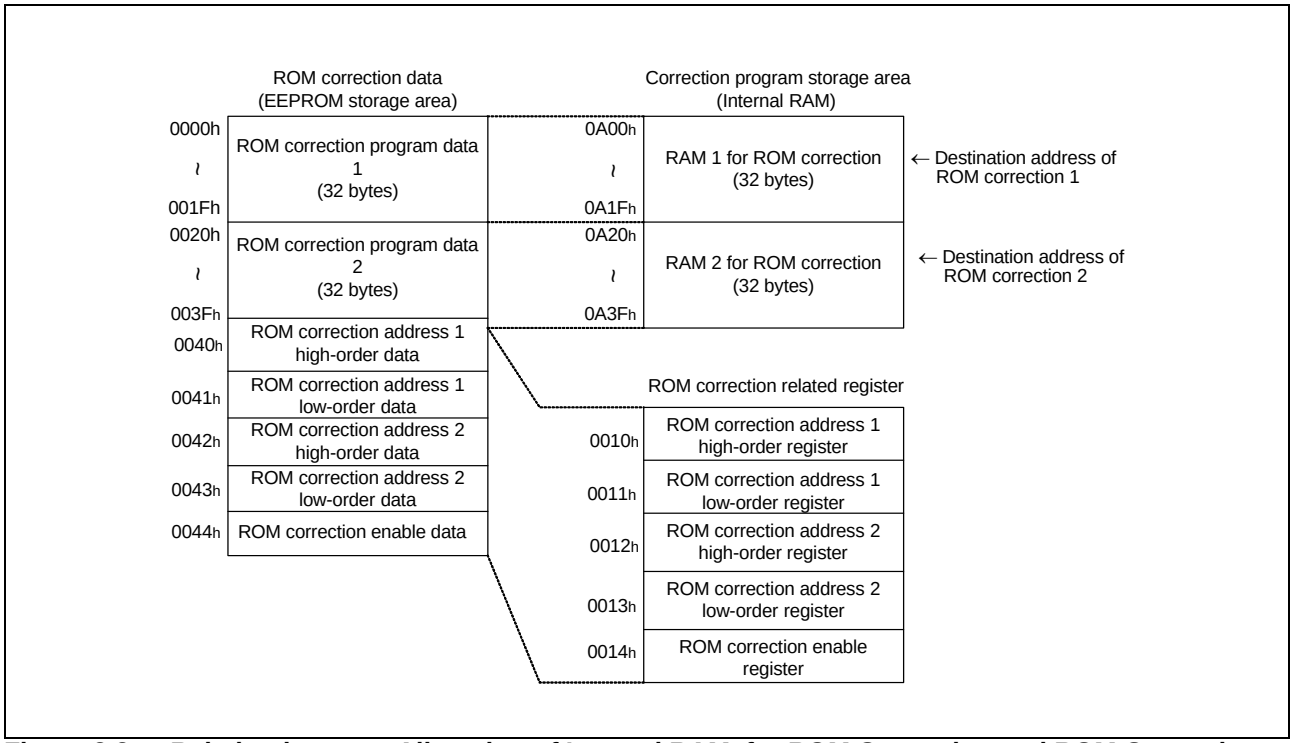


Figure 3.3 Relation between Allocation of Internal RAM for ROM Correction and ROM Correction Data

3.3 Control Procedure

Figure 3.4 shows the Control Procedure for Start-up Processing.

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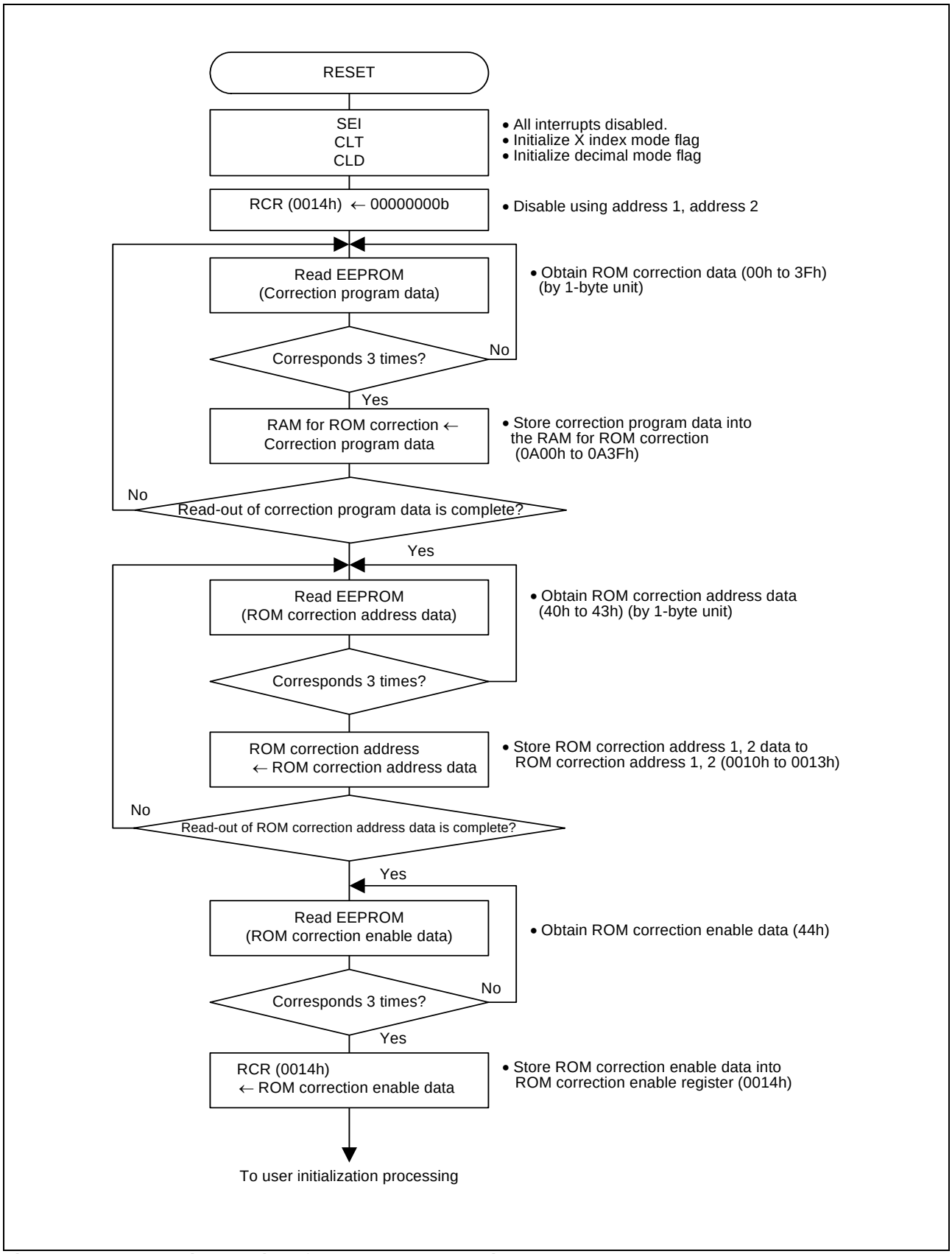

Figure 3.4 Control Procedure for Start-up Processing

3.4 Example of ROM correction function use

Figure 3.5 shows the Example of ROM Correction Function Use.

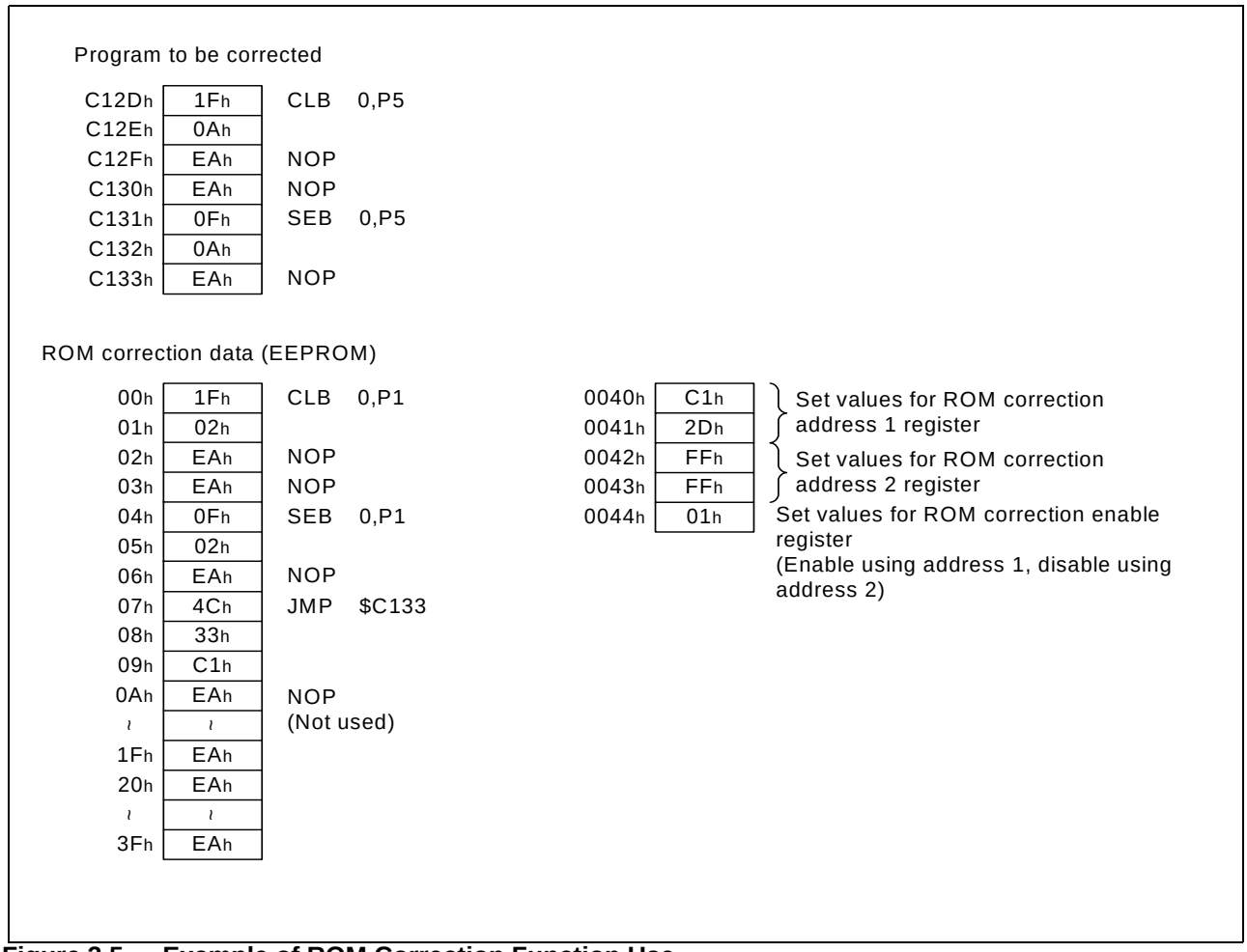

Figure 3.5 Example of ROM Correction Function Use

In this example, the program jumps to the start address of the RAM 1 for ROM correction (0A00h) when the value of the program counter (PC) corresponds with the value set to the ROM correction address 1 (C12Dh). (The instruction in the address C12Dh is not executed). Then, the correction program stored in the address 0A00h is executed. (Addresses 0A00h to 0A1Fh are used as storage for ROM correction program). The program returns to the destination address (C133h) of the JMP instruction set at the end of the correction program.

4. Sample Programming Code

Download a sample program from the Renesas Technology website.
To download, click “Application Notes” in the left side menu on the page of the 3823 Group.

5. Reference Documents

Datasheet
3823 Group Datasheet
Download the latest version from the Renesas Technology website.

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REVISION HISTORY	3823 Group ROM Correction Function

Rev.	Date	Description	
		Page	Summary
1.00	Feb 23, 2007	–	First Edition issued

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