To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

Send any inquiries to http://www.renesas.com/inquiry.

Notice

1. All information included in this document is current as of the date this document is issued. Such information, however, is subject to change without any prior notice. Before purchasing or using any Renesas Electronics products listed herein, please confirm the latest product information with a Renesas Electronics sales office. Also, please pay regular and careful attention to additional and different information to be disclosed by Renesas Electronics such as that disclosed through our website.
2. Renesas Electronics does not assume any liability for infringement of patents, copyrights, or other intellectual property rights of third parties by or arising from the use of Renesas Electronics products or technical information described in this document. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
3. You should not alter, modify, copy, or otherwise misappropriate any Renesas Electronics product, whether in whole or in part.
4. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation of these circuits, software, and information in the design of your equipment. Renesas Electronics assumes no responsibility for any losses incurred by you or third parties arising from the use of these circuits, software, or information.
5. When exporting the products or technology described in this document, you should comply with the applicable export control laws and regulations and follow the procedures required by such laws and regulations. You should not use Renesas Electronics products or the technology described in this document for any purpose relating to military applications or use by the military, including but not limited to the development of weapons of mass destruction. Renesas Electronics products and technology may not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations.
6. Renesas Electronics has used reasonable care in preparing the information included in this document, but Renesas Electronics does not warrant that such information is error free. Renesas Electronics assumes no liability whatsoever for any damages incurred by you resulting from errors in or omissions from the information included herein.
7. Renesas Electronics products are classified according to the following three quality grades: "Standard", "High Quality", and "Specific". The recommended applications for each Renesas Electronics product depends on the product's quality grade, as indicated below. You must check the quality grade of each Renesas Electronics product before using it in a particular application. You may not use any Renesas Electronics product for any application categorized as "Specific" without the prior written consent of Renesas Electronics. Further, you may not use any Renesas Electronics product for any application for which it is not intended without the prior written consent of Renesas Electronics. Renesas Electronics shall not be in any way liable for any damages or losses incurred by you or third parties arising from the use of any Renesas Electronics product for an application categorized as "Specific" or for which the product is not intended where you have failed to obtain the prior written consent of Renesas Electronics. The quality grade of each Renesas Electronics product is "Standard" unless otherwise expressly specified in a Renesas Electronics data sheets or data books, etc.

   "Standard": Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; and industrial robots.

   "High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control systems; anti-disaster systems; anti-crime systems; safety equipment; and medical equipment not specifically designed for life support.

   "Specific": Aircraft; aerospace equipment; submersible repeaters; nuclear reactor control systems; medical equipment or systems for life support (e.g. artificial life support devices or systems), surgical implantations, or healthcare intervention (e.g. excision, etc.), and any other applications or purposes that pose a direct threat to human life.
8. You should use the Renesas Electronics products described in this document within the range specified by Renesas Electronics, especially with respect to the maximum rating, operating supply voltage range, movement power voltage range, heat radiation characteristics, installation and other product characteristics. Renesas Electronics shall have no liability for malfunctions or damages arising out of the use of Renesas Electronics products beyond such specified ranges.
9. Although Renesas Electronics endeavors to improve the quality and reliability of its products, semiconductor products have specific characteristics such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Further, Renesas Electronics products are not subject to radiation resistance design. Please be sure to implement safety measures to guard them against the possibility of physical injury, and injury or damage caused by fire in the event of the failure of a Renesas Electronics product, such as safety design for hardware and software including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult, please evaluate the safety of the final products or system manufactured by you.
10. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. Please use Renesas Electronics products in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. Renesas Electronics assumes no liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
11. This document may not be reproduced or duplicated, in any form, in whole or in part, without prior written consent of Renesas Electronics.
12. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products, or if you have any other inquiries.

(Note 1) "Renesas Electronics" as used in this document means Renesas Electronics Corporation and also includes its majority-owned subsidiaries.

(Note 2) "Renesas Electronics product(s)" means any product developed or manufactured by or for Renesas Electronics.

3803 Group (Spec.H)

List of Registers

1. Abstract

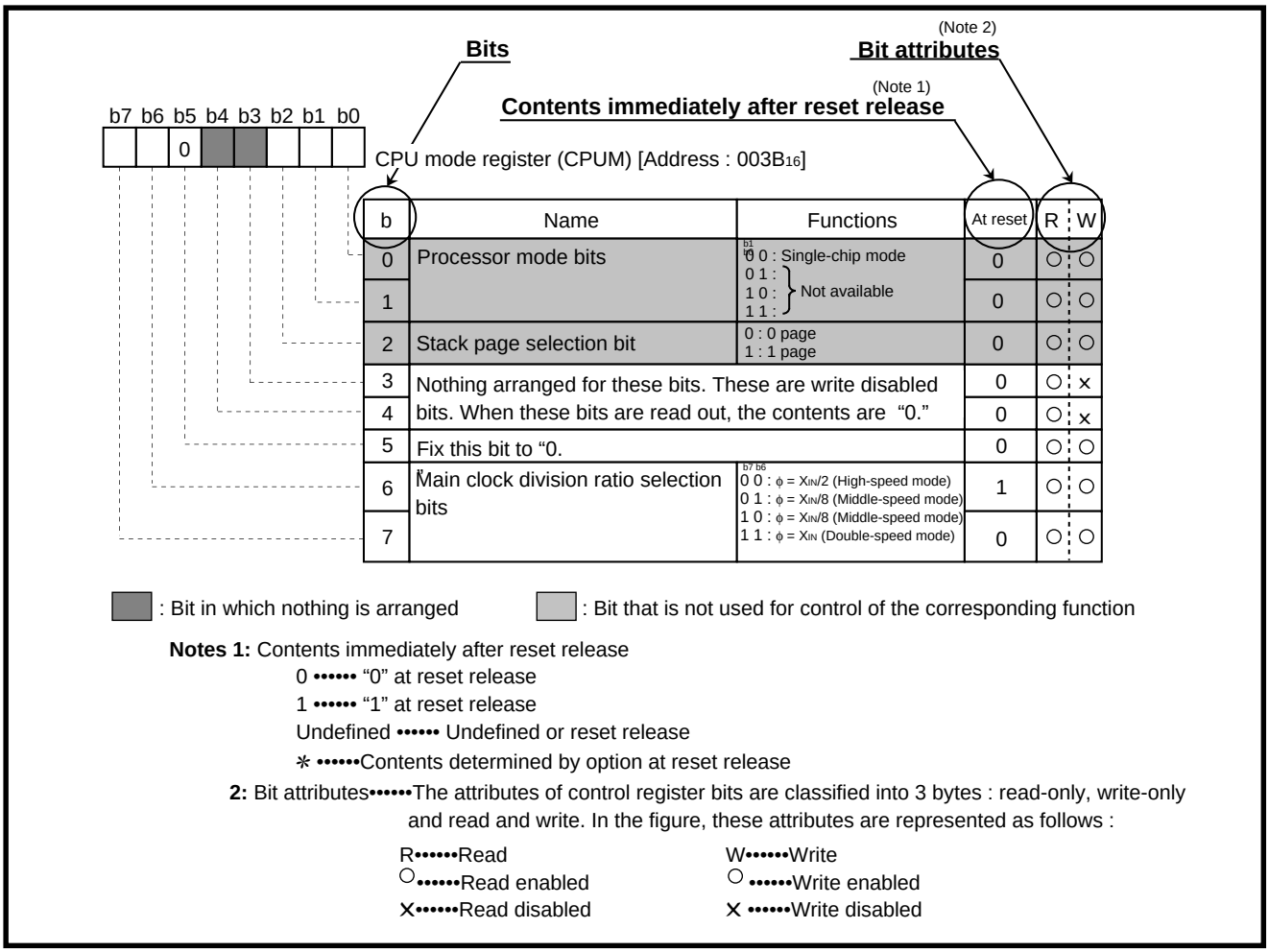
The following article describes the control registers of the 3803 Group (Spec.H).

2. Introduction

The explanation of this issue is applied to the following condition:
Applicable MCU: 3803 Group (Spec.H)

3. Structure of Register

The figure of each register structure describes its functions, contents at reset, and attributes as follows:



Notes 1: Contents immediately after reset release
0 •••••• "0" at reset release
1 •••••• "1" at reset release
Undefined •••••• Undefined or reset release
✻ ••••••Contents determined by option at reset release

2: Bit attributes••••••The attributes of control register bits are classified into 3 bytes : read-only, write-only and read and write. In the figure, these attributes are represented as follows :

R••••••Read
○••••••Read enabled
×••••••Read disabled

W••••••Write
○ ••••••Write enabled
× ••••••Write disabled

4 List of registers

Port Pi

b7 b6 b5 b4 b3 b2 b1 b0

Port Pi (i = 0, 1, 2, 3, 4, 5, 6)
(Pi: addresses 0000_{16}, 0002_{16}, 0004_{16}, 0006_{16}, 0008_{16}, $000A_{16}$, $000C_{16}$)

b	Name	Functions	At reset	R	W
0	Port Pi_0	●In output mode Write •••••••• Port latch Read •••••••• Port latch ●In input mode Write •••••••• Port latch Read •••••••• Value of pin	0	○	○
1	Port Pi_1		0	○	○
2	Port Pi_2		0	○	○
3	Port Pi_3		0	○	○
4	Port Pi_4		0	○	○
5	Port Pi_5		0	○	○
6	Port Pi_6		0	○	○
7	Port Pi_7		0	○	○

Fig. 4.1 Structure of Port Pi

Port Pi direction register

b7 b6 b5 b4 b3 b2 b1 b0

Port Pi direction register (i = 0, 1, 2, 3, 4, 5, 6)
(PiD: addresses 0001_{16}, 0003_{16}, 0005_{16}, 0007_{16}, 0009_{16}, $000B_{16}$, $000D_{16}$)

b	Name	Functions	At reset	R	W
0	Port Pi direction register	0 : Port Pi_0 input mode 1 : Port Pi_0 output mode	0	×	○
1		0 : Port Pi_1 input mode 1 : Port Pi_1 output mode	0	×	○
2		0 : Port Pi_2 input mode 1 : Port Pi_2 output mode	0	×	○
3		0 : Port Pi_3 input mode 1 : Port Pi_3 output mode	0	×	○
4		0 : Port Pi_4 input mode 1 : Port Pi_4 output mode	0	×	○
5		0 : Port Pi_5 input mode 1 : Port Pi_5 output mode	0	×	○
6		0 : Port Pi_6 input mode 1 : Port Pi_6 output mode	0	×	○
7		0 : Port Pi_7 input mode 1 : Port Pi_7 output mode	0	×	○

Fig. 4.2 Structure of Port Pi direction register

Timer 12, X count source selection register

b7 b6 b5 b4 b3 b2 b1 b0

Timer 12, X count source selection register
(T12XCSS: address 000E16)

b	Name	Functions	At reset	R	W
0	Timer 12 count source selection bits	b3b2b1b0 0 0 0 0: f(XIN)/2 or f(XCIN)/2 0 0 0 1: f(XIN)/4 or f(XCIN)/4 0 0 1 0: f(XIN)/8 or f(XCIN)/8 0 0 1 1: f(XIN)/16 or f(XCIN)/16 0 1 0 0: f(XIN)/32 or f(XCIN)/32 0 1 0 1: f(XIN)/64 or f(XCIN)/64 0 1 1 0: f(XIN)/128 or f(XCIN)/128 0 1 1 1: f(XIN)/256 or f(XCIN)/256 1 0 0 0: f(XIN)/512 or f(XCIN)/512 1 0 0 1: f(XIN)/1024 or f(XCIN)/1024 1010 to 1111: Not available	1	○	○
1			1	○	○
2			0	○	○
3			0	○	○
4	Timer X count source selection bits	b7b6b5b4 0 0 0 0: f(XIN)/2 or f(XCIN)/2 0 0 0 1: f(XIN)/4 or f(XCIN)/4 0 0 1 0: f(XIN)/8 or f(XCIN)/8 0 0 1 1: f(XIN)/16 or f(XCIN)/16 0 1 0 0: f(XIN)/32 or f(XCIN)/32 0 1 0 1: f(XIN)/64 or f(XCIN)/64 0 1 1 0: f(XIN)/128 or f(XCIN)/128 0 1 1 1: f(XIN)/256 or f(XCIN)/256 1 0 0 0: f(XIN)/512 or f(XCIN)/512 1 0 0 1: f(XIN)/1024 or f(XCIN)/1024 1 0 1 0: f(XCIN) 1011 to 1111: Not available	1	○	○
5			1	○	○
6			0	○	○
7			0	○	○

Fig. 4.3 Structure of Timer 12, X count source selection register

Timer Y, Z count source selection register

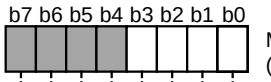
b7 b6 b5 b4 b3 b2 b1 b0

Timer Y, Z count source selection register
(TYZCSS: address 000F16)

b	Name	Functions	At reset	R	W
0	Timer Y count source selection bits	b3b2b1b0 0 0 0 0: f(XIN)/2 or f(XCIN)/2 0 0 0 1: f(XIN)/4 or f(XCIN)/4 0 0 1 0: f(XIN)/8 or f(XCIN)/8 0 0 1 1: f(XIN)/16 or f(XCIN)/16 0 1 0 0: f(XIN)/32 or f(XCIN)/32 0 1 0 1: f(XIN)/64 or f(XCIN)/64 0 1 1 0: f(XIN)/128 or f(XCIN)/128 0 1 1 1: f(XIN)/256 or f(XCIN)/256 1 0 0 0: f(XIN)/512 or f(XCIN)/512 1 0 0 1: f(XIN)/1024 or f(XCIN)/1024 1 0 1 0: f(XCIN) 1011 to 1111: Not available	1	○	○
1			1	○	○
2			0	○	○
3			0	○	○
4	Timer Z count source selection bits	b7b6b5b4 0 0 0 0: f(XIN)/2 or f(XCIN)/2 0 0 0 1: f(XIN)/4 or f(XCIN)/4 0 0 1 0: f(XIN)/8 or f(XCIN)/8 0 0 1 1: f(XIN)/16 or f(XCIN)/16 0 1 0 0: f(XIN)/32 or f(XCIN)/32 0 1 0 1: f(XIN)/64 or f(XCIN)/64 0 1 1 0: f(XIN)/128 or f(XCIN)/128 0 1 1 1: f(XIN)/256 or f(XCIN)/256 1 0 0 0: f(XIN)/512 or f(XCIN)/512 1 0 0 1: f(XIN)/1024 or f(XCIN)/1024 1 0 1 0: f(XCIN) 1011 to 1111: Not available	1	○	○
5			1	○	○
6			0	○	○
7			0	○	○

Fig. 4.4 Structure of Timer Y, Z count source selection register

MISRG



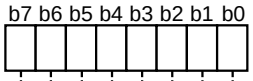
MISRG
(MISRG: address 0010_{16})

b	Name	Functions	At reset	R	W
0	Oscillatin stabilizing time set after STP instruction released bit	0: Automatically set (**Note 1**) 1: Autimatically set disabled	0	○	○
1	Middle-speed mode automatic switch set bit	0: Not set automatically 1: Automatic switching enabled (**Notes 2**)	0	○	○
2	Middle-speed mode automatic switch wait time set bit	0: 4.5 to 5.5 machine cycles 1: 6.5 to 7.5 machine cycles	0	○	○
3	Middle-speed mode automatic switch start bit (Depending on program)	0: Invalid 1: Automatic switch start (**Note 2**)	0	○	○
4	Nothing is arranged for these bits. These are write disabled bits. When these bits are read out, the contents are “0”.		0	○	×
5			0	○	×
6			0	○	×
7			0	○	×

Notes 1: “01_{16}” is set to Timer 1, “FF_{16}” is set to Prescaler 12.
2: When automatic switch to middle-speed mode from low-speed mode occurs, the values of CPU mode register ($003B_{16}$) change.

Fig. 4.5 Structure of MISRG

Transmit/Receive buffer register 1, Transmit/Receive buffer register 3



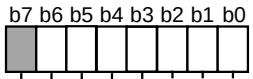
Transmit/Receive buffer register 1 (TB1/RB1: address 0018_{16})
Transmit/Receive buffer register 3 (TB3/RB3: address 0030_{16})

b	Functions	At reset	R	W
0	The transmission data is written to or the receive data is read out from this buffer register. • At write: A data is written to the transmit buffer register. • At read: The contents of the receive buffer register are read out.	Undefined	○	○
1		Undefined	○	○
2		Undefined	○	○
3		Undefined	○	○
4		Undefined	○	○
5		Undefined	○	○
6		Undefined	○	○
7		Undefined	○	○

Note: The contents of transmit buffer register cannot be read out.
The data cannot be written to the receive buffer register.

Fig. 4.6 Structure of Transmit/Receive buffer register 1, Transmit/Receive buffer register 3

Serial I/O1 status register, Serial I/O3 status register

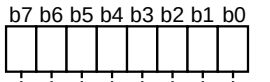


Serial I/O1 status register (SIO1STS: address 0019_{16})
Serial I/O3 status register (SIO3STS: address 0031_{16})

b	Name	Functions	At reset	R	W
0	Transmit buffer empty flag (TBE)	0: Buffer full 1: Buffer empty	0	○	×
1	Receive buffer full flag (RBF)	0: Buffer empty 1: Buffer full	0	○	×
2	Transmit shift register shift completion flag (TSC)	0: Transmit shift in progress 1: Transmit shift completed	0	○	×
3	Overrun error flag (OE)	0: No error 1: Overrun error	0	○	×
4	Parity error flag (PE)	0: No error 1: Parity error	0	○	×
5	Framing error flag (FE)	0: No error 1: Framing error	0	○	×
6	Summing error flag (SE)	0: (OE) U (PE) U (FE) = 0 1: (OE) U (PE) U (FE) = 1	0	○	×
7	Nothing is arranged for this bit. This bit is a write disabled bit. When this bit is read out, the contents are “1”.		1	○	×

Fig. 4.7 Structure of Serial I/O1 status register, Serial I/O3 status register

Serial I/O1 control register



Serial I/O1 control register
(SIO1CON: address 001A16)

b	Name	Functions	At reset	R	W
0	BRG count source selection bit (CSS)	0: f(XIN) 1: f(XIN)/4	0	○	○
1	Serial I/O1 synchronous clock selection bit (SCS)	When clock synchronous serial I/O is selected, 0: BRG output divided by 4 1: External clock input When UART is selected, 0: BRG output divided by 16 1: External clock input divided by16	0	○	○
2	$\overline{SRDY1}$ output enable bit (SRDY)	0: I/O port (P47) 1: $\overline{SRDY1}$ output pin	0	○	○
3	Transmit interrupt source selection bit (TIC)	0: Transmit buffer empty 1: Transmit shift operation completion	0	○	○
4	Transmit enable bit (TE)	0: Transmit disabled 1: Transmit enabled	0	○	○
5	Receive enable bit (RE)	0: Receive disabled 1: Receive enabled	0	○	○
6	Serial I/O1 mode selection bit (SIOM)	0: UART 1: Clock synchronous serial I/O	0	○	○
7	Serial I/O1 enable bit (SIOE)	0: Serial I/O1 disabled (P44 to P47: normal I/O pins) 1: Serial I/O1 enabled (P44 to P47: Serial I/O pins)	0	○	○

Fig. 4.8 Structure of Serial I/O1 control register

UART1 control register

b7 b6 b5 b4 b3 b2 b1 b0

UART1 control register
(UART1CON: address 001B16)

b	Name	Functions	At reset	R	W
0	Character length selection bit (CHAS)	0: 8 bits 1: 7 bits	0	○	○
1	Parity enable bit (PARE)	0: Parity checking disabled 1: Parity checking enabled	0	○	○
2	Parity selection bit (PARS)	0: Even parity 1: Odd parity	0	○	○
3	Stop bit length selection bit (STPS)	0: 1 stop bit 1: 2 stop bits	0	○	○
4	P45/TxD1 P-channel output disable bit (POFF)	0: CMOS output (in output mode) 1: N-channel open-drain output (in output mode)	0	○	○
5	Nothing is arranged for these bits. These are write disabled bits. When these bits are read out, the contents are “1”.		1	○	×
6			1	○	×
7			1	○	×

Fig. 4.9 Structure of UART1 control register

Baud rate generator i (i = 1, 3)

b7 b6 b5 b4 b3 b2 b1 b0

Baud rate generator i
(BRGi (i=1, 3): address 001C16, 002F16)

b	Functions	At reset	R	W
0	Set a count value of baud rate generator.	Undefined	○	○
1		Undefined	○	○
2		Undefined	○	○
3		Undefined	○	○
4		Undefined	○	○
5		Undefined	○	○
6		Undefined	○	○
7		Undefined	○	○

Note: Write to this register while transmit/receive operation is stopped.

Fig. 4.10 Structure of Baud rate generator i

Serial I/O2 control register

b7 b6 b5 b4 b3 b2 b1 b0

Serial I/O2 control register
(SIO2CON: address 001D16)

b	Name	Functions	At reset	R	W
0	Internal synchronous clock selection bits	b2b1b0 0 0 0: f(XIN)/8 0 0 1: f(XIN)/16 0 1 0: f(XIN)/32 0 1 1: f(XIN)/64 1 1 0: f(XIN)/128 1 1 1: f(XIN)/256	0	○	○
1			0	○	○
2			0	○	○
3	Serial I/O2 port selection bit	0: I/O port (P51, P52) 1: SOUT2, SCLK2 signal output	0	○	○
4	$\overline{\text{SRDY2}}$ output enable bit	0: I/O port (P53) 1: $\overline{\text{SRDY2}}$ signal output	0	○	○
5	Transfer direction selection bit	0: LSB first 1: MSB first	0	○	○
6	Serial I/O2 synchronous clock selection bit	0: External clock 1: Internal clock	0	○	○
7	P51/SOUT2 P-channel output disable bit	0: CMOS output (in output mode) 1: N-channel open-drain output (in output mode)	0	○	○

Fig. 4.11 Structure of Serial I/O2 control register

Watchdog timer control register

b7 b6 b5 b4 b3 b2 b1 b0

Watchdog timer control register
(WDTCON: address 001E16)

b	Name	Functions	At reset	R	W
0	Watchdog timer H (for read-out of high-order 6 bit)		1	○	×
1			1	○	×
2			1	○	×
3			1	○	×
4			1	○	×
5			1	○	×
6	STP instruction disable bit	0: STP instruction enabled 1: STP instruction disabled	0	○	○
7	Watchdog timer H count source selection bit	0: Watchdog timer L underflow 1: f(XIN)/16 or f(XCIN)/16	0	○	○

Fig. 4.12 Structure of Watchdog timer control register

Serial I/O2 register

b7 b6 b5 b4 b3 b2 b1 b0

Serial I/O2 register
(SIO2: address 001F16)

b	Name	Functions	At reset	R	W
0	This register becomes shift register. At transmit: Set transmit data to this register. At receive: Received data is stored to this register.		Undefined	○	○
1			Undefined	○	○
2			Undefined	○	○
3			Undefined	○	○
4			Undefined	○	○
5			Undefined	○	○
6			Undefined	○	○
7			Undefined	○	○

Fig. 4.13 Structure of Serial I/O2 register

Prescaler 12, Prescaler X, Prescaler Y

b7 b6 b5 b4 b3 b2 b1 b0

Prescaler 12 (PRE12), Prescaler X (PREX), Prescaler Y (PREY)
(addresses 002016, 002416, 002616)

b	Functions	At reset	R	W
0	• Set a count value of each prescaler. • The value set in this register is written to both each prescaler and the corresponding prescaler latch at the same time. • When this register is read out, the count value of the corresponding prescaler is read out.	1	○	○
1		1	○	○
2		1	○	○
3		1	○	○
4		1	○	○
5		1	○	○
6		1	○	○
7		1	○	○

Fig. 4.14 Structure of Prescaler 12, Prescaler X, Prescaler Y

Timer 1

b7 b6 b5 b4 b3 b2 b1 b0

Timer 1
(T1: address 0021$_{16}$)

b	Functions	At reset	R	W
0	• Set timer 1 count value. • The value set in this register is written to both the timer 1 and the timer 1 latch at the same time. • When the timer 1 is read out, the count value of the timer 1 is read out.	1	○	○
1		0	○	○
2		0	○	○
3		0	○	○
4		0	○	○
5		0	○	○
6		0	○	○
7		0	○	○

Fig. 4.15 Structure of Timer 1

Timer 2, Timer X, Timer Y

b7 b6 b5 b4 b3 b2 b1 b0

Timer 2 (T2), Timer X (TX), Timer Y (TY)
(addresses 0022$_{16}$, 0025$_{16}$, 0027$_{16}$)

b	Functions	At reset	R	W
0	• Set each timer count value. • The value set in this register is written to both each timer and the corresponding timer latch at the same time. • When each timer is read out, the count value of the corresponding timer is read out.	1	○	○
1		1	○	○
2		1	○	○
3		1	○	○
4		1	○	○
5		1	○	○
6		1	○	○
7		1	○	○

Fig. 4.16 Structure of Timer 2, Timer X, Timer Y

Timer XY mode register

b7 b6 b5 b4 b3 b2 b1 b0

Timer XY mode register
(TM: address 0023$_{16}$)

b	Name	Functions	At reset	R	W
0	Timer X operating mode bits	b1 b0 0 0: Timer mode 0 1: Pulse output mode 1 0: Event counter mode 1 1: Pulse width measurement mode	0	○	○
1			0	○	○
2	CNTR$_0$ active edge switch bit	Refer to Table 3.5.1	0	○	○
3	Timer X count stop bit	0: Count start 1: Count stop	0	○	○
4	Timer Y operating mode bits	b5 b4 0 0: Timer mode 0 1: Pulse output mode 1 0: Event counter mode 1 1: Pulse width measurement mode	0	○	○
5			0	○	○
6	CNTR$_1$ active edge switch bit	Refer to Table 3.5.1	0	○	○
7	Timer Y count stop bit	0: Count start 1: Count stop	0	○	○

Fig. 4.17 Structure of Timer XY mode register

Table 4.1 CNTR$_0$/CNTR$_1$ active edge switch bit function

Timer X/Timer Y operation modes	CNTR$_0$/CNTR$_1$ active edge switch bit (bits 2 and 6 of address 0023$_{16}$) contents	
Timer mode	"0"	CNTR$_0$/CNTR$_1$ interrupt request occurrence: Falling edge ; No influence to timer count
	"1"	CNTR$_0$/CNTR$_1$ interrupt request occurrence: Rising edge ; No influence to timer count
Pulse output mode	"0"	Pulse output start: Beginning at "H" level CNTR$_0$/CNTR$_1$ interrupt request occurrence: Falling edge
	"1"	Pulse output start: Beginning at "L" level CNTR$_0$/CNTR$_1$ interrupt request occurrence: Rising edge
Event counter mode	"0"	Timer X/Timer Y: Rising edge count CNTR$_0$/CNTR$_1$ interrupt request occurrence: Falling edge
	"1"	Timer X/Timer Y: Falling edge count CNTR$_0$/CNTR$_1$ interrupt request occurrence: Rising edge
Pulse width measurement mode	"0"	Timer X/Timer Y: "H" level width measurement CNTR$_0$/CNTR$_1$ interrupt request occurrence: Falling edge
	"1"	Timer X/Timer Y: "L" level width measurement CNTR$_0$/CNTR$_1$ interrupt request occurrence: Rising edge

Timer Z low-order, Timer Z high-order

b7 b6 b5 b4 b3 b2 b1 b0

Timer Z low-order (TZL), Timer Z high-order (TZH)
(addresses 002816, 002916)

b	Functions	At reset	R	W
0	• Set each timer count value. [At write] • Depending on the write control bit (bit 3 of TZM), the value set to this register is written to each timer and the corresponding timer latch at the same time, or is written only to the latch. [At read] • The corresponding timer count value is read out by reading this register. • Read both registers in order of TZH and TZL following. • Write both registers in order of TZL and TZH following.	1	O	O
1		1	O	O
2		1	O	O
3		1	O	O
4		1	O	O
5		1	O	O
6		1	O	O
7		1	O	O

Fig. 4.18 Structure of Timer Z low-order, Timer Z high-order

Timer Z mode register

b7 b6 b5 b4 b3 b2 b1 b0

Timer Z mode register
(TZM: address $002A16$)

b	Name	Functions	At reset	R	W
0	Timer Z operating mode bits	b2b1b0 0 0 0: Timer/Event counter mode 0 0 1: Pulse output mode 0 1 0: Pulse period measurement mode 0 1 1: Pulse width measurement mode 1 0 0: Programmable waveform generating mode 1 0 1: Programmable one-shot generating mode 1 1 0: Not available 1 1 1: Not available	0	O	O
1			0	O	O
2			0	O	O
3	Timer Z write control bit	0: Writing data to both latch and timer simultaneousuly 1: Writing data only to latch	0	O	O
4	Output level latch	0: “L” output 1: “H” output	0	O	O
5	$CNTR_2$ active edge switch bit	Refer to Table 3.5.2.	0	O	O
6	Timer Z count stop bit	0: Count start 1: Count stop	0	O	O
7	Timer/Event counter mode switch bit **(Note)**	0: Timer mode 1: Event counter mode	0	O	O

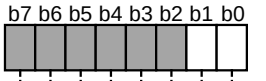
Note: When selecting the modes except the timer/event counter mode, set “0” to this bit.

Fig. 4.19 Structure of Timer Z mode register

Table 4.2 $CNTR_2$ active edge switch bit function

Timer Z operation modes	$CNTR_2$ active edge switch bit (bit 5 of address $002A_{16}$) contents	
Timer mode	"0"	$CNTR_2$ interrupt request occurrence: Falling edge ; No influence to timer count
	"1"	$CNTR_2$ interrupt request occurrence: Rising edge ; No influence to timer count
Event counter mode	"0"	Timer Z: Rising edge count $CNTR_2$ interrupt request occurrence: Falling edge
	"1"	Timer Z: Falling edge count $CNTR_2$ interrupt request occurrence: Rising edge
Pulse output mode	"0"	Pulse output start: Beginning at "H" level $CNTR_2$ interrupt request occurrence: Falling edge
	"1"	Pulse output start: Beginning at "L" level $CNTR_2$ interrupt request occurrence: Rising edge
Pulse period measurement mode	"0"	Timer Z: Period from falling edge to the next falling edge measurement $CNTR_2$ interrupt request occurrence: Falling edge
	"1"	Timer Z: Period from rising edge to the next rising edge measurement $CNTR_2$ interrupt request occurrence: Rising edge
Pulse width measurement mode	"0"	Timer Z: "H" level width measurement $CNTR_2$ interrupt request occurrence: Falling edge
	"1"	Timer Z: "L" level width measurement $CNTR_2$ interrupt request occurrence: Rising edge
Programmable one-shot generating mode	"0"	Timer Z: after start outputting "L", "H" one-shot pulse generated $CNTR_2$ interrupt request occurrence: Falling edge
	"1"	Timer Z: after start outputting "H", "L" one-shot pulse generated $CNTR_2$ interrupt request occurrence: Rising edge

PWM control register

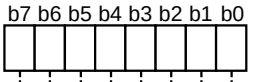


PWM control register (PWMCON: address 002B16)

b	Name	Functions	At reset	R	W
0	PWM function enable bit	0 : PWM disabled 1 : PWM enabled	0	○	○
1	Count source selection bit	0 : f(XIN) 1 : f(XIN)/2	0	○	○
2	Nothing is arranged for these bits. These are write disabled bits. When these bits are read out, the contents are “0”.		0	○	×
3			0	○	×
4			0	○	×
5			0	○	×
6			0	○	×
7			0	○	×

Fig. 4.20 Structure of PWM control register

PWM prescaler

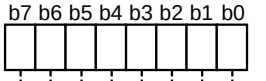


PWM prescaler
(PREPWM: address 002C16)

b	Functions	At reset	R	W
0	•Set the PWM period. •The value set in this register is written to both PWM prescaler pre-latch and PWM prescaler latch at the same time. • When data is written to this register during PWM output, the pulse corresponding to changed value is output at the next period. • When this register is read out, the count value of the PWM prescaler latch is read out.	Undefined	○	○
1		Undefined	○	○
2		Undefined	○	○
3		Undefined	○	○
4		Undefined	○	○
5		Undefined	○	○
6		Undefined	○	○
7		Undefined	○	○

Fig. 4.21 Structure of PWM prescaler

PWM register



PWM register
(PWM: address 002D16)

b	Functions	At reset	R	W
0	• Set the PWM “H” level output interval. • The value set in this register is written to both PWM register pre-latch and PWM register latch at the same time. • When data is written to this register during PWM output, the pulse corresponding to changed value is output at the next period. • When this register is read out, the contents of the PWM register latch is read out.	Undefined	○	○
1		Undefined	○	○
2		Undefined	○	○
3		Undefined	○	○
4		Undefined	○	○
5		Undefined	○	○
6		Undefined	○	○
7		Undefined	○	○

Fig. 4.22 Structure of PWM register

Serial I/O3 control register

b7 b6 b5 b4 b3 b2 b1 b0

Serial I/O3 control register
(SIO3CON: address 0032$_{16}$)

b	Name	Functions	At reset	R	W
0	BRG count source selection bit (CSS)	0: f(XIN) 1: f(XIN)/4	0	○	○
1	Serial I/O3 synchronous clock selection bit (SCS)	When clock synchronous serial I/O is selected, 0: BRG output divided by 4 1: External clock input When UART is selected, 0: BRG output divided by 16 1: External clock input divided by16	0	○	○
2	$\overline{SRDY3}$ output enable bit (SRDY)	0: I/O port (P37) 1: $\overline{SRDY3}$ output pin	0	○	○
3	Transmit interrupt source selection bit (TIC)	0: Transmit buffer empty 1: Transmit shift operation completion	0	○	○
4	Transmit enable bit (TE)	0: Transmit disabled 1: Transmit enabled	0	○	○
5	Receive enable bit (RE)	0: Receive disabled 1: Receive enabled	0	○	○
6	Serial I/O3 mode selection bit (SIOM)	0: UART 1: Clock synchronous serial I/O	0	○	○
7	Serial I/O3 enable bit (SIOE)	0: Serial I/O3 disabled (P34 to P37: normal I/O pins) 1: Serial I/O3 disabled (P34 to P37: Serial I/O pins)	0	○	○

Fig. 4.23 Structure of Serial I/O3 control register

UART3 control register

b7 b6 b5 b4 b3 b2 b1 b0

UART3 control register
(UART3CON: address 0033_{16})

b	Name	Functions	At reset	R	W
0	Character length selection bit (CHAS)	0: 8 bits 1: 7 bits	0	○	○
1	Parity enable bit (PARE)	0: Parity checking disabled 1: Parity checking enabled	0	○	○
2	Parity selection bit (PARS)	0: Even parity 1: Odd parity	0	○	○
3	Stop bit length selection bit (STPS)	0: 1 stop bit 1: 2 stop bits	0	○	○
4	$P3_5$/TxD_3 P-channel output disable bit (POFF)	0: CMOS output (in output mode) 1: N-channel open-drain output (in output mode)	0	○	○
5	Nothing is arranged for these bits. These are write disabled bits. When these bits are read out, the contents are “1”.		1	○	×
6			1	○	×
7			1	○	×

Fig. 4.24 Structure of UART3 control register

AD/DA control register

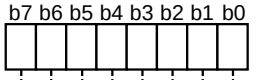
b7 b6 b5 b4 b3 b2 b1 b0

AD/DA control register
(ADCON: address 0034_{16})

b	Name	Functions	At reset	R	W
0	Analog input pin selection bits 1	b2 b1 b0 0 0 0: $P6_0$/AN_0 or $P0_0$/AN_8 0 0 1: $P6_1$/AN_1 or $P0_1$/AN_9 0 1 0: $P6_2$/AN_2 or $P0_2$/AN_{10} 0 1 1: $P6_3$/AN_3 or $P0_3$/AN_{11} 1 0 0: $P6_4$/AN_4 or $P0_4$/AN_{12} 1 0 1: $P6_5$/AN_5 or $P0_5$/AN_{13} 1 1 0: $P6_6$/AN_6 or $P0_6$/AN_{14} 1 1 1: $P6_7$/AN_7 or $P0_7$/AN_{15}	0	○	○
1			0	○	○
2			0	○	○
3	AD conversion completion bit	0: Conversion in progress 1: Conversion completed	1	○	○
4	Analog input pin selection bit 2	0: AN_0 to AN_7 side 1: AN_8 to AN_{15} side	0	○	○
5	Nothing is arranged for this bit. This is a write disabled bit. When this bit is read out, the contents are “0”.		0	○	×
6	DA_1 output enable bit	0: DA_1 output disabled 1: DA_1 output enabled	0	○	○
7	DA_2 output enable bit	0: DA_2 output disabled 1: DA_2 output enabled	0	○	○

Fig. 4.25 Structure of AD/DA control register

A-D conversion register 1

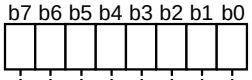


A-D conversion register 1
(AD1: address 0035$_{16}$)

b	Functions	At reset	R	W
0	This is A-D conversion result stored bits. This is read exclusive register. 8-bit read: b7 … b0 = b9 b8 b7 b6 b5 b4 b3 b2 10-bit read: b7 … b0 = b7 b6 b5 b4 b3 b2 b1 b0	Undefined	○	×
1		Undefined	○	×
2		Undefined	○	×
3		Undefined	○	×
4		Undefined	○	×
5		Undefined	○	×
6		Undefined	○	×
7		Undefined	○	×

Fig. 4.26 Structure of A-D conversion register 1

D-Ai conversion register

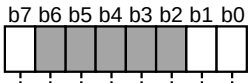


D-Ai conversion register (i = 1, 2)
(DAi: addresses 0036$_{16}$, 0037$_{16}$)

b	Functions	At reset	R	W
0	This is D-A output value stored bits. This is write exclusive register.	0	×	○
1		0	×	○
2		0	×	○
3		0	×	○
4		0	×	○
5		0	×	○
6		0	×	○
7		0	×	○

Fig. 4.27 Structure of D-Ai conversion register (i = 1, 2)

A-D conversion register 2

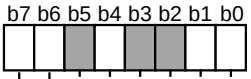


A-D conversion register 2
(AD2: address 0038$_{16}$)

b	Functions		At reset	R	W
0	This is A-D conversion result stored bits. This is read exclusive register. 10-bit read: b7 … b0 = b9 b8		Undefined	○	×
1			Undefined	○	×
2	Nothing is arranged for these bits. These are write disabled bits. When these bits are read out, the contents are “0”.		0	○	×
3			0	○	×
4			0	○	×
5			0	○	×
6			0	○	×
7	Conversion mode selection bit	0: 10-bit A-D mode 1: 8-bit A-D mode	0	○	○

Fig. 4.28 Structure of A-D conversion register 2

Interrupt source selection register



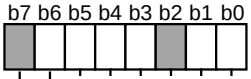
Interrupt source selection register
(INTSEL: address 0039_{16})

b	Name	Functions	At reset	R	W
0	INT_0/Timer Z interrupt source selection bit (*1)	0: INT_0 interrupt 1: Timer Z interrupt	0	○	○
1	Serial I/O2/Timer Z interrupt source selection bit (*1)	0: Serial I/O2 interrupt 1: Timer Z interrupt	0	○	○
2	Nothing is arranged for these bits. Do not write “1” to these bits. When these bits are read out, the contents are “0”.		0	○	○
3			0	○	○
4	INT_4/$CNTR_2$ interrupt source selection bit	0: INT_4 interrupt 1: $CNTR_2$ interrupt	0	○	○
5	Nothing is arranged for this bit. Do not write “1” to this bit. When this bit is read out, the contents are “0”.		0	○	○
6	$CNTR_1$/Serial I/O3 receive interrupt source selection bit	0: $CNTR_1$ interrupt 1: Serial I/O3 receive interrupt	0	○	○
7	AD converter/Serial I/O3 transmit interrupt source selection bit	0: A-D converter interrupt 1: Serial I/O3 transmit interrupt	0	○	○

*1: Do not write “1” to these bits simultaneously.

Fig. 4.29 Structure of Interrupt source selection register

Interrupt edge selection register



Interrupt edge selection register
(INTEDGE: address $003A_{16}$)

b	Name	Functions	At reset	R	W
0	INT_0 active edge selection bit	0: Falling edge active 1: Rising edge active	0	○	○
1	INT_1 active edge selection bit	0: Falling edge active 1: Rising edge active	0	○	○
2	Nothing is arranged for this bit. This is a write disabled bit. When this bit is read out, the contents are “0”.		0	○	×
3	INT_2 active edge selection bit	0: Falling edge active 1: Rising edge active	0	○	○
4	INT_3 active edge selection bit	0: Falling edge active 1: Rising edge active	0	○	○
5	INT_4 active edge selection bit	0: Falling edge active 1: Rising edge active	0	○	○
6	INT_0, INT_4 interrupt switch bit	0: INT_{00}, INT_{40} interrupt 1: INT_{01}, INT_{41} interrupt	0	○	○
7	Nothing is arranged for this bit. This is a write disabled bit. When this bit is read out, the contents are “0”.		0	○	×

Fig. 4.30 Structure of Interrupt edge selection register

CPU mode register

b7 b6 b5 b4 b3 b2 b1 b0

1

CPU mode register
(CPUM: address 003B16)

b	Name	Functions	At reset	R	W
0	Processor mode bits	b1 b0 00 : Single-chip mode 01 : 10 : } Not available 11 :	0	○	○
1			0	○	○
2	Stack page selection bit	0 : 0 page 1 : 1 page	0	○	○
3	Fix this bit to “1”.		1	○	○
4	Port Xc switch bit	0: I/O port function (stop oscillating) 1: XCIN-XCOUT oscillation function	0	○	○
5	Main clock (XIN-XOUT) stop bit	0: Oscillating 1: Stopped	0	○	○
6	Main clock division ratio selection bits	b7 b6 0 0: ϕ=f(XIN)/2 (high-speed mode) 0 1: ϕ=f(XIN)/8 (middle-speed mode) 1 0: ϕ=f(XCIN)/2 (low-speed mode) 1 1: not available	1	○	○
7			0	○	○

Fig. 4.31 Structure of CPU mode register

Interrupt request register 1

b7 b6 b5 b4 b3 b2 b1 b0

Interrupt request register 1
(IREQ1 : address 003C16)

b	Name	Functions	At reset	R	W
0	INT0/Timer Z interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	○	✻
1	INT1 interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	○	✻
2	Serial I/O1 receive interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	○	✻
3	Serial I/O1 transmit interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	○	✻
4	Timer X interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	○	✻
5	Timer Y interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	○	✻
6	Timer 1 interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	○	✻
7	Timer 2 interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	○	✻

✻: “0” can be set by software, but “1” cannot be set.

Fig. 4.32 Structure of Interrupt request register 1

Interrupt request register 2

b7 b6 b5 b4 b3 b2 b1 b0

Interrupt request register 2
(IREQ2 : address 003D16)

b	Name	Functions	At reset	R	W
0	CNTR0 interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	○	✻
1	CNTR1/Serial I/O3 receive interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	○	✻
2	Serial I/O2/Timer Z interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	○	✻
3	INT2 interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	○	✻
4	INT3 interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	○	✻
5	INT4/CNTR2 interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	○	✻
6	AD converter/Serial I/O3 transmit interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	○	✻
7	Nothing is arranged for this bit. This is a write disabled bit. When this bit is read out, the contents are “0”.		0	○	×

✻: “0” can be set by software, but “1” cannot be set.

Fig. 4.33 Structure of Interrupt request register 2

Interrupt control register 1

b7 b6 b5 b4 b3 b2 b1 b0

Interrupt control register 1
(ICON1 : address 003E16)

b	Name	Functions	At reset	R	W
0	INT0/Timer Z interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
1	INT1 interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
2	Serial I/O1 receive interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
3	Serial I/O1 transmit interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
4	Timer X interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
5	Timer Y interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
6	Timer 1 interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
7	Timer 2 interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○

Fig. 4.34 Structure of Interrupt control register 1

Interrupt control register 2

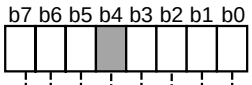
b7 b6 b5 b4 b3 b2 b1 b0
0

Interrupt control register 2
(ICON2 : address 003F16)

b	Name	Functions	At reset	R	W
0	CNTR0 interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
1	CNTR1/ Serial I/O3 receive interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
2	Serial I/O2/ Timer Z interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
3	INT2 interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
4	INT3 interrupt enable bit	0 : Interrupt disabled	0	○	○
5	INT4/CNTR2 interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
6	AD converter/Serial I/O3 transmit interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
7	Fix this bit to “0”.		0	○	○

Fig. 4.35 Structure of Interrupt control register 2

Flash memory control register 0



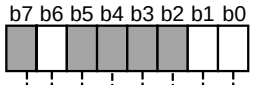
Flash memory control register 0
(FMCR0 : address 0FE0$_{16}$)

b	Name	Functions	At reset	R	W
0	RY/$\overline{BY}$ status flag	0 : Busy (being automatic written or automatic erased) 1 : Ready	1	○	×
1	CPU rewrite mode select bit **(Note 1)**	0 : CPU rewrite mode invalid (software commandes invalid) 1 : CPU rewrite mode valid (Software commands acceptable)	0	○	○
2	8 KB user block E/W enable bit **(Notes 1, 2)**	0: E/W disabled 1: E/W enabled	0	○	○
3	Flash memory reset bit **(Note 3)**	0: Normal operation 1: Reset	0	○	○
4	Not used (Do not write “1” to this bit.)		0	○	○
5	User ROM area select bit	0: User ROM area is accessed 1: Boot ROM area is accessed	0	○	○
6	Program status flag	0: Pass 1: Error	0	○	×
7	Erase status flag	0: Pass 1: Error	0	○	×

Notes 1: For this bit to be set to “1”, the user needs to write a “0” and then a “1” to it in succession. For this bit to be set to “0”, write “0” only to this bit.
2: This bit can be written only when the CPU rewrite mode select bit is “1”.
3: Effective only when the CPU rewrite mode select bit = “1”. Fix this bit to “0” when the CPU rewrite mode select bit is “0”.
4: When setting this bit to “1” (when the control circuit of flash memory is reset), the flash memory cannot be accessed for 10 µs.
5: Write to this bit from program on RAM.

Fig. 4.36 Structure of Flash memory control register 0 (Flash memory version only)

Flash memory control register 1



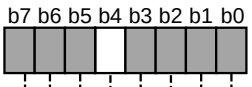
Flash memory control register 1
(FMCR1 : address 0FE1$_{16}$)

b	Name	Functions	At reset	R	W
0	Erase suspend enable bit **(Note 1)**	0 : Suspend invalid 1 : Suspend valid	0	○	○
1	Erase suspend request bit **(Note 2)**	0 : Erase restart (no request issued) 1 : Suspend request (request issued)	0	○	○
2	Nothing is arranged for these bits. If writing to these bits, write “0”. The contents are undefined at reading.		0	○	×
3			0	○	×
4			0	○	×
5			0	○	×
6	Erase suspend flag	0 : Erase active 1 : Erase inactive (Erase suspend mode)	1	○	×
7	Nothing is arranged for these bits. If writing to these bits, write “0”. The contents are undefined at reading.		0	○	×

Notes 1: For this bit to be set to “1”, the user needs to write a “0” and then a “1” to it in succession.
2: Only when the erase suspend bit is “1”, this bit is valid.

Fig. 4.37 Structure of Flash memory control register 1 (Flash memory version only)

Flash memory control register 2



Flash memory control register 2
(FMCR2 : address 0FE2$_{16}$)

b	Name	Functions	At reset	R	W
0	Nothing is arranged for these bits. If writing to these bits, write “0”. The contents are undefined at reading.		1	○	×
1			0	○	×
2			1	○	×
3			0	○	×
4	All user block E/W enable bit **(Notes 1, 2)**	0 : E/W disabled 1 : E/W enabled	0	○	○
5	Nothing is arranged for these bits. If writing to these bits, write “0”. The contents are undefined at reading.		0	○	×
6			1	○	×
7			0	○	×

Notes 1: For this bit to be set to “1”, the user needs to write a “0” and then a “1” to it in succession.
2: Effective only when the CPU rewrite mode select bit = “1”.

Fig. 4.38 Structure of Flash memory control register 2 (Flash memory version only)

Port Pi pull-up control register (i = 0 to 2, 4 to 6)

b7 b6 b5 b4 b3 b2 b1 b0

Port Pi pull-up control register (i = 0 to 2, 4 to 6)
(PULLi: addresses 0FF0$_{16}$, 0FF1$_{16}$, 0FF2$_{16}$, 0FF4$_{16}$, 0FF5$_{16}$, 0FF6$_{16}$)

b	Name	Functions	At reset	R	W
0	Port Pi$_0$ pull-up control bit	0: No pull-up 1: Pull-up	0	○	○
1	Port Pi$_1$ pull-up control bit	0: No pull-up 1: Pull-up	0	○	○
2	Port Pi$_2$ pull-up control bit	0: No pull-up 1: Pull-up	0	○	○
3	Port Pi$_3$ pull-up control bit	0: No pull-up 1: Pull-up	0	○	○
4	Port Pi$_4$ pull-up control bit	0: No pull-up 1: Pull-up	0	○	○
5	Port Pi$_5$ pull-up control bit	0: No pull-up 1: Pull-up	0	○	○
6	Port Pi$_6$ pull-up control bit	0: No pull-up 1: Pull-up	0	○	○
7	Port Pi$_7$ pull-up control bit	0: No pull-up 1: Pull-up	0	○	○

Fig. 4.39 Structure of Port Pi pull-up control register (i = 0 to 2, 4 to 6)

Port P3 pull-up control register

b7 b6 b5 b4 b3 b2 b1 b0

Port P3 pull-up control register
(PULL3: address 0FF3$_{16}$)

b	Name	Functions	At reset	R	W
0	Port P3$_0$ pull-up control bit	0: No pull-up 1: Pull-up	0	○	○
1	Port P3$_1$ pull-up control bit	0: No pull-up 1: Pull-up	0	○	○
2	Nothing is arranged for these bits. These are write disabled bits. When these bits are read out, the contents are “0”.		0	○	×
3			0	○	×
4	Port P3$_4$ pull-up control bit	0: No pull-up 1: Pull-up	0	○	○
5	Port P3$_5$ pull-up control bit	0: No pull-up 1: Pull-up	0	○	○
6	Port P3$_6$ pull-up control bit	0: No pull-up 1: Pull-up	0	○	○
7	Port P3$_7$ pull-up control bit	0: No pull-up 1: Pull-up	0	○	○

Fig. 4.40 Structure of Port P3 pull-up control register

5. Reference Program Example

Please find the reference program on the Renesas Technology website.
Click the upper left menu of the screen “Application Notes” on the 740 family.

6. Reference

Data Sheet
3803 Group (Spec.H) Data Sheet

Technical News/Technical Update
Before using this material, please visit our website to verify that this is the most updated document available.

7. Website and Support

Renesas Technology Corporation Semiconductor Home Page
http://www.renesas.com

E-mail Support
E-mail: csc@renesas.com

REVISION HISTORY	3803 Group (Spec.H) List of registers

Rev.	Date	Description	
		Page	Summary
1.00	Nov 14, 2005	-	This application note is issued using the information of "Chapter 3.5 List of registers" in the 3803 Group (Spec.H) User's Manual Rev.2.02.

Keep safety first in your circuit designs!

1. Renesas Technology Corporation puts the maximum effort into making semiconductor products better and more reliable, but there is always the possibility that trouble may occur with them. Trouble with semiconductors may lead to personal injury, fire or property damage.
   Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.

Notes regarding these materials

1. These materials are intended as a reference to assist our customers in the selection of the Renesas Technology Corporation product best suited to the customer's application; they do not convey any license under any intellectual property rights, or any other rights, belonging to Renesas Technology Corporation or a third party.
2. Renesas Technology Corporation assumes no responsibility for any damage, or infringement of any third-party's rights, originating in the use of any product data, diagrams, charts, programs, algorithms, or circuit application examples contained in these materials.
3. All information contained in these materials, including product data, diagrams, charts, programs and algorithms represents information on products at the time of publication of these materials, and are subject to change by Renesas Technology Corporation without notice due to product improvements or other reasons. It is therefore recommended that customers contact Renesas Technology Corporation or an authorized Renesas Technology Corporation product distributor for the latest product information before purchasing a product listed herein.
   The information described here may contain technical inaccuracies or typographical errors.
   Renesas Technology Corporation assumes no responsibility for any damage, liability, or other loss rising from these inaccuracies or errors.
   Please also pay attention to information published by Renesas Technology Corporation by various means, including the Renesas Technology Corporation Semiconductor home page (http://www.renesas.com).
4. When using any or all of the information contained in these materials, including product data, diagrams, charts, programs, and algorithms, please be sure to evaluate all information as a total system before making a final decision on the applicability of the information and products. Renesas Technology Corporation assumes no responsibility for any damage, liability or other loss resulting from the information contained herein.
5. Renesas Technology Corporation semiconductors are not designed or manufactured for use in a device or system that is used under circumstances in which human life is potentially at stake. Please contact Renesas Technology Corporation or an authorized Renesas Technology Corporation product distributor when considering the use of a product contained herein for any specific purposes, such as apparatus or systems for transportation, vehicular, medical, aerospace, nuclear, or undersea repeater use.
6. The prior written approval of Renesas Technology Corporation is necessary to reprint or reproduce in whole or in part these materials.
7. If these products or technologies are subject to the Japanese export control restrictions, they must be exported under a license from the Japanese government and cannot be imported into a country other than the approved destination.
   Any diversion or reexport contrary to the export control laws and regulations of Japan and/or the country of destination is prohibited.
8. Please contact Renesas Technology Corporation for further details on these materials or the products contained therein.