Interfacing the RC32355/RC32351 with PCMCIA-based Devices, such as Intersil ISL3873B Wireless MAC

RC32355 Application Note AN-370

Notes

By Harold Gomard

Revision History

June 24, 2002: Initial publication.

Introduction

Although this document specifically references the Intersil ISL3873B Wireless MAC, it is generally applicable to most devices which feature a PCMCIA interface. The dual I/O and memory space addressing is fully specified by the PCMCIA standard, allowing designers to implement their own interface based on this example.

This document describes two alternatives to interfacing the RC32355 or RC32351 Integrated Communications Processor (ICP) with Intersil's ISL3873B wireless MAC. The combination of Intersil's wireless chipset and IDT's integrated processor offers a complete and cost-effective solution to designing an 802.11b Wireless Access-Point, bridging and processing data over DSL, and Ethernet and USB interfaces.

The ILS3873B has a host interface that is designed to connect directly to a PC Card 95 (PCMCIA) socket. Because of the close similarities between PCMCIA and the legacy ISA bus, it is also possible to connect the ISL3873B to the RC32355/RC32351 through its memory controller. The ISL3873B is connected as a 16-bit I/O device and accessed as such through the RC32355/RC32351 memory controller interface. Some basic logic needs to be implemented to interface these two devices, and this document describes two possible implementations of this logic: Using an EPLD or using some logic gates.

Background

IDT RC32355/RC32351 Communications Processors

The RC32355/RC32351 ICPs meet the requirements of various embedded communications applications, including residential gateways, Internet Access Devices (IAD), SOHO routers, and wireless Access Points. It is a single-chip solution that incorporates most of the generic system functions and application-specific interfaces that enable rapid time to market, very low cost systems, simplified designs, and reduced board real estate.

In addition to a high performance 32-bit CPU core, the RC32355/RC32351 ICPs incorporate a number of on-chip generic peripherals, including an SDRAM controller, a separate memory/IO controller supporting 8-, 16-, and 32-bit peripherals, an interrupt controller, timers, and serial ports. The RC32355/RC32351 devices also integrate four on-chip peripherals specifically targeted for communications applications, such as a TDM/PCM bus interface, a 10/100 Ethernet, a USB device controller, and an ATM interface.

Intersil ISL3873B

The Intersil ISL3873B Wireless LAN Integrated Medium Access Controller with Integrated Baseband Processor is part of the PRISM® 2.4GHz radio chip set. The ISL3873B directly interfaces with the Intersil's IF QMODEM (HFA3783). Adding Intersil's RF/IF Converter (ISL3685) and Intersil's Power Amp (HFA3983) offers the designer a complete end-to-end WLAN 802.11b Chip Set solution. Protocol and PHY support are implemented in firmware, thereby supporting customization of the WLAN solution. Firmware implements the full IEEE 802.11 Wireless LAN MAC protocol.

Notes

Interfacing the RC32355/RC32351 with the ISL3873B

Interface Based on an EPLD

The PCMCIA host interface of the ISL3873B implements two different types of address space, Memory space and I/O space, to conform to PCMCIA specifications. During normal operation, i.e., wireless data transfer, it behaves as an I/O device. User read and write operations to internal registers and buffer memory are accomplished via PCMCIA I/O accesses (I/O addresses 0 to 0x3F -> 64 8-bit registers).

To configure the ISL3873B chip, the user must access the attribute space memory, which contains the Card Information Structure (CIS) as well as the 3 Function Configuration Registers (COR, CSR, and PPR). The information contained in the CIS is specific to the PCMCIA protocol and is not used when connected to an RC32355/RC32351 memory interface. However, the FCRs contain control bits essential to the initialization of the ISL3873B and to the firmware download.

These two different types of space (I/O and memory) are accessed separately and through a different set of commands: MEM_READ, MEM_WRITE, IO_READ and IO_WRITE. The I/O space can only be accessed after firmware initialization, which first requires access to Memory space. After proper initialization, the I/O space becomes accessible through its own read/write commands.

From the RC32355/RC32351 standpoint, both spaces will be accessed through the same chip_select signal, CS5, but they will have separate addresses within the CS5-mapped memory space (0x1A00_0000 to 0x1BFF_FFFF). Because the RC32355/RC32351 devices output only one set of read/write commands, some decoding logic is needed to differentiate between the two types of access:

- The attribute memory space which contains the CIS and the FCR registers consists of 1KB of address space starting at the address 0x1A00_0000 and goes up to 0x1A00_03FF
- The I/O space consists of 64 Bytes of data and is located in the address range of 0x1B00_0000 to 0x1B00_00FC.

Note: These address spaces are specific to the Intersil ISL3873B chip. Other devices may use other address spacing.

By asserting or deasserting the ADD[24] signal, it is possible to access either area, as reflected in the EPLD equations shown below.

EPLD Equations

HRST = ! CLD_RST

HCE1 = CS5

HCE2 = CS5 | ! ADD[24]

IORD = OE | CS5 | ! ADD[24]

IOWR = BWE[0] | CS5 | ! ADD[24]

MEMRD = OE | CS5 | ADD[24]

MEMWR = BWE[0] | CS5 | ADD[24]

REG = CS5

Notes

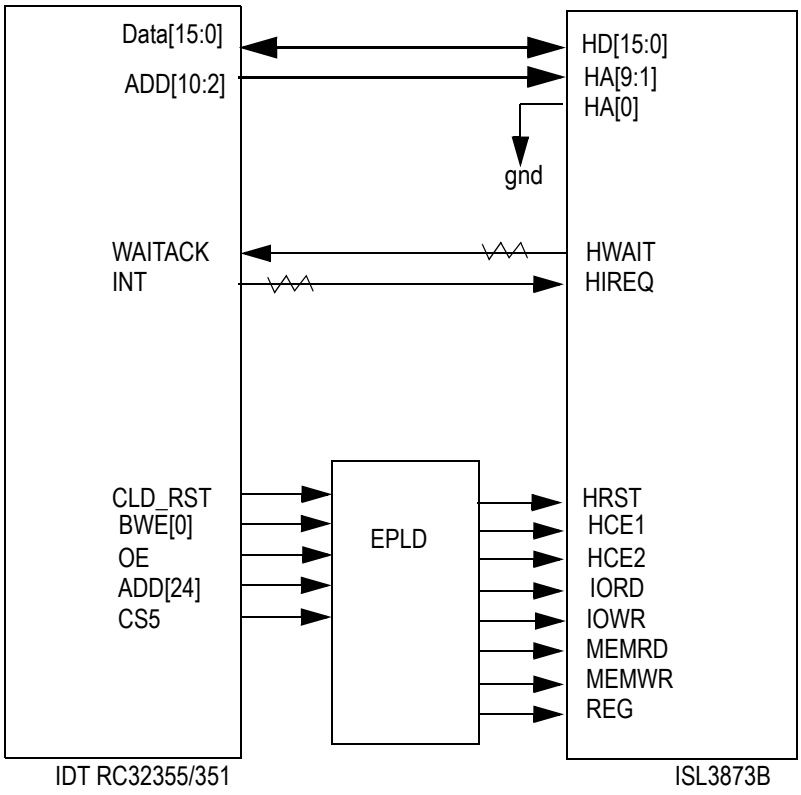

Figure 1 RC32355/351 and XCR3064XL Interface

The EPLD-based interface has been implemented on IDT's 79DB355W wireless daughter board and successfully validated. This board can be plugged into IDT's 79RP355 reference platform and demonstrates the Access-Point, DSL bridge, and Ethernet router capabilities of the RC32355/RC32351 ICPs. Figure 1 displays an EPLD-based interface using the Xilinx XCR3064XL EPLD.

Although the Xilinx XCR3064XL EPLD was used in this case, smaller and cheaper devices, such as the Xilinx XCR3032XL, Xilinx XC2C32, Lattice 3032VE, or Altera EMP3032A EPLD, can be used instead because only 13 I\O pins are required.

Interface Based on Logic Gates

Given the relative simplicity of the glue logic between the Intersil chip and the RC32355/RC32351 processors, logic gates could be used instead of an EPLD, resulting in reduced system cost. Figure 2 displays the necessary logic.

Notes

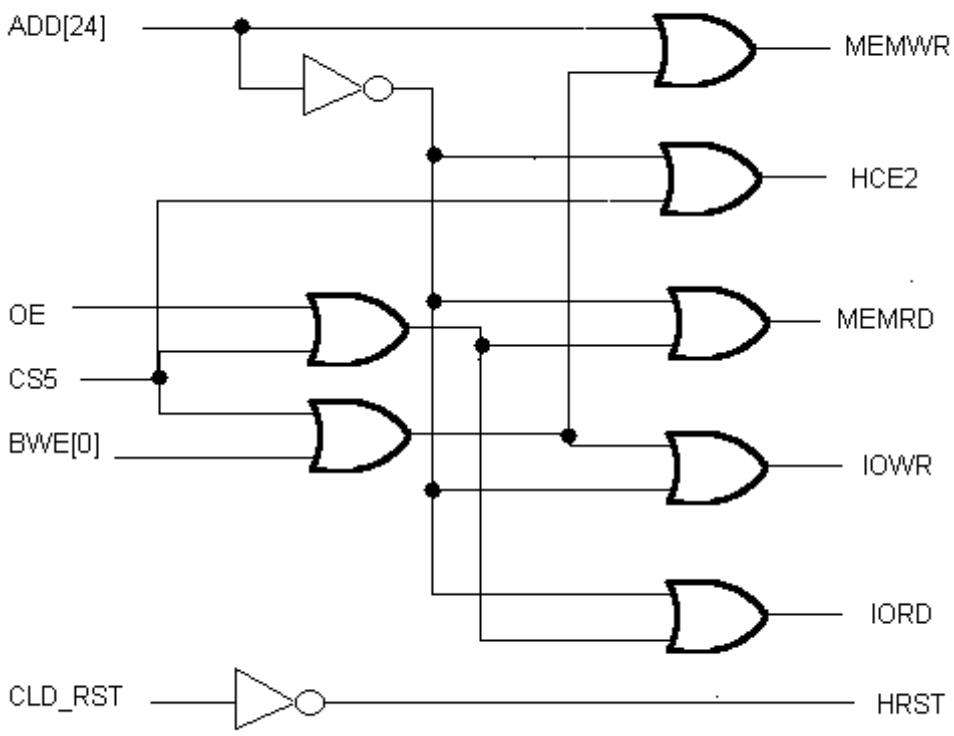

Figure 2 Logic Gate Interface

Only 3 chips are needed: 1 quad Inverter, IDT 74ALVC04, and 2 quad OR gates, IDT 74ALVC32. It should be noted that such a gate-based implementation scheme has not been tested or validated, but the logic is functionally equivalent to the logic synthesized in the EPLD, and the propagation delays are very similar. The PCMCIA standard is a relatively slow interface—up to 48Mb/second—which accounts for a 300ns transaction time (1 access, either I/O or memory). By comparison, the pin-to-pin propagation delays of both the EPLD and the logic gates are approximately 3 to 4 ns and are not, therefore, a factor with respect to the total cycle time.

Conclusion

Two easy-to-implement and inexpensive solutions to interface the RC32355/RC32351 integrated communications processors to the Intersil 802.11b wireless MAC have been described in this document. The EPLD-based interface has been successfully implemented on an IDT 79DB355W wireless board which, when plugged into a 79RP355 board, demonstrates the Access-Point and DSL to Wireless bridging capabilities of this combination.

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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

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