Notes

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Introduction

The IDT79RC32355 is a 32-bit microprocessor that incorporates an ATM module, an Ethernet controller, a TDM interface and a USB controller. It is well suited for a variety of gateway applications, such as integrated access devices (IADs) and small office / home office (SOHO) routers. The CPU core is built around the RISCore32300 32-bit high performance CPU core. Other specific application tasks implemented in software include firewall functions, modem emulation, and routing functions.

HiFn 7902

The HiFn 7902 is a high performance pipelined security processor that integrates a math processor and a random number generator. These blocks provide additional features to support public key cryptography. The integrated algorithms support standard network security protocols. With a minimum amount of external logic, the HiFn 7902 can be interfaced with standard processors such as the RC32355. A typical interface between the HiFn 7902 and RC32355 is shown in Figure 1 below.

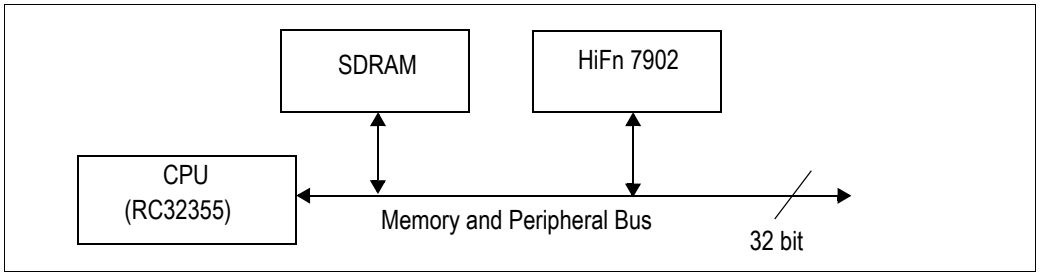

Figure 1 Implementing Security with the RC32355

Interfacing the RC32355 with the HiFn 7902

The HiFn 7902 data sheet refers to some pins, such as the address and data pins, with dual names. This application note uses the generic names to show the connections between the two processors. The RC32355 and HiFn 7902 interface is similar to an SRAM in some aspects. Data can be transferred between the CPU and the security processor using the standard load and store commands. The Memory and peripheral bus interface of the RC32355 provides the necessary signals to connect to the HiFn 7902. Since the Burst mode is not recommended for the RC32355, the HiFn 7902 will be used in single-beat transfer mode, i.e., non-burst mode. Figure 2 below shows an example interface between the two processors using the non-burst mode.

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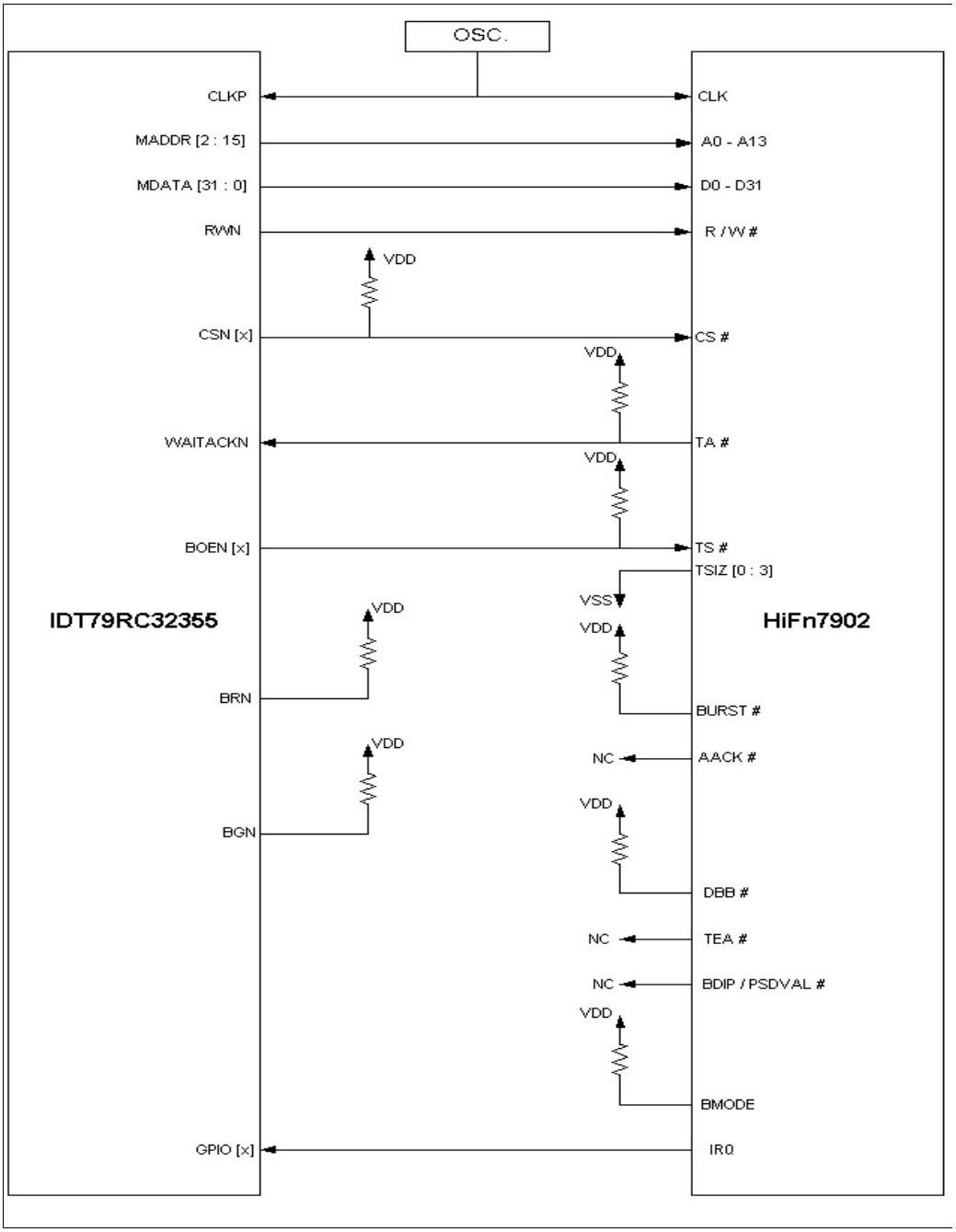

Figure 2 Example of HiFn 7902 Interface to the RC32355

The features of various pins and their interface is as described below:

CLK

The bus clock is supplied to the HiFn 7902 via this pin. The HiFn 7902 can function at clock rates between 40Mhz to 66Mhz. The RC32355 peripheral bus interface supports up to 75Mhz operation.

A0 - A13

The address bus of the HiFn 7902 is referred by dual names in the HiFn 7902 data sheet. The A0 - A13 lines are for interfacing any standard CPU to the address bus. These 14 lines are inputs to the HiFn 7902 where A0 is the LSB. The value specified on this bus indicates the memory location or register being accessed by the CPU.

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D0 - D31

Like the address bus, the data bus is given dual names. The conventional D0 - D31 indicates that the HiFn 7902 is being used with a standard processor. This bus is bi-directional and is normally an input unless a Read operation is being performed. It interfaces to the RC32355's data bus.

BURST #

This pin is used to indicate that a data transfer is a burst transfer. However, burst transfers can be done by programming parameters in the Device controller registers of the 32355. Therefore, the BURST # pin is tied to "high" to ensure that it never gets enabled.

TSIZ [0 : 3]

These pins are inputs to the HiFn 7902 and indicate the transfer size. Since BURST # is tied to high, TSIZ [0 : 1] will have values of [00]. Pins TSIZ [2 : 3] are not used and therefore tied to low to prevent the input buffers from floating.

CS #

The chip select pin is an input to the HiFn 7902 and is used along with the R/W # pin to initiate a data transfer in either direction.

TS #

Transfer start is an input to the HiFn 7902 and indicates a start of transfer. A similar function is provided by the RC32355's BOEN [x] output. This output controls the output enable for external transceivers on the peripheral bus and asserts low during read operations. Note that the timing requirements for the TS # signal are met by the BOEN [x] signals.

TA #

The transfer acknowledge pin is an output from the HiFn 7902 and indicates an end of transfer. This feature is supported by the RC32355's WAITACKN pin. This pin has a dual purpose in the RC32355. Therefore, it should be configured as the transfer acknowledge function in the device controller registers.

AACK # and DBB #

The AACK # and DBB # pins are specific pins designed in the HiFn 7902 processor to make it compatible with other processors, such as the MPC8260. The AACK # pin is left open and the DBB # pin is tied high for this interface, as recommended by HiFn.

R / W #

The read/write input pin in the HiFn 7902 is active high, when the pin is high a read operation is performed. The RC32355's RWN pin performs the same function and is therefore directly connected to the HiFn 7902.

TEA #

The transfer error acknowledge feature of the HiFn 7902 is not supported by the RC32355. This pin is left unconnected.

BDIP / PSDVAL #

Since the burst data transfers are done by configuring registers when using the RC32355, this pin is left unconnected. Its function is to indicate that a hardware burst transfer is in progress.

BMODE

As recommended in the HiFn 7902, the BMODE pin is tied high when any processor other than the MPC8260 is used.

IRQ

The interrupt request is a tri-stateable output from the HiFn 7902 processor. It can be used with one of the valid interrupts of the RC32355. The GPIO [x] pin can be used for this function. This signal is pulled high, as recommended in the HiFn 7902 data sheet.

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Timing

Note that some of the functions of the HiFn 7902 are unused, as mentioned in the section above. The functions that are used for the RC32355 and HiFn 7902 interface meet all applicable timing requirements. Specifically, the R / W # single-beat timing is met between the RC32355 and HiFn 7902.

For information on timing for the RC32355, refer to Table 6, Memory and Peripheral Bus AC Timing Characteristics, in the RC32355 Data Sheet, located at: http://www.idt.com/products/pages/Integrated_Processors-79RC32355.html.

Conclusion

Using the example interface shown in Figure 2 above, the RC32355 can be used with the HiFn 7902 for single-beat transfers. Note that this document is for reference purposes only and is intended to give the system designer a first-hand view of the interface between the two processors. The logic has not been verified or characterized by IDT.

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