CONVERTING DESIGNS USING THE LXT380/385 TO THE IDT82V2058

APPLICATION NOTE AN-356

1.0 GENERAL DESCRIPTION

The IDT82V2058 is a full featured octal E1 line interface unit and is a pin compatible, functional superset of the Intel (previously Level One) LXT380/385, octal E1 LIU. For the remainder of this document references to LXT385 also apply to the LXT380. Both devices provide the same register mapping and functions during normal operation. In addition, the IDT82V2058 offers an expanded register bank to allow increased flexibility and functionality when using a host controller. Converting designs using the LXT385 to the IDT82V2058 is a straightforward process involving minimal hardware changes. Software adjustments need only be made in applications where it is intended to access the enhanced register set of the IDT device. The primary purpose of this application note is to describe the differences between the LXT385 and the IDT82V2058 and highlight the design considerations that come into play when converting an existing LXT385 design.

2.0 REGISTERS

The register sets of the IDT82V2058 can be divided into Primary Registers and Expanded Registers. The Primary Registers of the IDT82V2058 are the same as those of the LXT385, with an added ADDP (Address Pointer) register. The address of the ADDP register in the IDT device is 1F (Hex), which is a reserved address in the LXT385. Writing "AA Hex" to this register will switch to the Expanded Registers of the IDT82V2058. (**Table 1** shows the Registers in the LXT385 and the Primary Registers in the IDT82V2058).

The functions controlled by the Expanded Registers are available only with the IDT device as the LXT385 does not offer these registers. Thus, when using only the Primary Registers, the two devices are completely software compatible but to take advantage of IDT's additional features and flexibility some software must be added to source code written for the LXT385. **Table 2** shows the Expanded Registers of the IDT82V2058. Writing "00 Hex" to the "Address Pointer " register will switch back to Primary Registers.

Table 1. Primary Register

Address (Hex)	LXT385	IDT82V2058
00 - 15	Registers	Primary Registers
16 - 1E	Reserved	Reserved
1F	Reserved	ADDP (Address Pointer), write "AA Hex" to this register will switch to Expanded Registers.

Table 2. Expanded Register

Address (Hex)	Register Name
00	e-SING (Single Rail Mode Setting)
01	e-CODE (Encoder/Decoder Selection)
02	e-CRS (Clock Recovery Enable/Disable)
03	e-RPDN (Receiver Power Down Enable/Disable)
04	e-TPDN (Transmitter Power Down Enable/Disable)
05	e-CZER (Consecutive Zero Detect Enable/Disable)
06	e-CODV (Code Violation Detect Enable/Disable)
07	e-EQUA (Equalizer Enable/Disable)
08 - 1E	Registers for testing. Default is 0, users should not change the default value
1F	ADDP, writing "00 Hex" to this register will switch to Primary Registers

3.0 WORKING WITHOUT MCLK

When MCLK is not available (High/Low), the Receive Path of the IDT82V2058 is the same as the LXT385, but the Transmit Path is different. For the IDT82V2058, if MCLK is not available, TCLK1 will be internally used as a virtual MCLK for transmit path (The status of the Receive Path is still determined by the real MCLK pin). As a result, similar operation can be achieved without an MCLK signal but, in this case, care must be taken to always supply TCLK1 for normal operation. If neither MCLK nor TCLK1 is available, the IDT82V2058 will put all the TTIPn and TRINGn in high impedance states. These operational modes are tabulated below.

4.0 EXTERNAL COMPONENTS

The transmit impedance on the line side between the IDT82V2058 and the LXT385 is slightly different. When converting an LXT385 design to the IDT82V2058, the performance will be better if the external transmit resisters and capacitor are modified. The recommended application circuit for the IDT82V2058 is shown in **Figure-1**. It is the same as that of the LXT385, except that the value of R_T is 9.5 Ohm +/- 1%. The LXT385 datasheet recommends an R_T value of 11 Ohm +/- 1%. In addition, the recommended value of C_P is 560 pF for the LXT385, whereas IDT recommends using a C_P value that is tuned to the line condition.

Table 3. MCLK and TCLK

MCLK	TCLKn (n=0-7 for LXT385) (n=0,2-7 for 2058)	Operation Mode of the Transmit Path		
		LXT385	IDT82V2058	
H/L	H	Transmit pulse-shaping is disabled.	TCLK1 is clocked	Transmit all ones
			TCLK1 is H/L	Transmit is high impedance
H/L	Clocked	Transmit with pulse-shaping	TCLK1 is clocked	Transmit with pulse-shaping
			TCLK1 is H/L	Transmit is high impedance

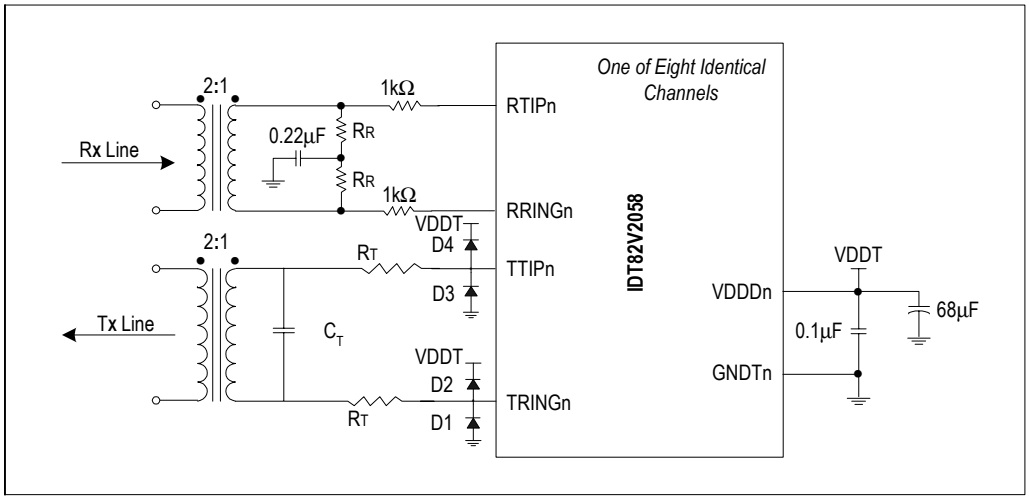

Figure 1. Recommended Application Circuit

5.0 JITTER ATTENUATOR 3DB CORNER FREQUENCY

The selection of the jitter attenuator 3dB corner frequency is different between the LXT385 and the IDT82V2058. Bit 2 in the Global Control Register (0F Hex) is named JACF bit in the LXT385, but the same bit is named JABW in the IDT82V2058. This bit and the depth of the jitter attenuator FIFO will affect the value of the jitter attenuator 3dB corner frequency in the LXT385. In the IDT82V2058, only the JABW bit will affect the jitter attenuator 3dB corner frequency. **Table 4** describes the details.

6.0 LPn SETTING (LOOP-BACK SELECTION PIN)

In hardware mode, the status of LPn pin decides the loop back configuration of the corresponding port. For "No Loop back" setting, LXT385 and IDT82V2058 are different. (Refer to **Table 5**)

7.0 JAS PIN SELECTION

In hardware mode, the status of the JAS pin (Pin # 87 QFP or Pin #J11 BGA) determines where to put the Jitter Attenuator. The LXT385 is different from the IDT82V2058 on this point. (Refer to **Table 6**)

8.0 DEFAULT VALUE OF RS REGISTER (RESET REGISTER, ADDRESS IS 0A HEX)

Writing to this register will set all registers to their default values. The default value of the RS register in the LXT385 is "00 Hex", but is "FF Hex" in the IDT82V2058.

Table 4. Jitter Attenuator 3dB Corner Frequency

	LXT385			IDT82V2058		
E1 jitter attenuator 3 dB corner frequency, host mode	32 bit FIFO	2.5 Hz	JACF does not affect this figure	JABW=0	1.7 Hz	FIFO setting does not affect this figure
	64 bit FIFO	3.5 Hz		JABW=1	6.5 Hz	
Jitter attenuator 3dB corner frequency, hardware mode	E1	3.5 Hz	JACF and FIFO do not affect this figure	E1	1.7 Hz	JACF and FIFO do not affect this figure

Table 5. LPn Setting

	LXT385	IDT82V2058
No Loop Back	LPn = Not connected	LPn = 0.5 * VDDIO
Remote Loop Back	LPn = Low	LPn = Low
Analog Loop Back	LPn = High	LPn = High

Table 6. JAS Pin Selection

JAS(IDT)/JASEL(LXT385)	JA Position in LXT385	JA Position in IDT82V2058
L	Transmit Path	Transmit Path
H	Receive Path	Receive Path
High Z	Disabled	Uncertain
VDDIO/2	Uncertain	Disabled

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