Use of x32 SDRAM Memory in the RC32355

RC32355 Application Note AN-295

Notes

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Revision History

March 29, 2001: Initial publication.

June 18, 2004: Added 2MB x32x4 (256Mb) SDRAM section.

Introduction

The RC32355 integrated processor includes a number of on-chip peripheral modules, including a memory controller. This provides a direct connection to a number of memory types, including ROM, Flash and SDRAM. The SDRAM controller supports a 32-bit wide data bus and was originally designed to link to two x16 wide SDRAM devices, four x8 SDRAM devices, or eight x4 SDRAM devices.

However, there are now a number of x32 SDRAM devices available in the marketplace. This application note outlines the considerations for using these memory types as the basis of an external memory subsystem for an RC32355-based platform.

32 Memory Support

The RC32355 is able to support two types of x32 SDRAMs:

- *0.5Mbx32x4*
- *1Mbx32x4*

In order to use such memories with the RC32355, the following guidelines should be followed:

0.5Mb x32x4 (64Mb) SDRAMs

Configure the RC32355 SDRAM controller to use the 512Kbx16x2 (16Mb) SDRAM. This will make RAS and CAS address multiplexing work as required by the x32 SDRAM.

Set the SDRAM controller in AUTO-PRECHARGE mode. This is necessary since by being configured to use the 512Kbx16x2 (16Mb) SDRAM, the RC32355 assumes the SDRAM has two banks. But the x32 SDRAM has four banks. To prevent page activation conflicts, it is necessary to open->access->close the addressed page each time the SDRAM is accessed. AUTO-PRECHARGE mode will accomplish this.

In order to access the four banks of the SDRAM, connect the MADDR[15] signal of the RC32355 to the SDRAM's BA[0] input and the MADDR[22] signal to the SDRAM's BA[1] input. Note that MADDR[22] is only available through GPIOP[27] in alternate mode.

Program the SDRAM Base & Mask registers to control 8Mbytes of memory per chip-select (each 0.5Mbx32x4 SDRAM provides 8MBytes of memory).

1Mb x32x4 (128Mb) SDRAMs

Configure the SDRAM controller on the RC32355 to use the 1Mbx16x4 (64Mb) SDRAM. This makes RAS and CAS address multiplexing work as required by the x32 SDRAM.

Program the SDRAM Base & Mask registers to control 16Mbytes of memory per chip-select (each 1Mbx32x4 SDRAM provides 16MBytes of memory).

Note: For 1Mbx32x4 (128Mb) SDRAM, enabling auto-precharge in the SDRAM controller is NOT necessary because both the 1Mbx32x4 (128Mb) SDRAM and the 1Mbx16x4 (64Mb) SDRAM happen to have the same # of banks, same # of pages, and the same page size.

DSC 6005

Notes

2Mb x32x4 (256Mb) SDRAMs

Configure the SDRAM controller on the RC32355/RC32351 to use the 2Mbx16x4 (128Mb) SDRAM. This makes RAS and CAS address multiplexing work as required by the x32 SDRAM. Program the SDRAM Base & Mask registers to control 32Mbytes of memory per chip-select (each 2Mbx32x4 SDRAM provides 32MBytes of memory).

Note: For 2Mbx32x4 (256Mb) SDRAM, enabling auto-precharge in the SDRAM controller is NOT necessary because both the 2Mbx32x4 (256Mb) SDRAM and the 2Mbx16x4 (128Mb) SDRAM happen to have the same # of banks, same # of pages, and the same page size.

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