BUS MATCHING WITH IDT FIFOs

BUS MATCHING

The Bus Matching feature offered in the SuperSync II family is a powerful feature designed to eliminate external MUXes. When used in applications where no parity data is passed to the FIFO, bus mapping between the FIFO buses and external buses becomes an important issue. When designing with 36-bit FIFOs and an application that operates on 8-bit bytes, 16-bit words, or 32-bit longs, care must be taken when matching the buses with the FIFO. The FIFO operates on 9-bit boundaries instead of 8-bit boundaries to allow externally generated parity data to pass through the FIFO.

x36 → x9			
"x32 → x8"			
BM	IW	OW	IP
H	L	H	H

The following diagrams show how an external byte-oriented bus should be mapped to the 9-bit oriented FIFO.

x32 → x8 INTERSPERSED

In this case, on the input, every 9th bit is skipped so when the bytes are read out they will map directly to Q0-7. Notice how external input bus D8-15 maps to FIFO D9-16, external input bus D16-23 maps to FIFO D18-25, and external input bus D24-31 maps to FIFO D27-34.

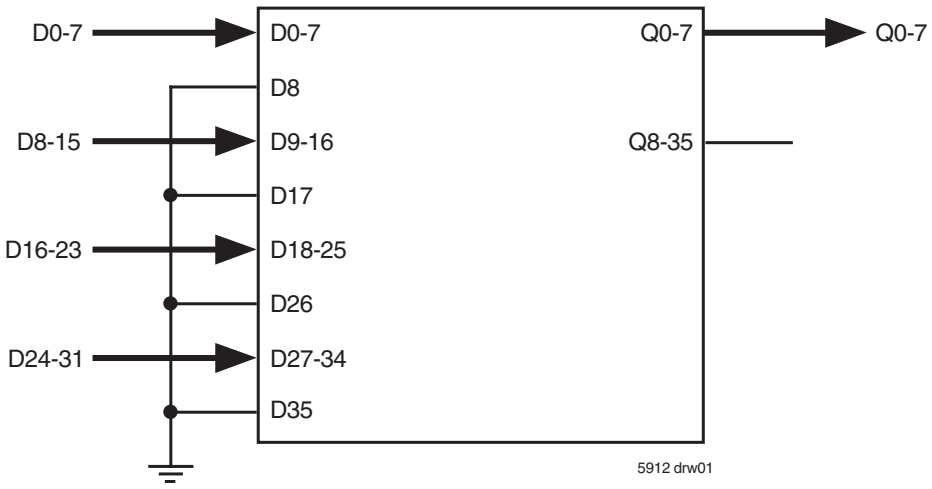


Figure 1. 32-bit input to 8-bit output bus matching

NOTE:

IP is only effective during offset register programming via the parallel data input port and offset register reading via the parallel data output port. IP does not effect words being written into or read from the FIFO memory as data.

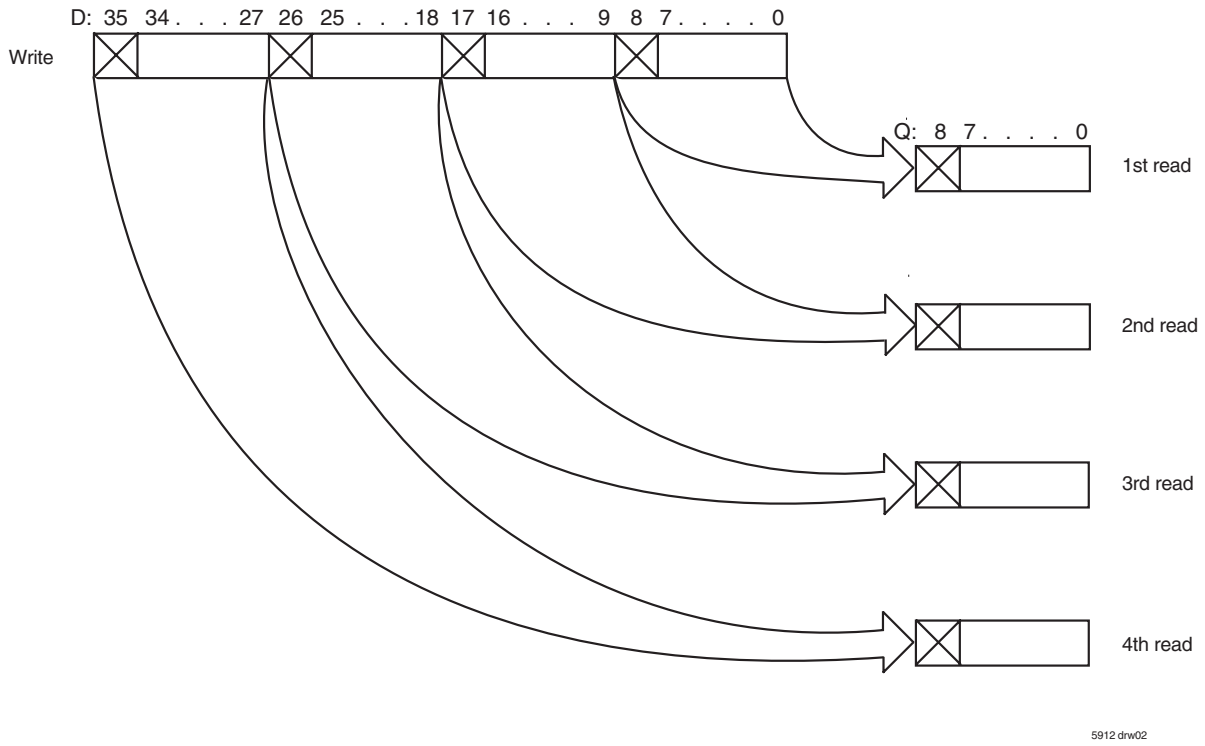


Figure 2. 32-bit input to 8-bit output with little endian and interspersed parity

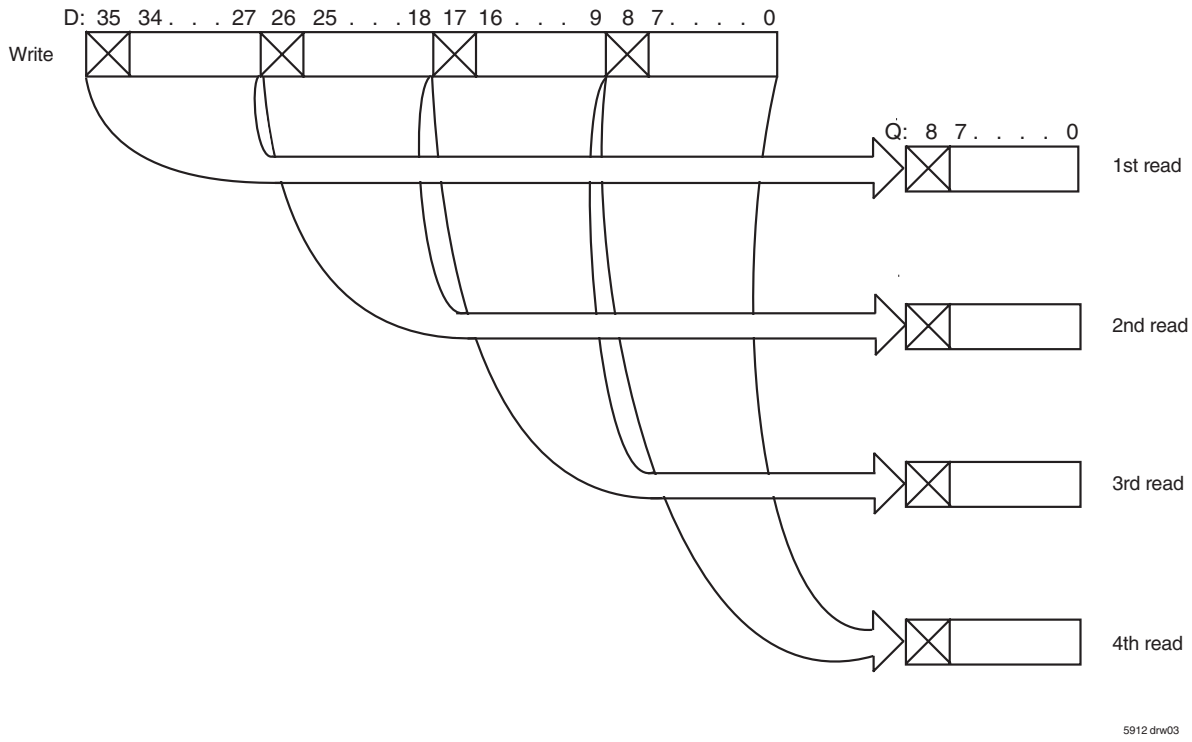


Figure 3. 32-bit input to 8-bit output with big endian and interspersed parity

x32 → x16 INTERSPERSED

In this case, on the input and the output, every 9th bit is skipped so when the bytes are read out they will map directly to Q0-7 and Q9-16. Notice how the external input bus D8-15 maps to FIFO D9-16, external input bus D16-23 maps to FIFO D18-25, and external input bus D24-31 maps to FIFO D27-34. This is true of the read bus as well: FIFO Q9-16 maps to external read bus Q8-15.

x36 → x18			
"x32 → x16"			
BM	IW	OW	IP
H	L	L	H

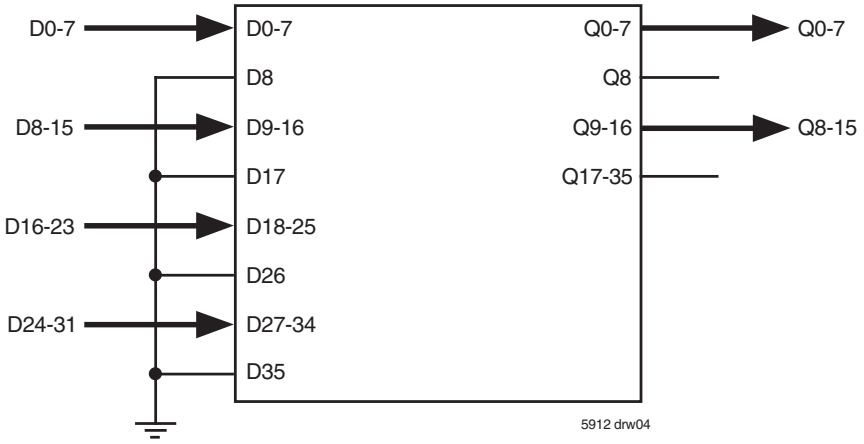


Figure 4. 32-bit input to 16-bit output bus matching

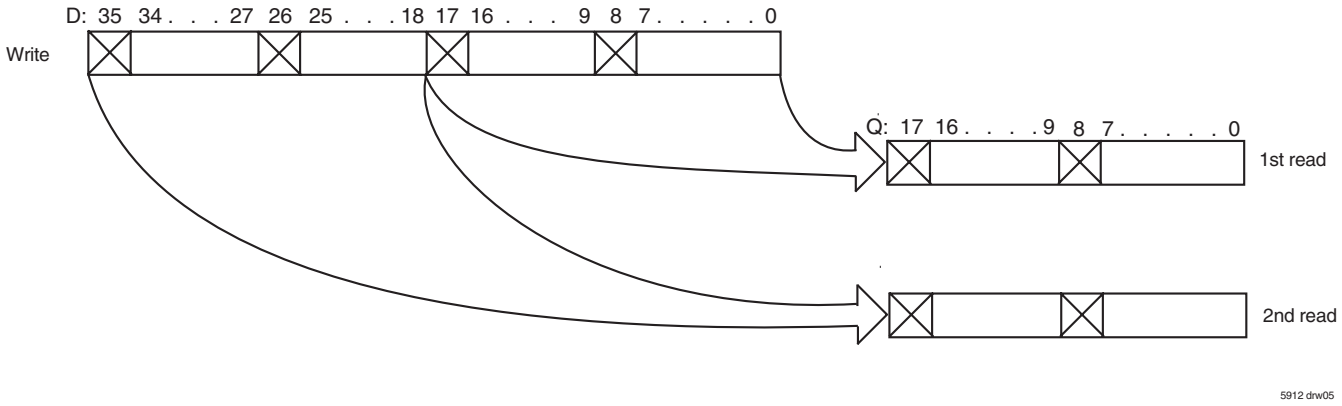


Figure 5. 32-bit input to 16-bit output with little endian and interspersed parity

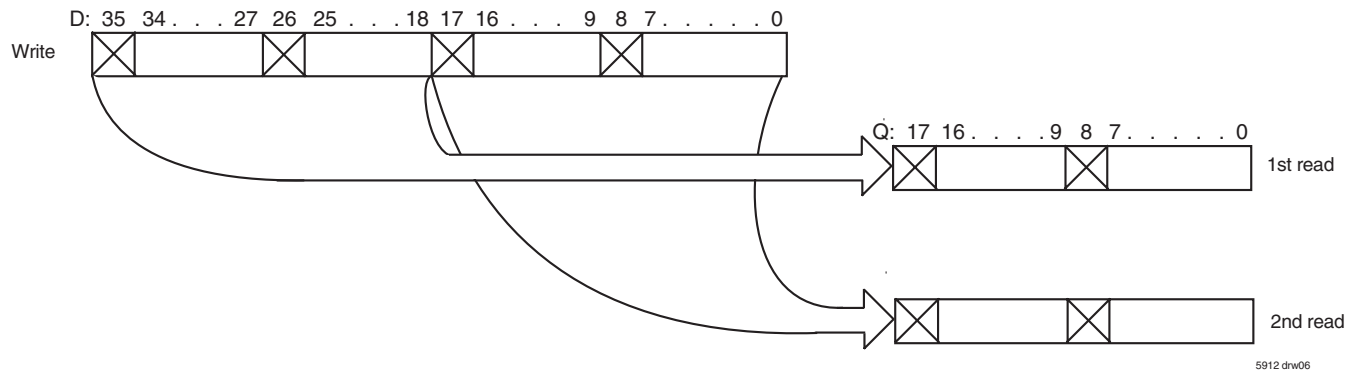


Figure 6. 32-bit input to 16-bit output with big endian and interspersed parity

x32 → x16 NON-INTERSPERSED

This configuration is similar to the previous, but in this case bits 16 and 17, and bits 34 and 35 are skipped. In this way, when 18-bit words are read out the two MSBs will be ignored leaving Q0-15 as the data read. Notice how external input bus D15-31 maps to FIFO D18-33. This configuration cannot be used with large density FIFOs (IDT72V36110 - - 4Megabit and larger) while also allowing programmable offset flags. The $\overline{PAE}$ and $\overline{PAF}$ offset registers are wider than 16 bits. In this case, the recommended interspersed methodolgy is recommended, (see Figure 4).

x36 → x18			
"x32 → x16"			
BM	IW	OW	IP
H	L	L	L

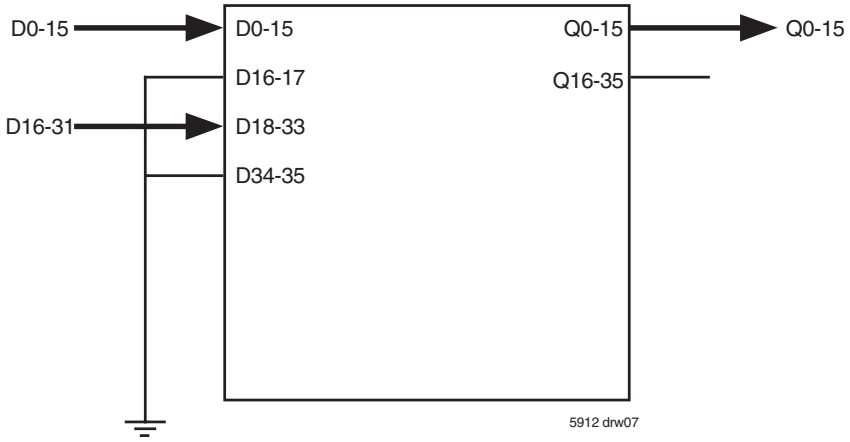


Figure 7. 32-bit input to 16-bit output bus matching

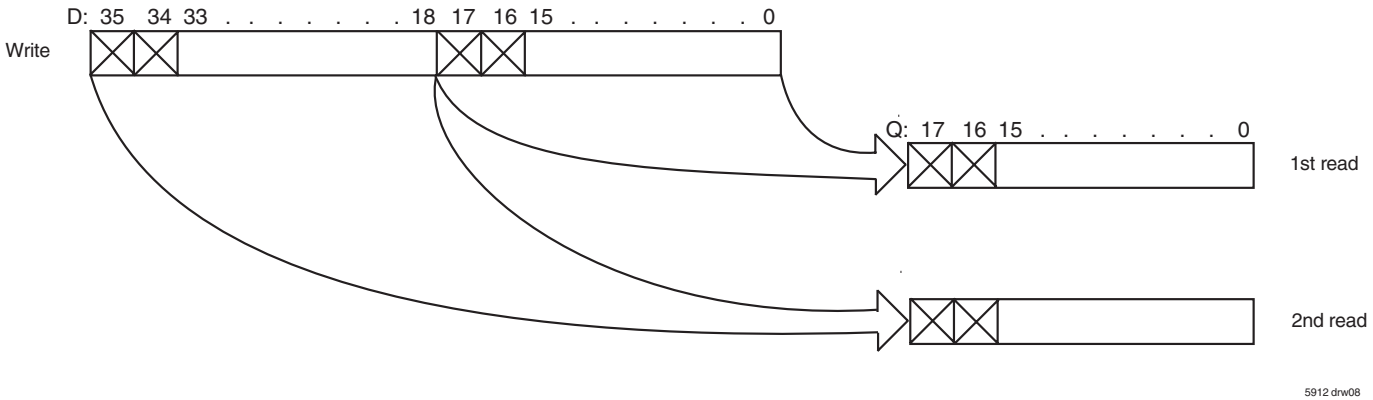


Figure 8. 32-bit input to 16-bit output with little endian and non-interspersed parity

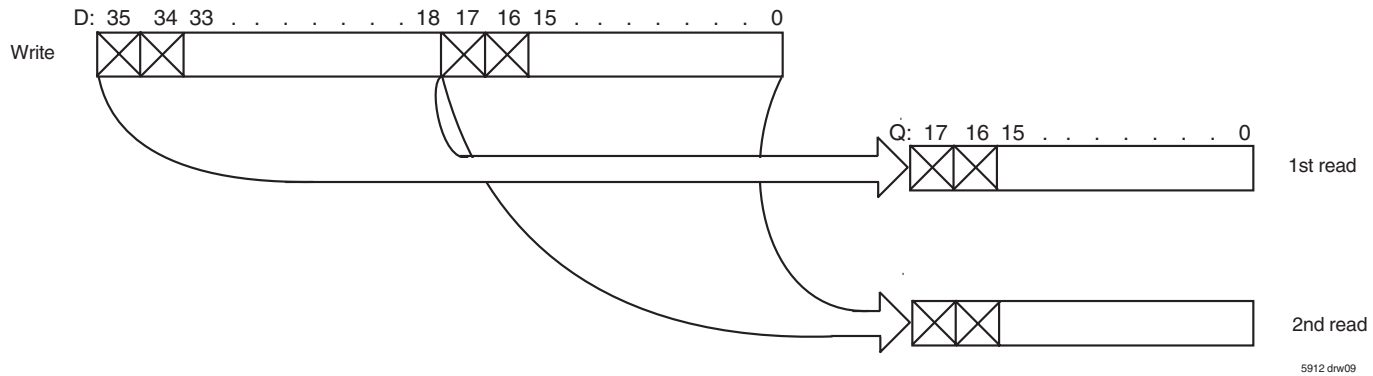


Figure 9. 32-bit input to 16-bit output with big endian and non-interspersed parity

x32 → x32 INTERSPERSED

In this case, on the input and the output, every 9th bit is skipped. Notice how external input bus D8-15 maps to FIFO D9-16, external input bus D16-23 maps to FIFO D18-25, and external input bus D24-31 maps to FIFO D27-34. This is true of the read bus as well.

x36 → x36			
"x32 → x32"			
BM	IW	OW	IP
L	L	L	H

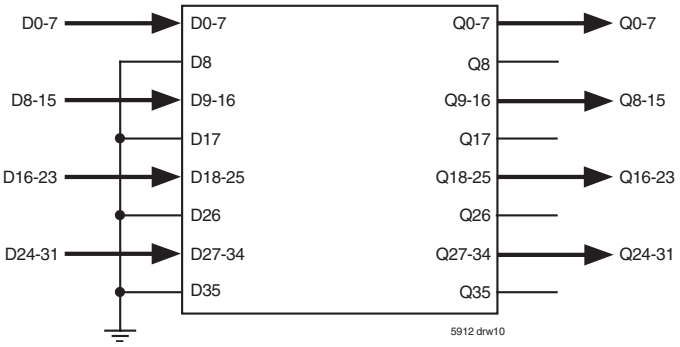


Figure 10. 32-bit input to 32-bit output bus matching

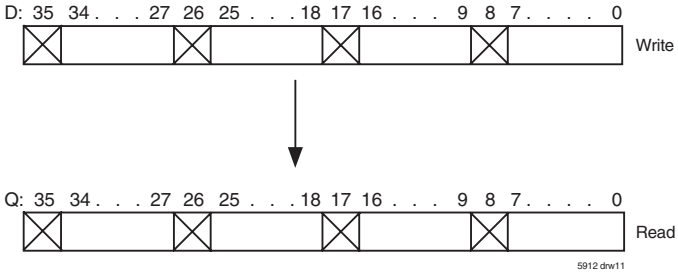


Figure 11. 32-bit input to 32-bit output with interspersed parity

x32 → x32 NON-INTERSPERSED

This configuration is similar to the previous, but in this case bits 32-35 are skipped. Notice how external input bus D0-31 maps to FIFO D0-31.

x36 → x36			
"x32 → x32"			
BM	IW	OW	IP
L	L	L	L

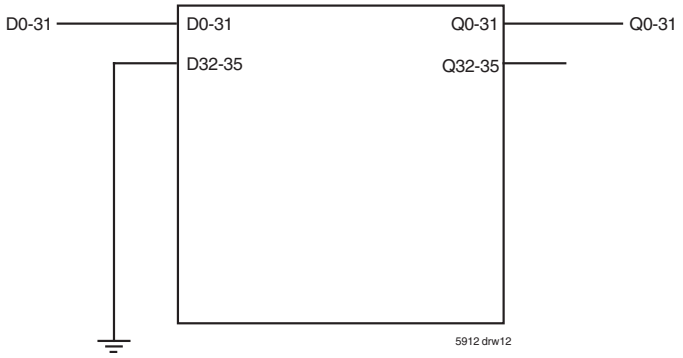


Figure 12. 32-bit input to 32-bit output bus matching

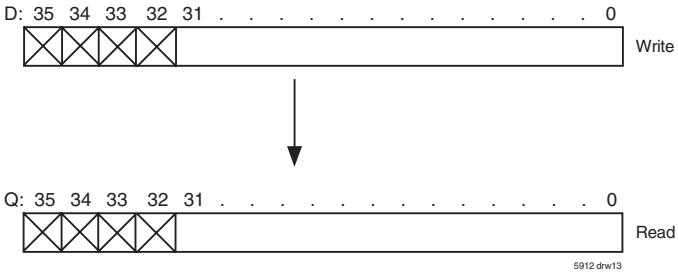


Figure 13. 32-bit input to 32-bit output with non-interspersed parity

x16 → x32 NON-INTERSPERSED

This configuration is similar to Figure 7 but the matching is on the other port. In this case bits 16 and 17, and bits 34 and 35 are skipped on the output. In this way, when 16-bit words are written, the two MSBs can be ignored leaving Q0-15 as the data to be read. Notice how external output bus Q16-31 maps to FIFO Q18-33.

x18 → x36			
"x16 → x32"			
BM	IW	OW	IP
H	H	L	L

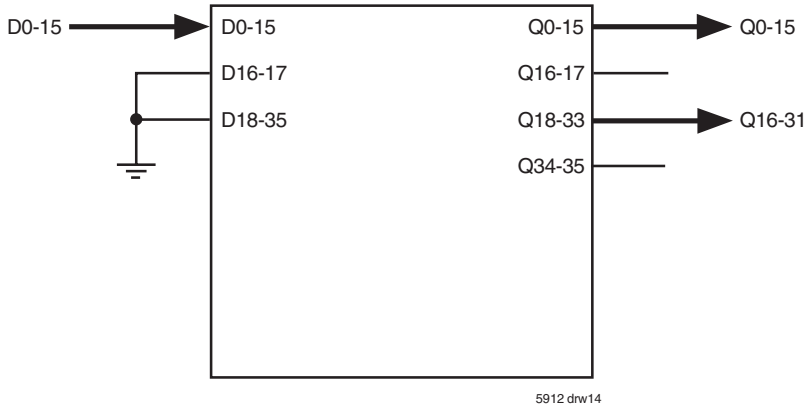


Figure 14. 16-bit input to 32-bit output bus matching

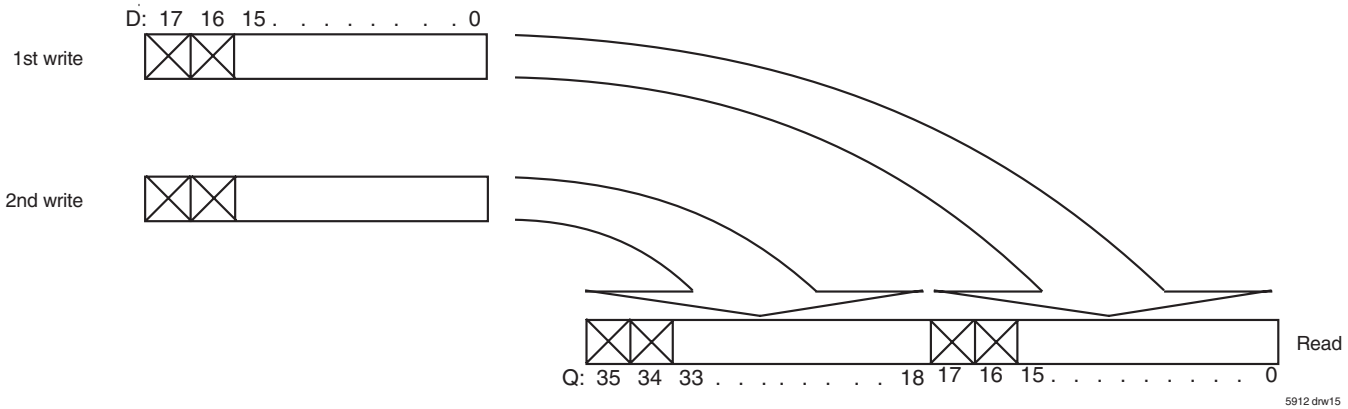


Figure 15. 16-bit input to 32-bit output with little endian and non-interspersed parity

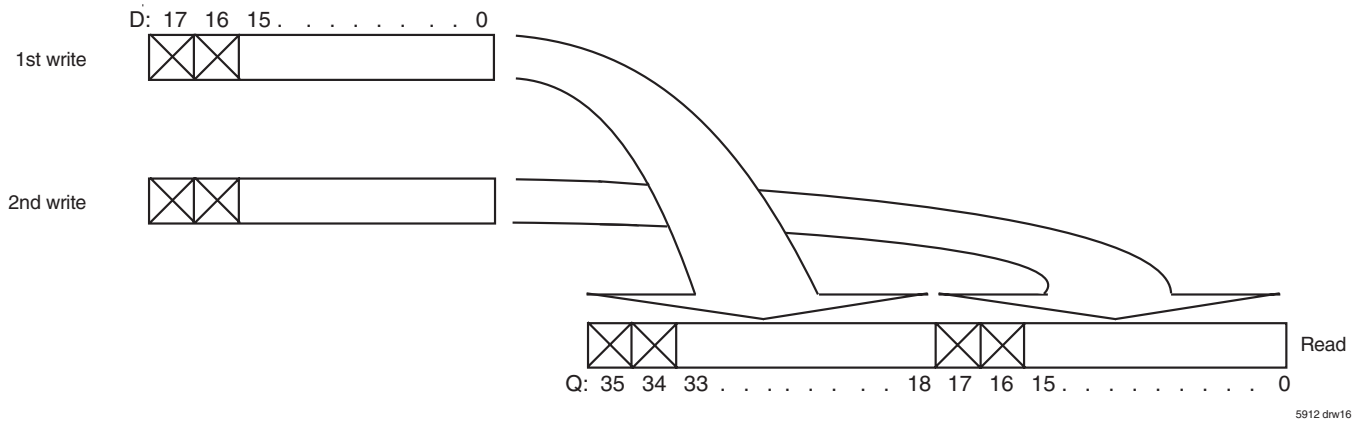


Figure 16. 16-bit input to 32-bit output with big endian and non-interspersed parity

x16 → x32 INTERSPERSED

This configuration is similar to Figure 4, but in this case, on the input and the output, every 9th bit is skipped. Notice how external input bus D8-15 maps to FIFO D9-16, external output bus Q8-15 maps to FIFO Q9-16, external output bus Q16-23 maps to FIFO Q18-25, and external output bus Q24-31 maps to FIFO Q27-34.

x18 → x36			
"x16 → x32"			
BM	IW	OW	IP
H	H	L	H

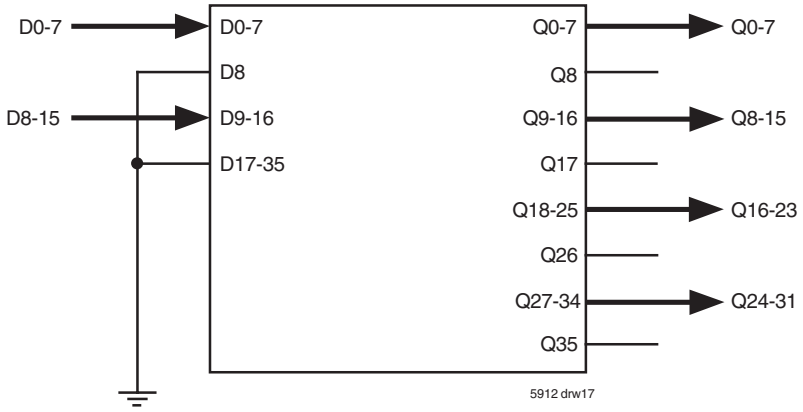


Figure 17. 16-bit input to 32-bit output bus matching

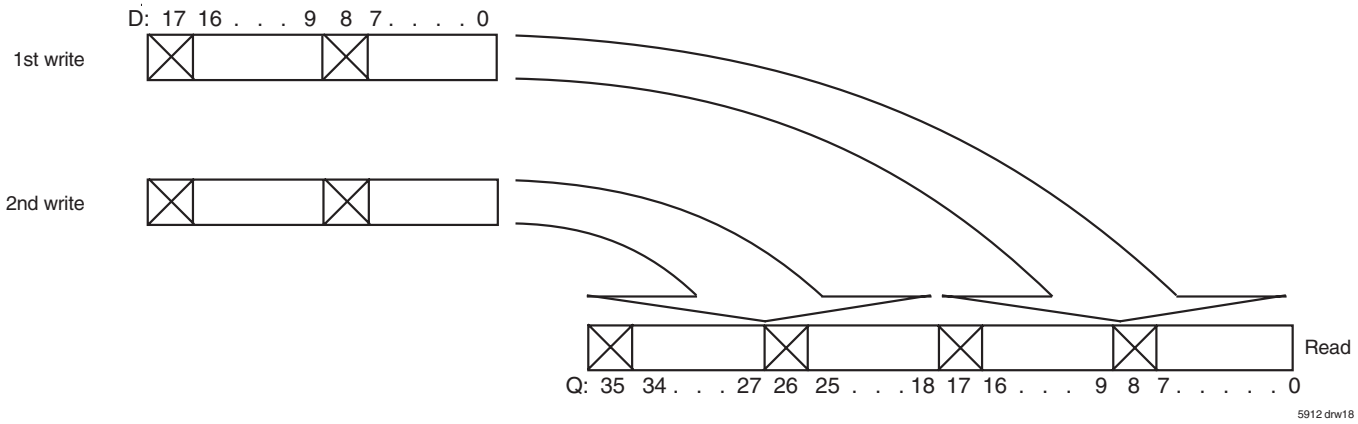


Figure 18. 16-bit input to 32-bit output with little endian and interspersed parity

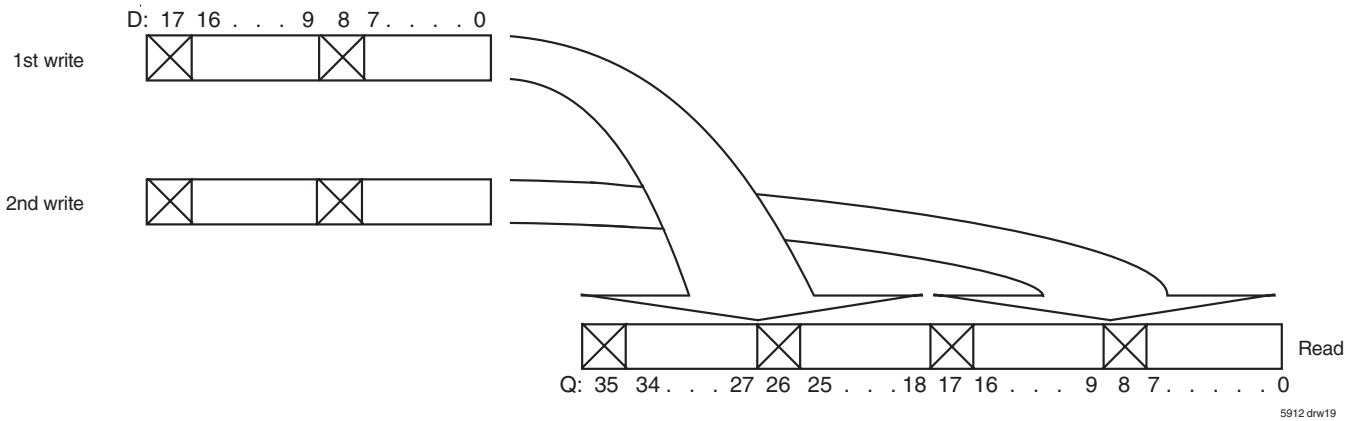


Figure 19. 16-bit input to 32-bit output with big endian and interspersed parity

x8 → x32 INTERSPERSED

This configuration is similar to Figure 1, but in this case, on the output, every 9th bit is skipped so when the bytes are written in they will map directly to Q0-7, Q9-16, Q18-25, and Q27-34. Notice how the external output bus Q8-15 maps to FIFO Q9-16, external output bus Q16-23 maps to FIFO Q18-25, and external output bus Q24-31 maps to FIFO Q27-34.

x9 → x36			
"x8 → x32"			
BM	IW	OW	IP
H	H	H	H

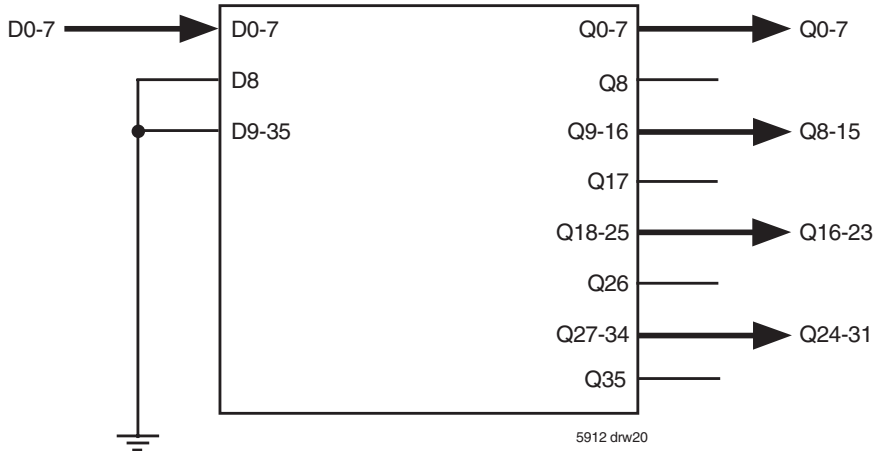


Figure 20. 8-bit input to 32-bit output bus matching

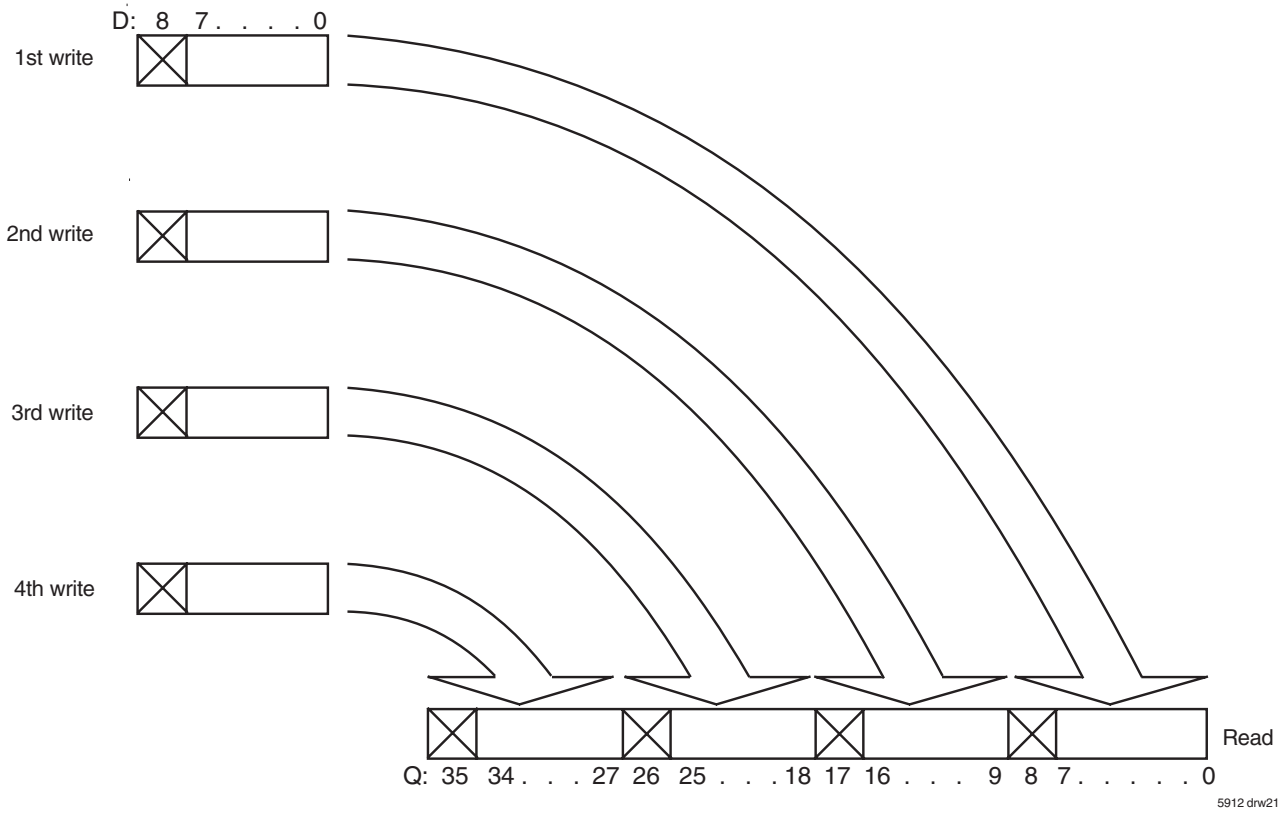


Figure 21. 8-bit input to 32-bit output with little endian and interspersed parity

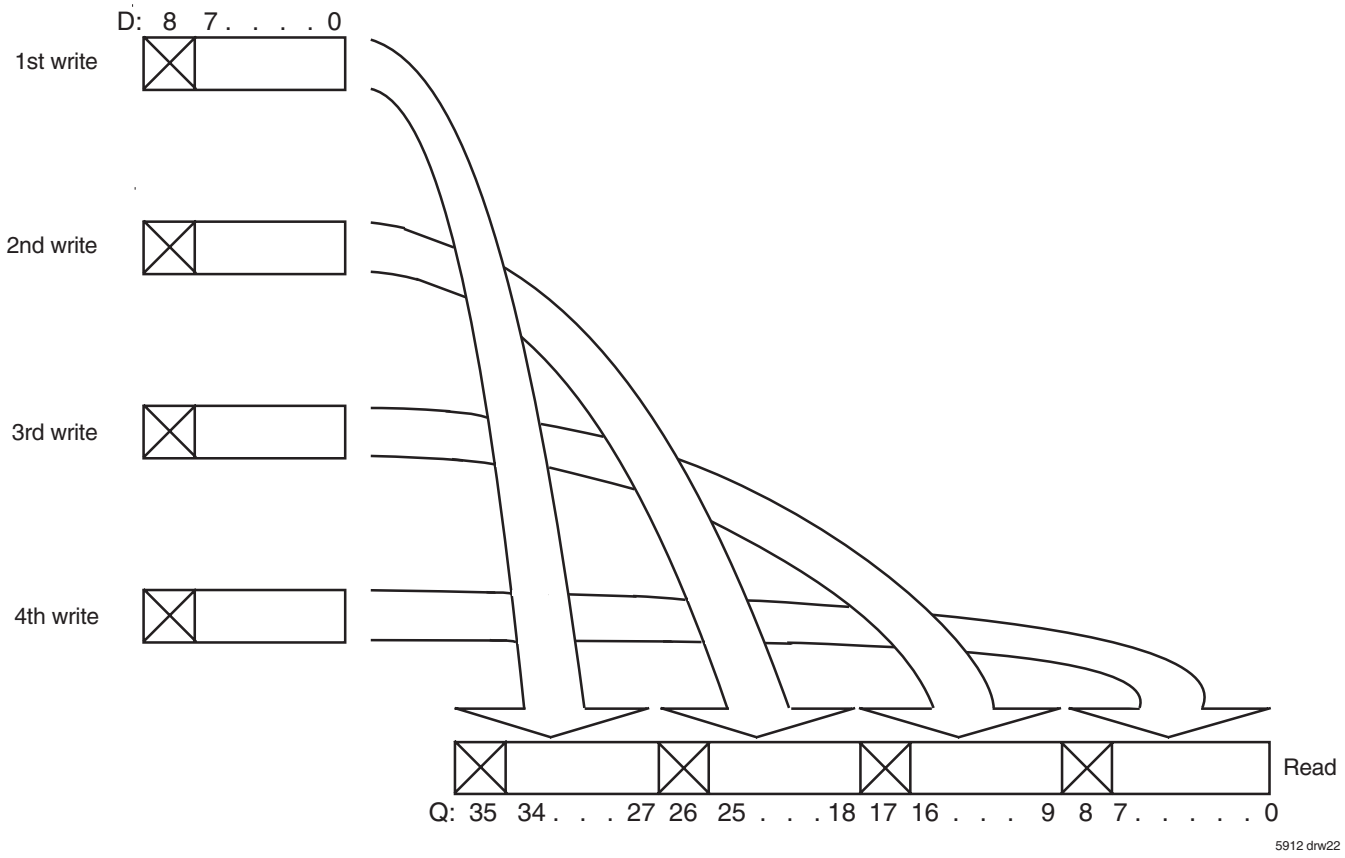


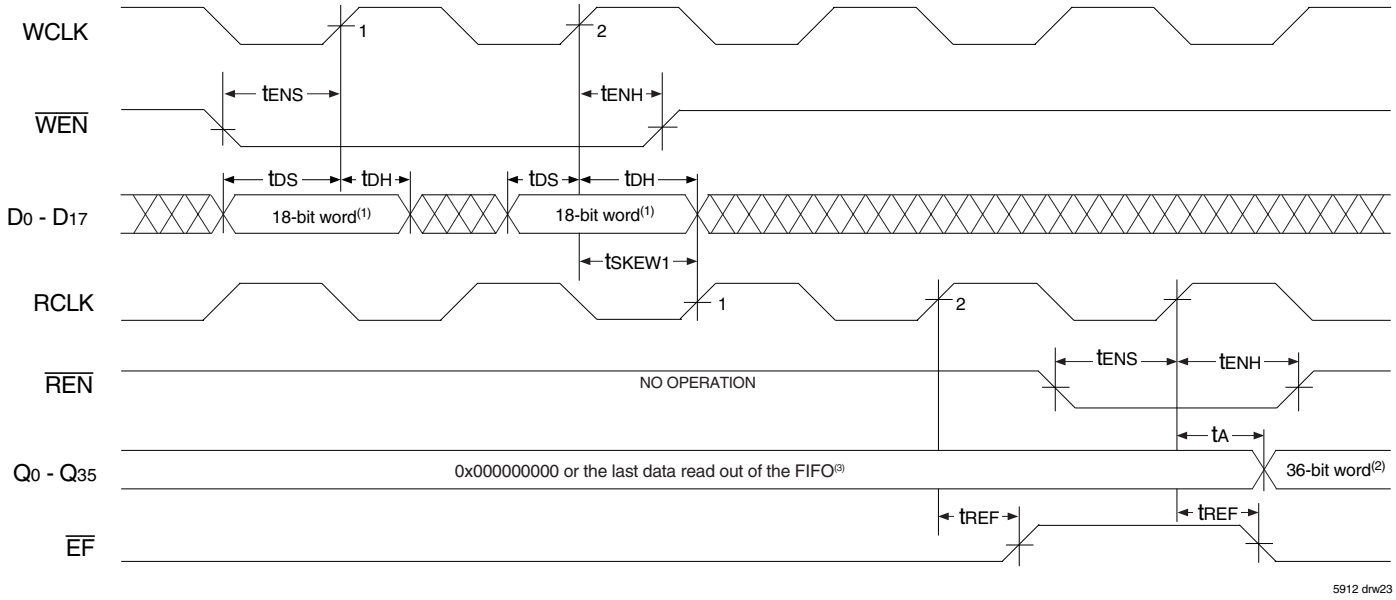
Figure 22. 8-bit input to 32-bit output with big endian and interspersed parity

FLAG OPERATION

When implementing the Bus Matching feature, the read and write operations will function slightly different from the normal Non-Bus Matching mode. The user needs to be aware that a single write cycle to the FIFO will not equal a single read cycle from the FIFO. In other words, the number of writes to reads is dependent upon the configuration of the input and output bus widths, and vice versa. The following pages will illustrate the differences between the read/write cycles and status flags of Bus Matching versus Non-Bus Matching mode.

The Bus Matching configuration determines how the data will be written/read from the FIFO. In a x36-in to x18-out configuration, each 36-bit word written into the FIFO will require two 18-bit read cycles to send the 36-bit word to the output register. The FIFO reads on 18-bit boundaries. The same methodology applies when the input bus is greater than the output bus. In the case of a x9-in to x36-out configuration, in order for a valid read operation to take place four 9-bit write cycles must first be executed.

Another issue is functionality of the status flags. Status flags are not asserted the same way as in the Non-Bus Matching mode. The diagram below shows the relationship between the empty flag and the read/write cycle. In this case the two 18-bit words are first written into the FIFO and the empty flag will be asserted after the second write cycle, not the first. It will be deasserted after the 36-bit word has been read out.

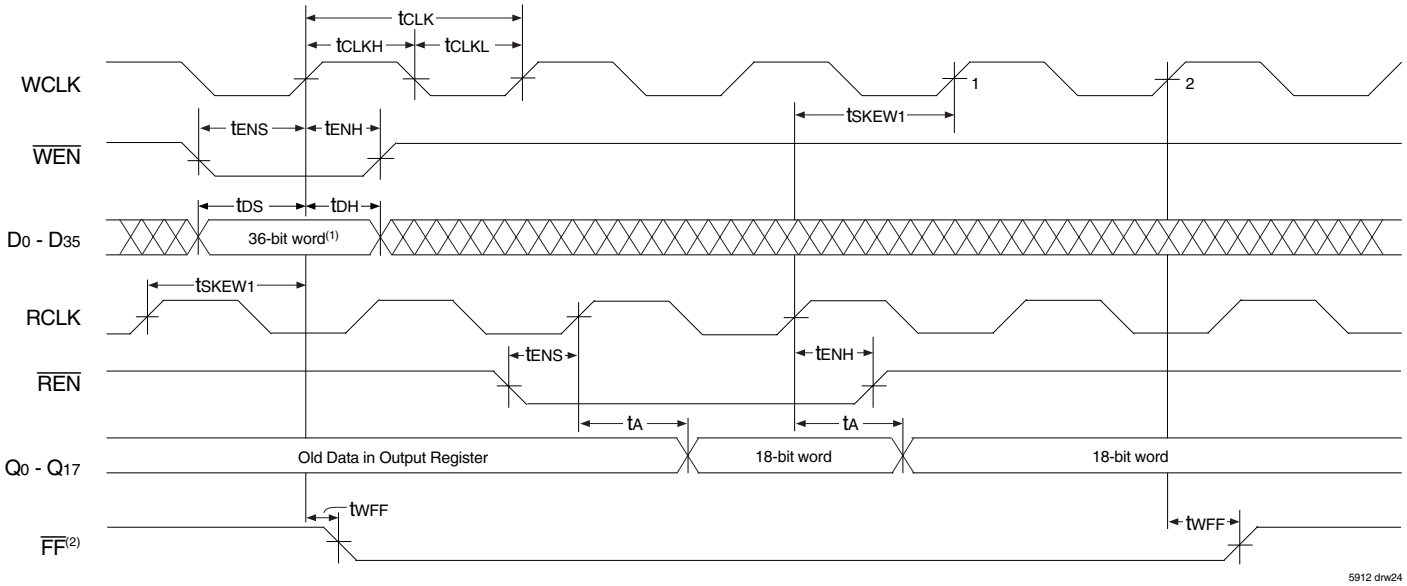


NOTES:

1. The two 18-bit words are the first words written into the empty FIFO. It will take two read clock cycles (after the last WCLK cycle plus t_{REF}) before $\overline{EF}$ will go HIGH.
2. t_{SKEW1} is the minimum time between a rising WCLK edge and a rising RCLK edge to guarantee that $\overline{EF}$ will go HIGH (after one RCLK cycle plus t_{REF}). If the time between the rising edge of WCLK and the rising edge of RCLK is less than t_{SKEW1}, then $\overline{EF}$ deassertion may be delayed one extra RCLK cycle.
3. After $\overline{MRS}$, output register is reset to zero.

Figure 23. x18-in to x36-out Bus Matching Two Write Cycles and Empty Flag Timing (IDT Standard Mode).

Here is a diagram that shows a x36 bit in to x18-out configuration. Notice now the write operation takes only one clock cycle to write a 36-bit word. However, now it will take two read clock cycles to read the 36-bit word, at 18-bit boundaries per RCLK. The full flag will go HIGH after two RCLK cycles instead of one.

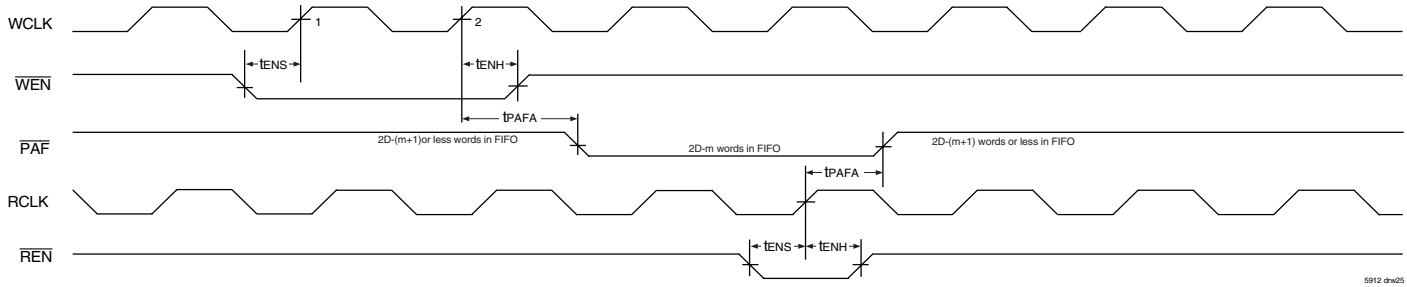


NOTES:

1. The 36-bit word is the last word written to make the FIFO full.
2. $\overline{FF}$ is updated synchronous to the rising edge of WCLK. It will go LOW after the write operation (plus t_{WFF}). If t_{SKEW} between RCLK and WCLK is less than t_{SKEW1}, updating $\overline{FF}$ may be delayed one extra WCLK edge.
3. t_{SKEW1} is the minimum time between a rising RCLK edge and a rising WCLK edge to guarantee that $\overline{FF}$ will go HIGH (after one WCLK cycle plus t_{WFF}). If the time between the rising edge of the RCLK and the rising edge of the WCLK is less than t_{SKEW1}, then the $\overline{FF}$ deassertion may be delayed one extra WCLK cycle.

Figure 24. x36-in to x18-out Bus Matching Two Read Cycles and Full Flag Timing.

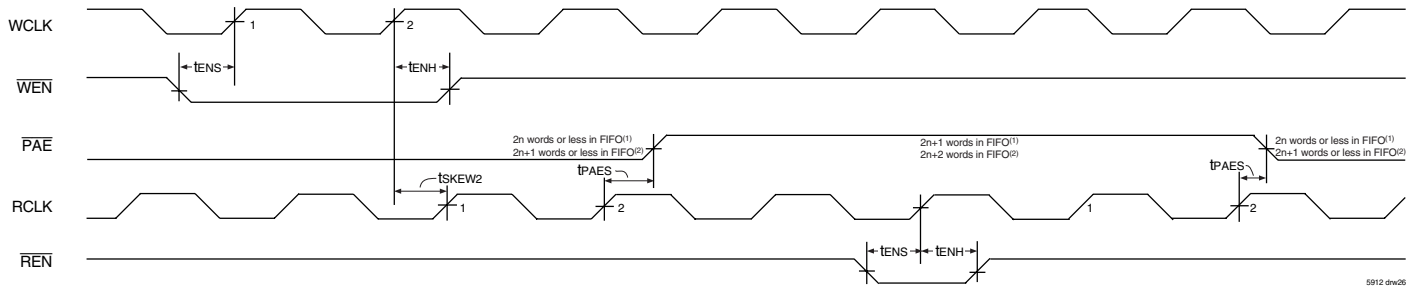
The Bus Matching feature also affects the programmable offset flags. For example, $\overline{PAF}$ will go LOW when 2D-m words are written into the FIFO for a x18-in to x36-out configuration. D is the density of the FIFO and m is the user programmable offset value. Similarly, the $\overline{PAE}$ will go HIGH when there are 2n+1 words written into the FIFO, where n is the user programmable offset value. Below is the timing diagram of the programmable offset flags as well a chart showing when the offset flags will be asserted.



Configuration	Minimum number of words to assert $\overline{PAF}$
x9 to x36	4D - m
x18 to x36	2D - m
x36 to x36	D - m
x36 to x9	D - m
x36 to x18	D - m

NOTES:
1. m = $\overline{PAF}$ offset.
2. D = Maximum FIFO depth.

Figure 25. x18-in to x36-out Bus Matching Asynchronous Programmable Almost-Full Flag Timing.



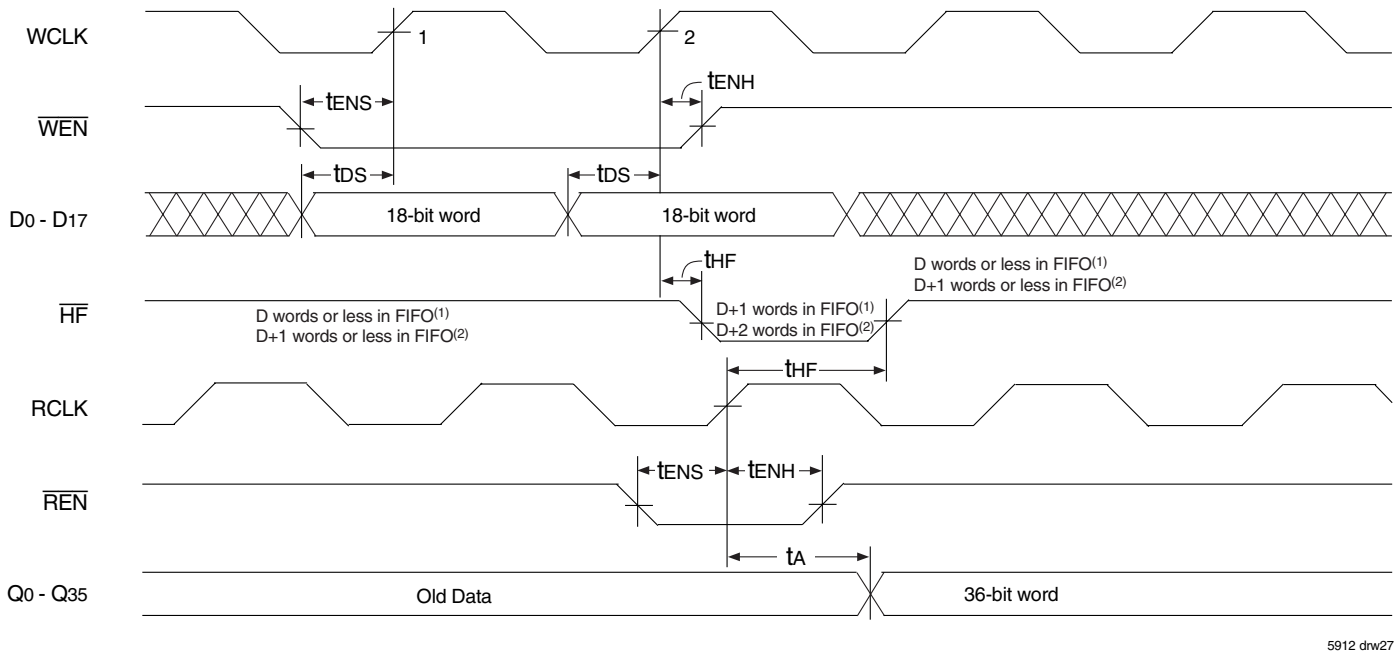
Configuration	Minimum number of words to assert $\overline{PAE}$ (Standard Mode)	Minimum number of words to assert $\overline{PAE}$ (FWFT Mode)
x9 to x36	4n	4n + 1
x18 to x36	2n	2n + 1
x36 to x36	n	n + 1
x36 to x18	n	n + 1
x36 to x9	n	n + 1

NOTES:
1. For IDT standard mode.
2. For FWFT mode.
3. n = $\overline{PAE}$ offset.

Figure 26. x18-in to x36-out Bus Matching Synchronous Programmable Almost-Empty Flag Timing.

The Bus Matching feature also affects the half flag. For example, the half flag goes LOW when the device is half full for Non-Bus Matching Mode. That is, when there are D/2 + 1 words in the FIFO, where D is the density of the FIFO. However, this will not be the case for Bus Matching mode. For instance, in a x18 to x36 configuration, it will take D + 1 words assert $\overline{HF}$ LOW. This is because we are writing in 18 bit words instead of 36, and thus it takes twice as many words to fill the FIFO. The timing diagram below shows each write cycle will write an 18-bit word into the FIFO. Thus the number of words to make the FIFO half full will be twice as much as for Non-Bus Matching Mode.

The full flag will be affected the same way as the half flag. That is, it will take twice as many words (or write cycles) for the full flag to be asserted in x18 to x36 configuration. The table below shows the number of writes it takes to assert the half and full flags for different modes and configurations.



Configuration	Minimum number of words to assert $\overline{HF}$ (Standard Mode)	Minimum number of words to assert $\overline{HF}$ (FWFT Mode)
x9 to x36	2D + 1	2D + 2
x18 to x36	D + 1	D + 2
x36 to x36	$\frac{D}{2}$ + 1	$\frac{D-1}{2}$ + 2
x36 to x18	$\frac{D}{2}$ + 1	$\frac{D+1}{2}$ + 2
x36 to x9	$\frac{D}{2}$ + 1	$\frac{D+1}{2}$ + 2

Configuration	Minimum number of words to assert $\overline{FF}$ (Standard Mode)	Minimum number of words to assert $\overline{FF}$ (FWFT Mode)
x9 to x36	4D	4D + 1
x18 to x36	2D	2D + 1
x36 to x36	D	D + 1
x36 to x18	D	D + 1
x36 to x9	D	D + 1

NOTES:

1. In IDT Standard Mode D is the maximum depth of FIFO.
2. In FWFT Mode D is the maximum depth of FIFO.

Figure 27. x18-in to x36-out Bus Matching Half-Full Flag Timing, Table and Full Flag Table.

INTERSPERSED PARITY

Although SuperSync II FIFOs do not contain any parity checking hardware, the FIFO buses are wider to accommodate parity data through the FIFO. The IP pin on the FIFO is related strictly to the programming of the flags and relates to how the external data buses align with the FIFO internal registers. In a bus matching application where the flags are programmed, the interspersed parity mode will likely need to be used to load valid data and not the parity data into the $\overline{PAE}$ and $\overline{PAF}$ offset registers. The following diagrams show which bits are valid with and without the interspersed parity.

IP is only effective during offset register programming via the parallel data input port and offset register reading via the parallel data output port. IP does not effect words being written into or read from the FIFO memory as data.

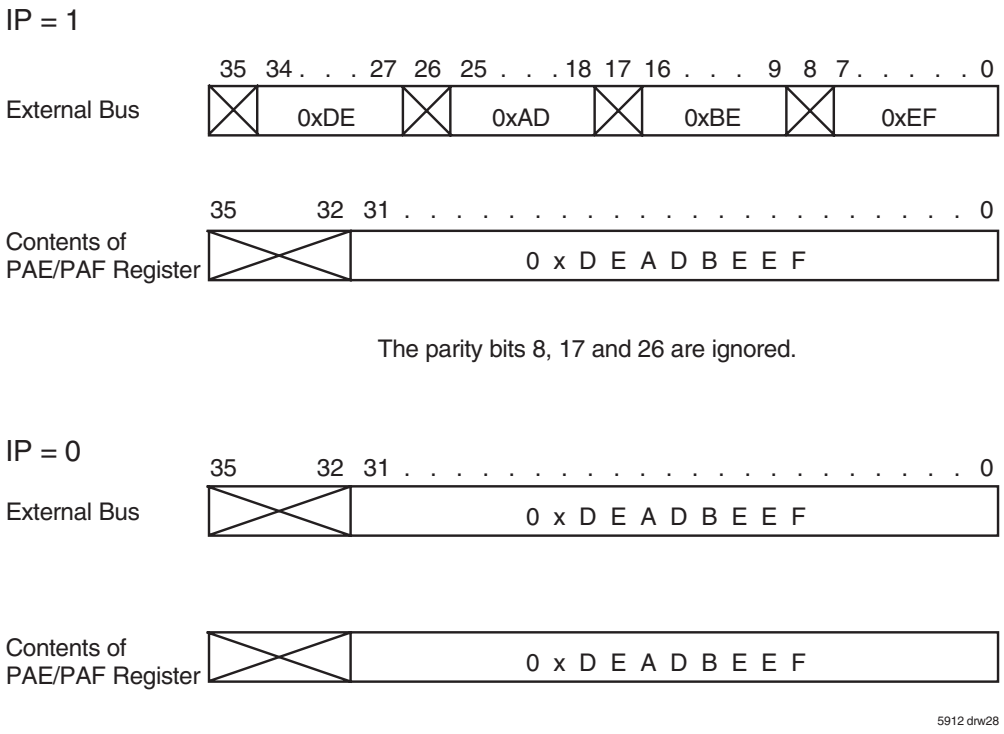


Figure 28. The relationship between external bus and internal offset register

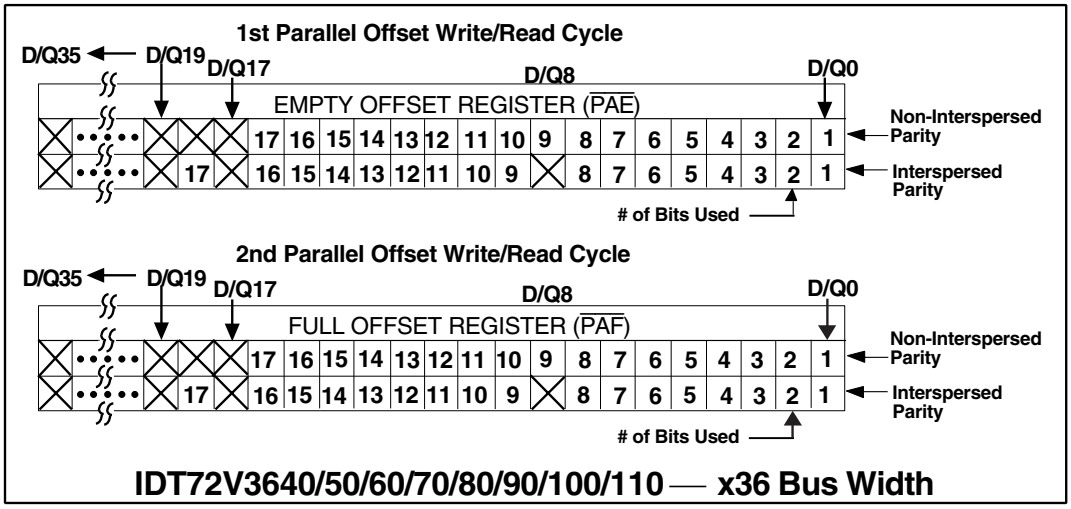


Figure 29. Parallel Offsets with x36 Bus Width

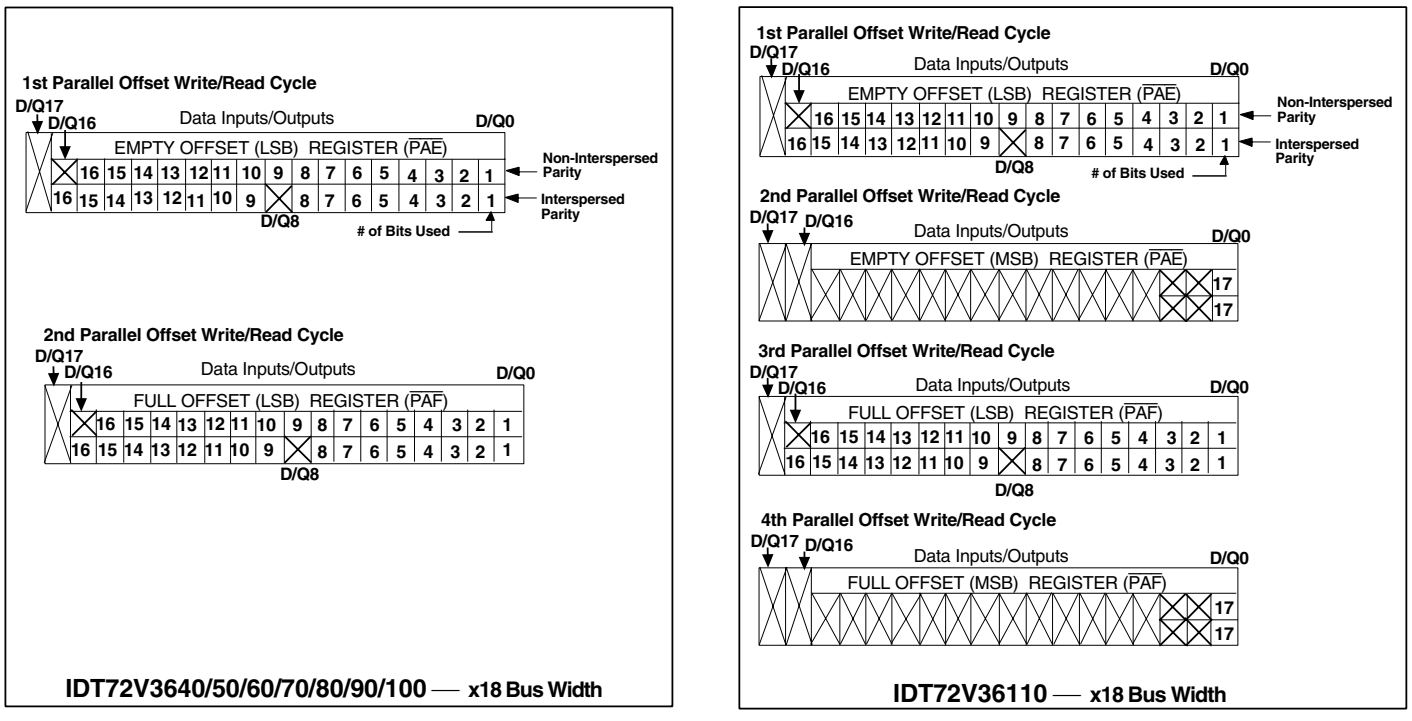
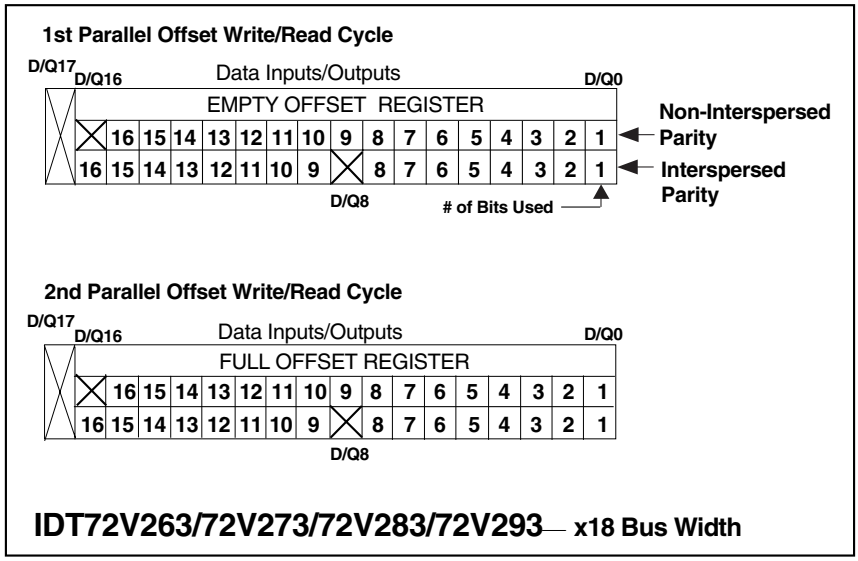


Figure 30. Parallel Offsets with x18 Bus Width



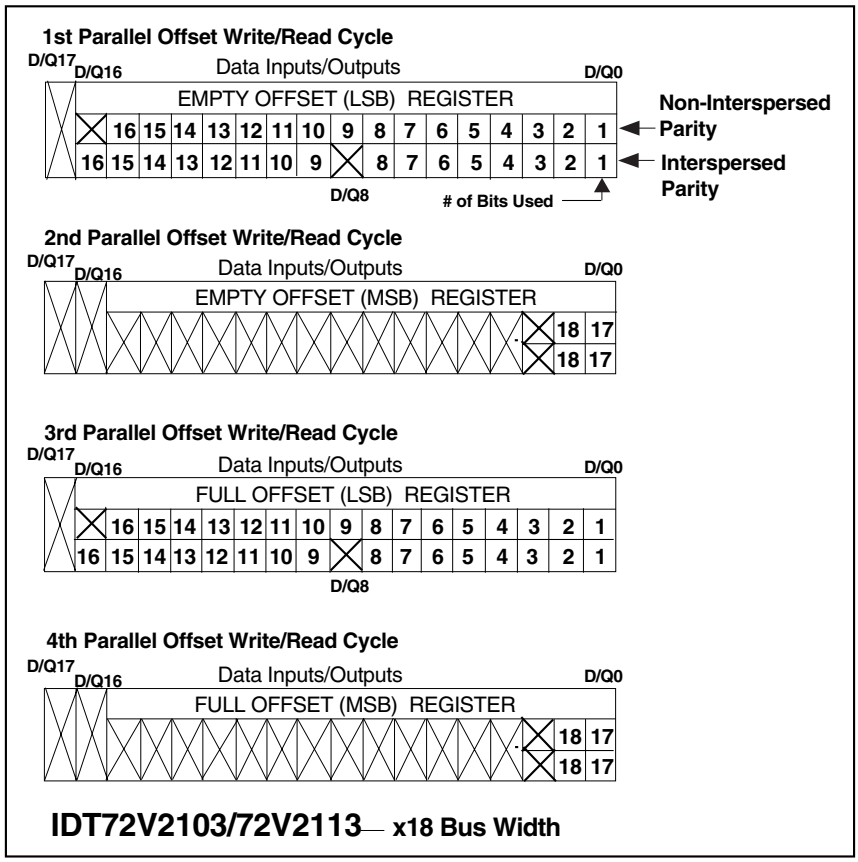


Figure 30. Parallel Offsets with x18 Bus Width (Continued)

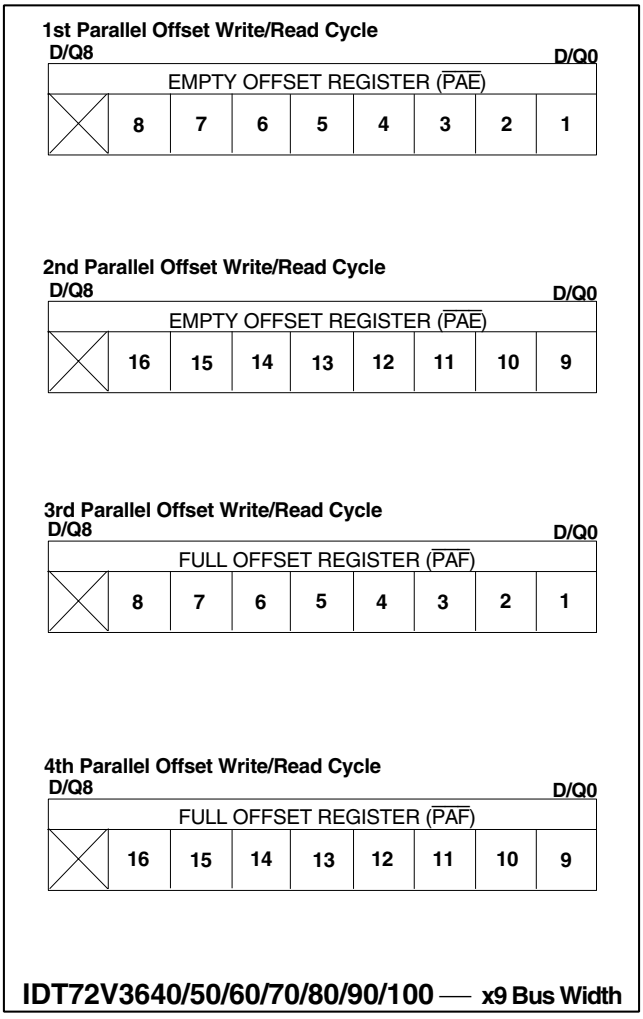
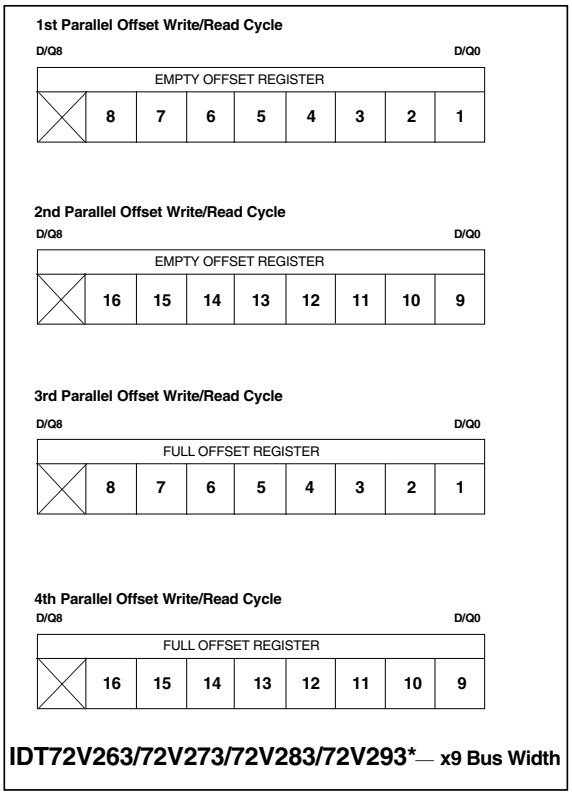
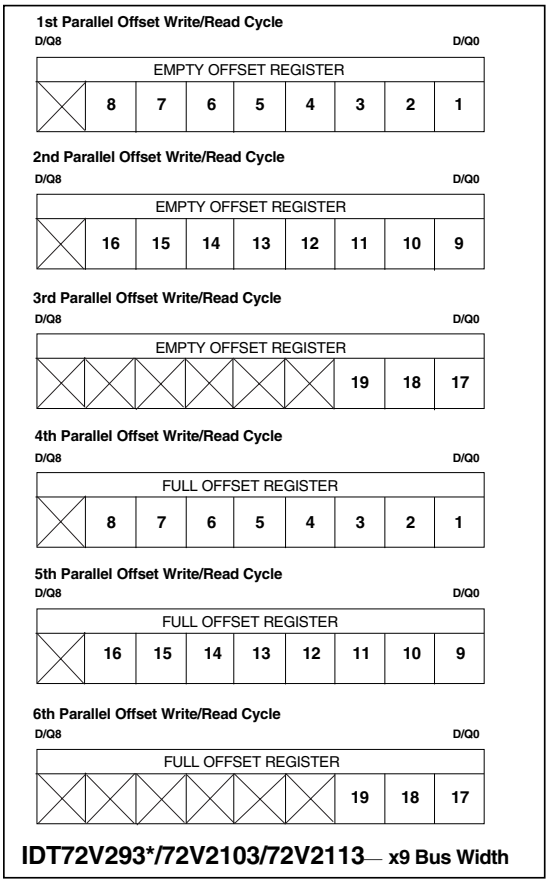


Figure 31. Parallel Offsets with x9 Bus Width





5912 drw33

x9 to x9 Mode
of Bits Used:
14 bits for the IDT72V263 15 bits for the IDT72V273 16 bits for the IDT72V283 17 bits for the IDT72V293 18 bits for the IDT72V2103 19 bits for the IDT72V2113 Note: All unused bits of the LSB & MSB are don't care
All Other Modes
of Bits Used:
13 bits for the IDT72V263 14 bits for the IDT72V273 15 bits for the IDT72V283 16 bits for the IDT72V293 17 bits for the IDT72V2103 18 bits for the IDT72V2113
of Bits Used:
10 bits for the IDT72V3640 11 bits for the IDT72V3650 12 bits for the IDT72V3660 13 bits for the IDT72V3670 14 bits for the IDT72V3680 15 bits for the IDT72V3690 16 bits for the IDT72V36100 17 bits for the IDT72V36110 Note: All unused bits of the LSB & MSB are don't care

Figure 31. Parallel Offsets with x9 Bus Width (Continued)

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