SDRAM Architecture, Signals, and Routing

Application Note AN-260

Notes

By Paul Snell

Introduction

IDT offers two integrated processors that incorporate a RISC CPU core, memory controller, PCI bridge, and other generic peripheral modules on a single die. These processors are:

- RC32334, packaged in a 256 pin ball grid array (BGA) package and supporting a maximum system bus frequency of 75MHz.
- RC32332, packaged in a 208 quad flat pack (QFP) package and supporting a maximum system bus frequency of 66MHz.

With the exception of bus frequency, the on-chip SDRAM controller logic on the two RC3233x integrated processors is identical.

This application note provides information on board architecture, signal routing requirements, and system loading requirements that should be followed when designing an SDRAM-based memory subsystem capable of operating at the maximum speeds indicated above.

Architectural Design

IDT recommends that for maximum SDRAM speed all SDRAM control and data signals be directly connected to the RC3233x. All other memory devices should be placed behind buffers. The system clock should be used to drive all of the memory interfaces in the design through a clock driver with adequate drive strength for the signal loading present in the system. The output clock (output_clk) was not designed for driving the SDRAM circuitry. Accordingly, this output clock does not meet the setup and hold criteria required by external SDRAM devices. Use the system clock instead (cpu_masterclk).

IDT can provide information from the 79S334 and 79S332 evaluation boards which are designed to support the maximum system bus frequencies.

The SDRAM board architecture is depicted in Figure 1.

Notes

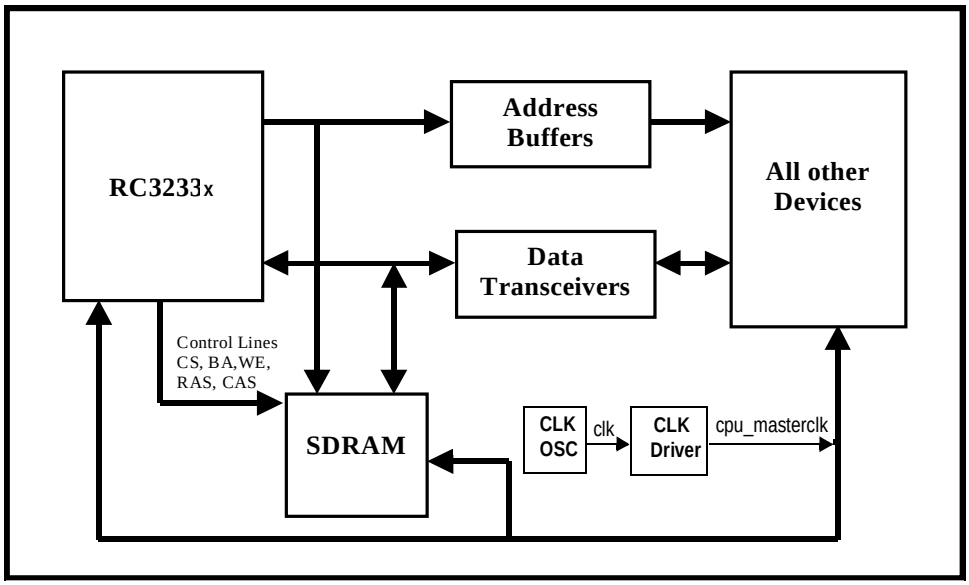

Figure 1 SDRAM Board Architecture

Signal Routing

All signals going to the SDRAM, address, data, and control signals should be kept as short as possible. The trace lengths should also be matched as close as possible.

SDRAM Loading

In order to support maximum speeds, reasonable SDRAM loading constraints must be followed. In particular, IDT recommends that for 75MHz operation no more than four discrete SDRAM chips be used. It is acceptable to use a SODIMM or DIMM, provided it does not contain more than four chips.

For 66MHz operation, no more than eight discrete SDRAM chips should be connected. SODIMMs with up to eight chips may also be used. DIMMs are not recommended, even at this slower speed. However, if DIMMs are used, they should contain a maximum of 8 chips. For example, if two DIMMs are used, each DIMM should contain no more than four chips.

It is possible to use more than eight SDRAM chips or very large DIMMs. However, if the loading exceeds the above recommendation, users should buffer all of the control, address, and data lines accordingly. Because of the extra delay associated with this, higher system speeds are not achievable. To calculate maximum possible system speeds for specific designs, users should review the RC32334 Data Sheet on IDT's RC32334 web page* and the data sheets for the buffers and other devices being used.

* http://www.idt.com/products/pages/Processors-PL100_Sub221_Dev453.html

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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

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