Using The 77V011 and SwitchStar™ in a Small Access Switch

77V011 Application Note AN-257

Obective

This application note covers the software and hardware configuration for an Access Switch using the 77V011 DPI to U2 translation device and the IDT Switchstar switch fabric. Example register values for programming the 77V011 as well as the hardware interfaces with the SwitchStar 77V400 Switching Memory and a 25Mbps PHY will be covered.

SwitchStar conveniently handles 155Mbps streams at the WAN interface of an access switch, but can't handle subporting to multiple 25Mbps ports without a mux/demux device. Headers can be handled downstream, while subport addresses need to be addressed upstream. The 77V011 is between SwitchStar and the lower bandwidth PHYs at the user's location, as shown in Figure 1.

Figure 1 represents a typical SwitchStar based access Switch. The SwitchStar system is based on the 77V500 Switch Controller and the 77V400 Switching Memory. The 77V500 is a call setup manager used for initializing the 77V500. The 77V500 is a state machine that controls VCI and VPI set up within the 77V400. In Figure 1 the 77V400 is configured as an eight port, 155Mbps/port switch fabric. The 77010 is a DPI to UTOPIA 1 translation device that allows Switchstar to communicate with UTOPIA 1 PHYs, such as the 77V156. The 77V012 is also a DPI to UTOPIA 1 translation device, but also provides a header translation feature that allows a full 32 bit ATM header to be converted into the 13 bit header used by SwitchStar. There are other application and tech notes available for both the 77V012 and the 77010. The 77V155, 77V156, and 77105 are 155Mbps and 25Mbps PHYs that

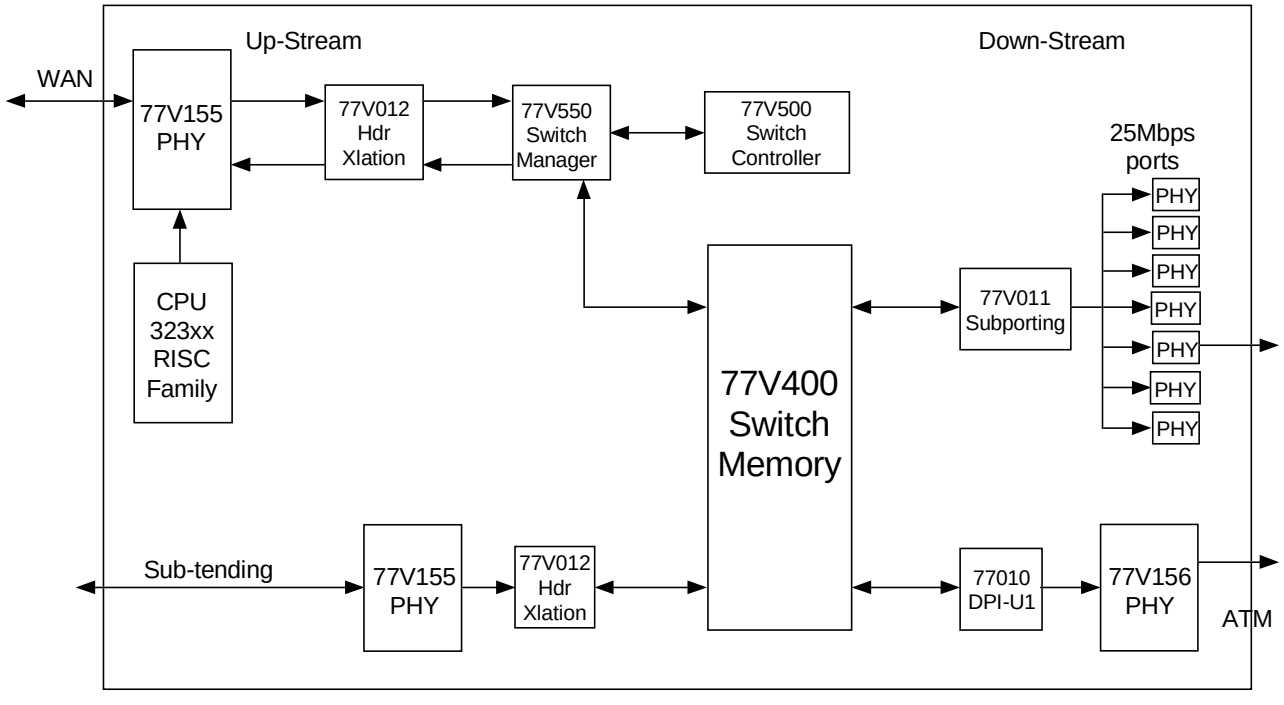

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Figure 1. Access Switch System Example

can also be used in a SwitchStar system. The 77V011 is shown as a subporting solution used to break up one of the 155Mbps streams into eight 25Mbps streams used in an Access Switch and will be the focus of this applicaiton note.

Traffic Flow

Feature 2 provides a closer look at 77V011 and the 25Mbps PHYs used in the example Access Switch presented in Figure 1. Traffic flows across the DPI bus interface to the V400, and across the U2 bus to the PHYs. The 77V011 typically resides on the switch card of the Access Switch, but depending on design requirements it may be placed near the switch as well. The PHYs reside on the linecards and are used to provide external access to the Access Switch.

The 77V011 translates between the DPI and UTOPIA2 formats and sends traffic to the correct subport as programmed by the user. Note the eight 25Mbps ports of figure 2 would exceed the 155Mbps bandwidth of a single 77V400 port if all ports are running simultaneously at full data rate. The UTOPIA 2 bus could be running in either 8 or 16 bit mode, while the DPI bus could be in either 4 or 8 bit mode.

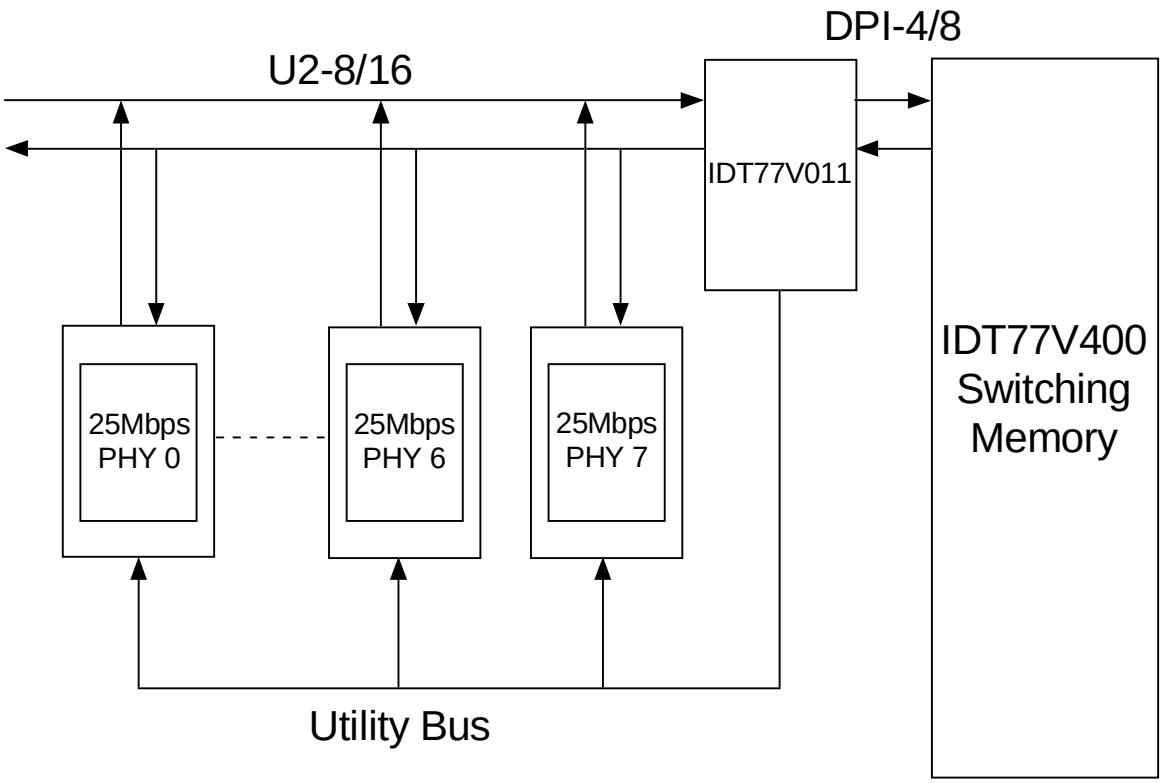

Figure 2. Access Switch Subports

Traffic Flow and Cell Routing

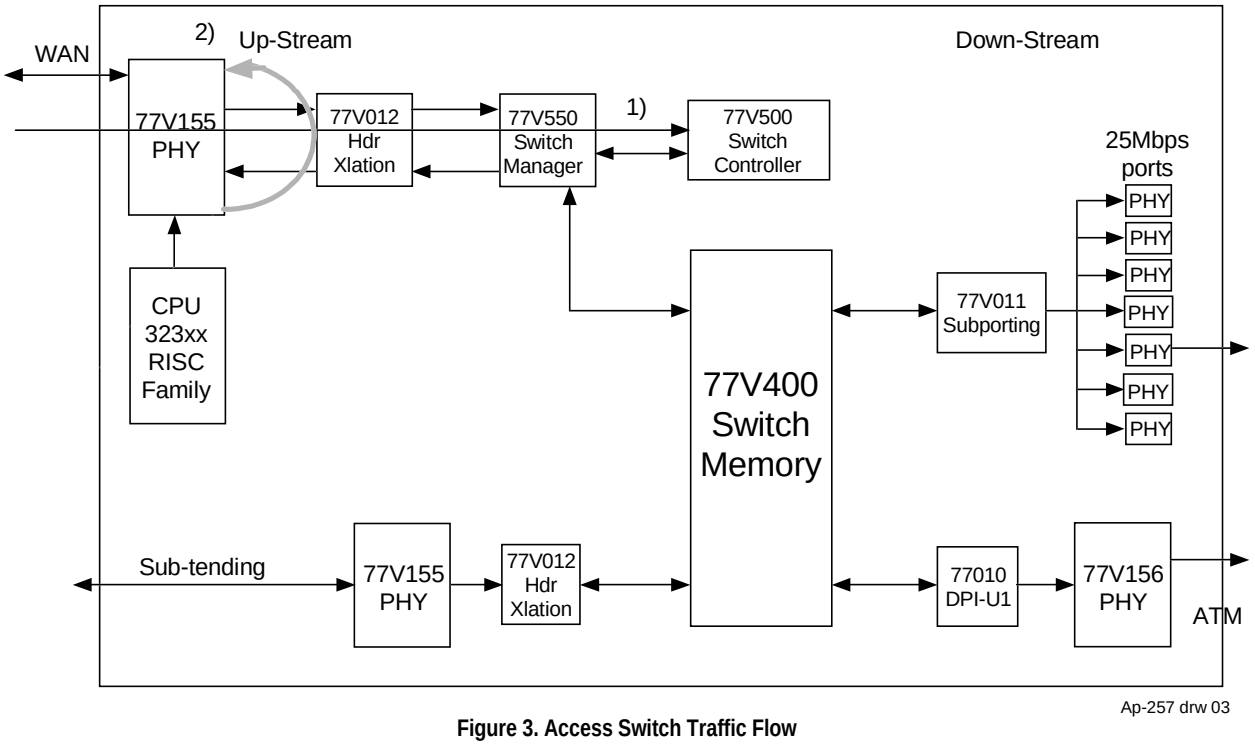

Figure 3. Access Switch Traffic Flow

Path 1 of Figure 3 shows the In-Stream cell path for programming the 77V500 Switch Manager. The 77V500 is used to program the 77V500 Switch Controller. Path 2 shows the traffic path the 77V012 Header Translation device uses to program the 77155 PHY over its Utility Bus.

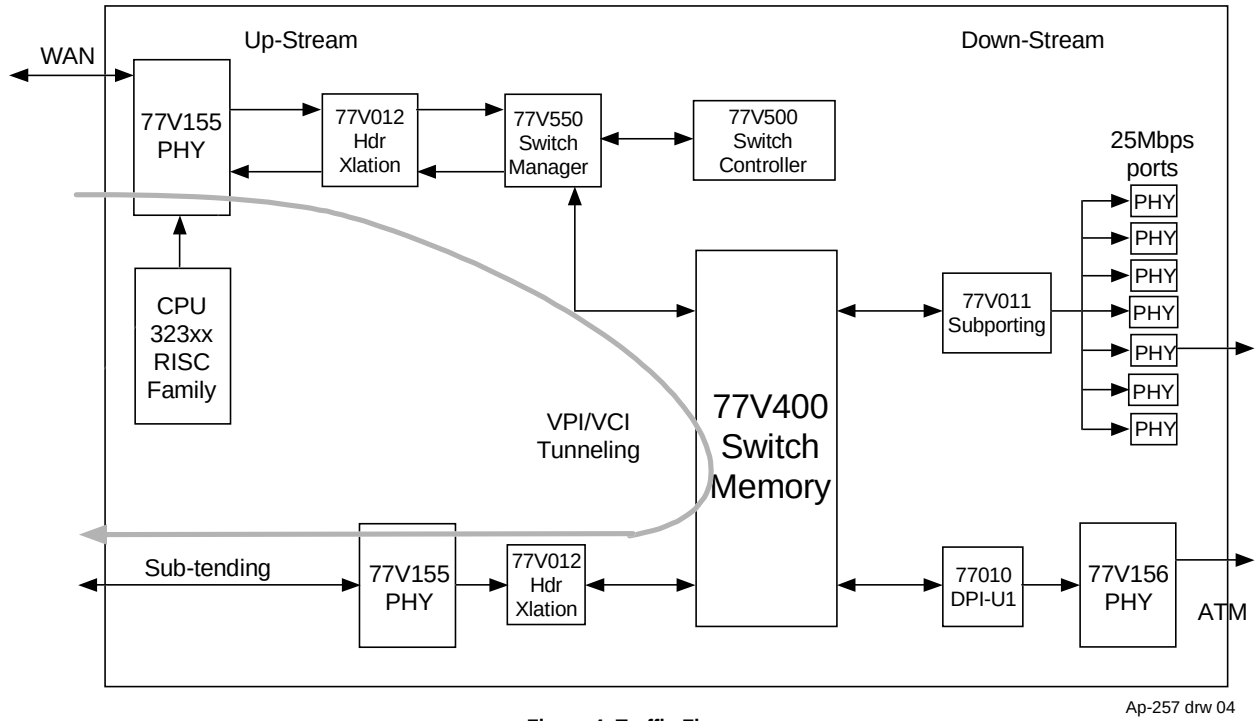

Figure 4. Traffic Flow

Path 1 of Figure 4 Shows the VPI/VCI tunnelling and sub-tending path.

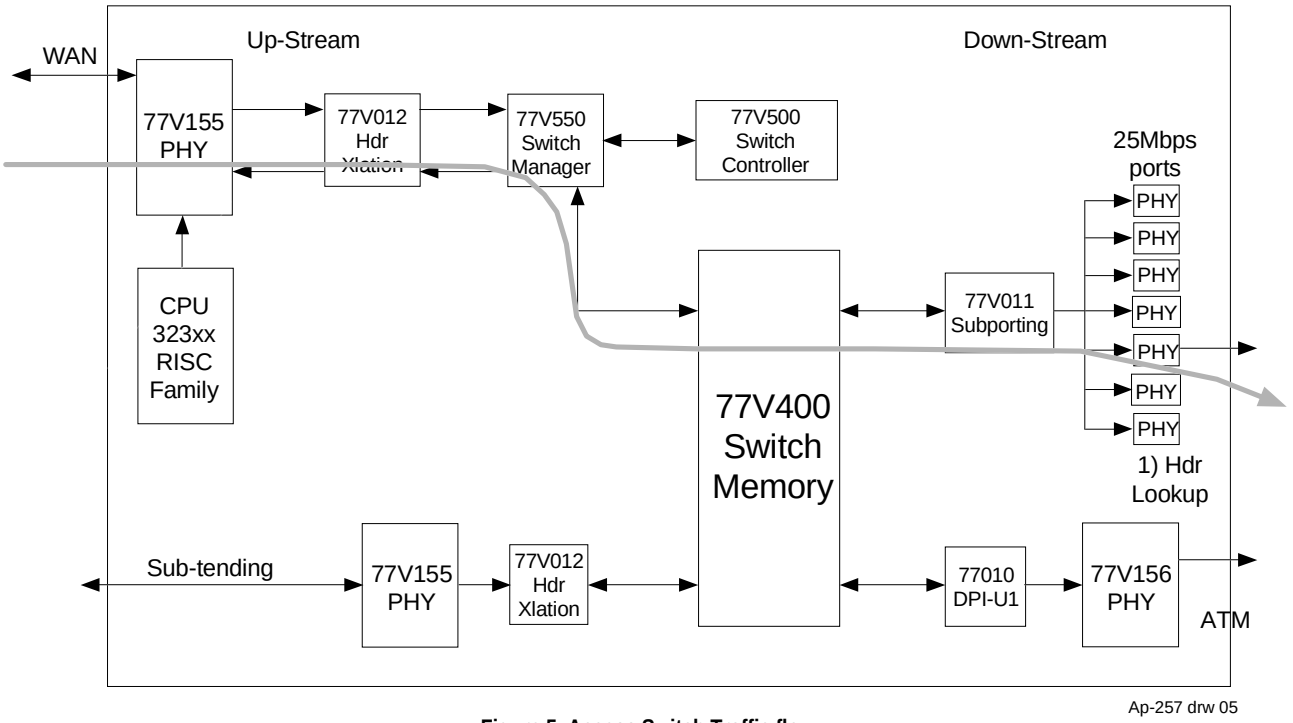

Figure 5. Access Switch Traffic flow

Path 1 of Figure shows a header lookup that uses the 77V011's subporting capabilities. An In-Stream cell goes thorugh the 77155 and the 77V012 for programming the 77V550. The same cell then configures the 77V011 for traffic depending on the header lookup requirements.

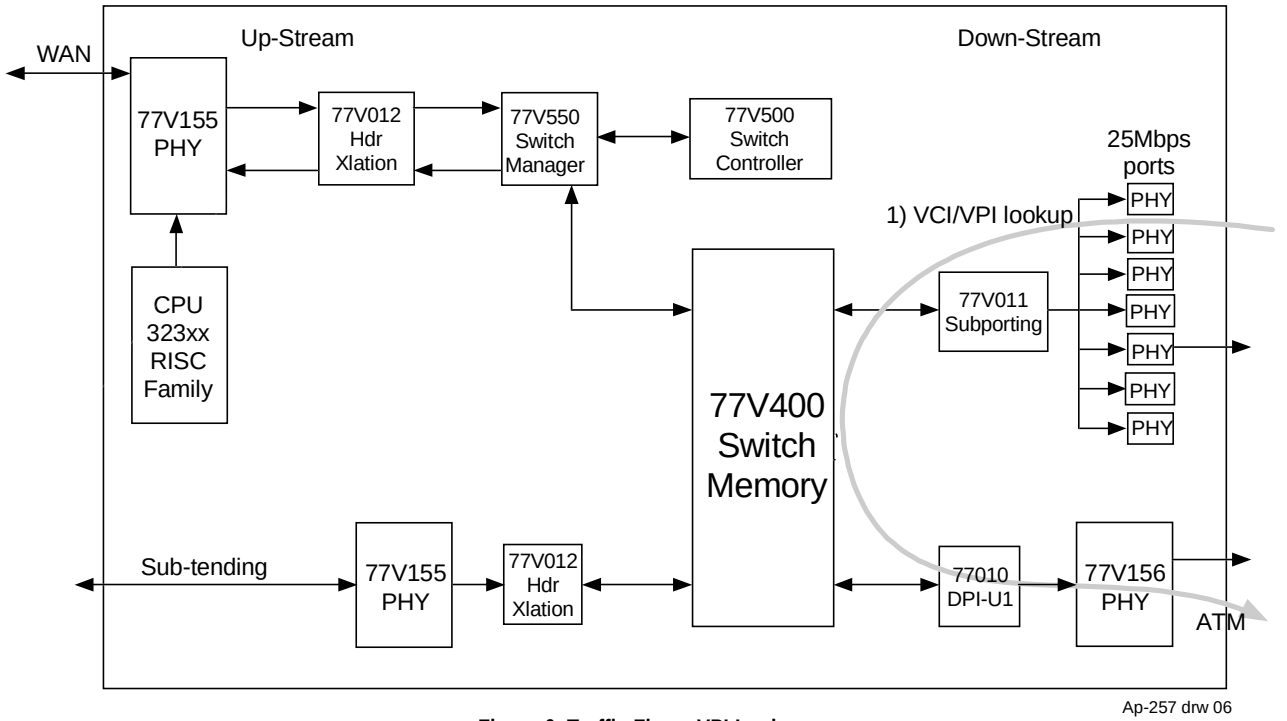

Figure 6. Traffic Flow - VPI Lookup

Figure 6 illustrates an example VPI Lookup with traffic flowing through the 25Mbps PHYs and into the 77V400. It then flows through the 77010 DPI to U1 translation device and out the 77156 PHY.

Path 1 of Figure 7 shows a lookup on both the VPI and VCI with traffic flowing through one 25Mbps PHY and out the 77V400 through another 25Mbps PHY.

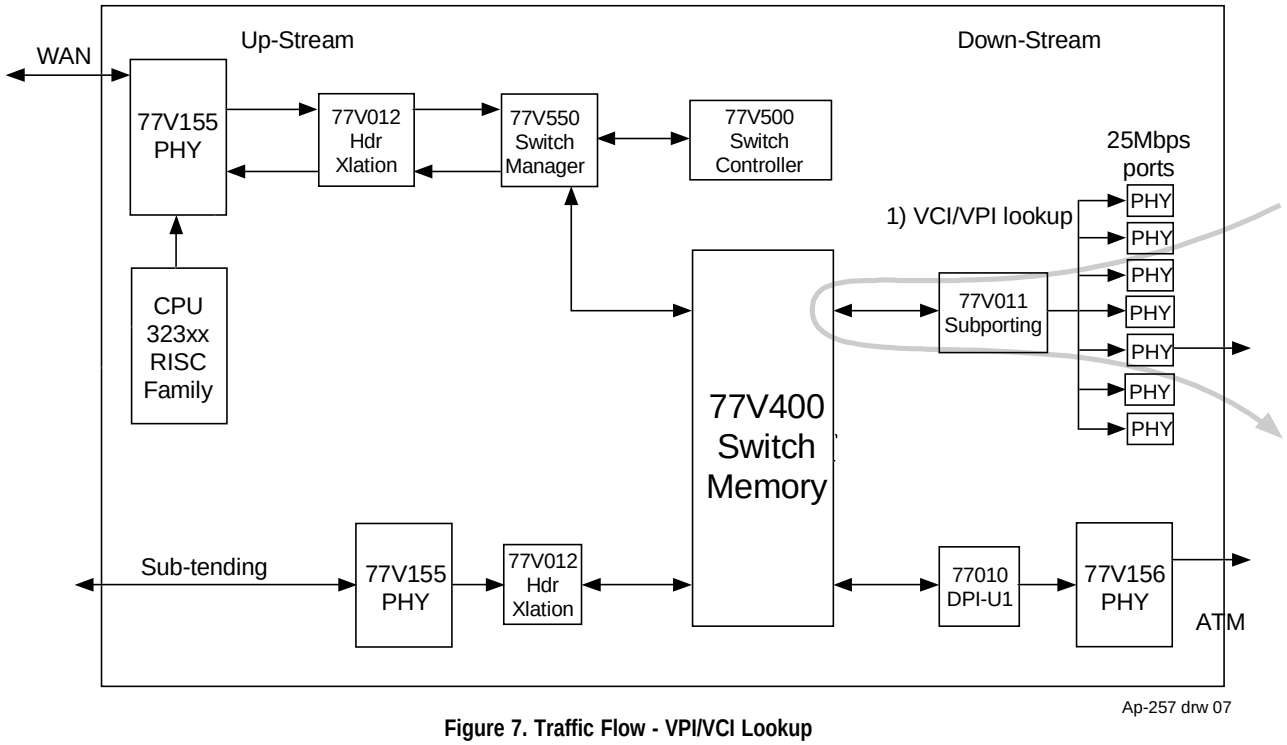

Figure 7. Traffic Flow - VPI/VCI Lookup

77V011 Functional Description

The following section briefly describes the features of the 77V011, for greater detail consult the 77V011 datasheet. The 77V011 is a DPI to UTOPIA 2 translation device used with SwitchStar and supporting physical layer devices. Features include support for UTOPIA 2 eight and sixteen bit data formats, as well as the four or eight bit DPI interfaces. The DPI interface supports cell sizes from 52 to 56 bytes. Up to 31 PHYs can be accessed using the UTOPIA 2 interface. This allows for subporting of a 155Mbps (4 bit DPI) or 310Mbps (8 bit DPI) port of the 77V400 where the bandwidth can be split into multiple lower bandwidth streams.

A TAG routing feature allows up to four bytes to be pre- or post-pended to an ATM cell entering the 77V400, giving additional cell routing flexibility. Cell accounting is provided in both receive and transmit directions. An optional serial EEPROM interface holds initialization information and Discovery/Identify cells. A Management Interface accesses PHYs connected to the 77V011.

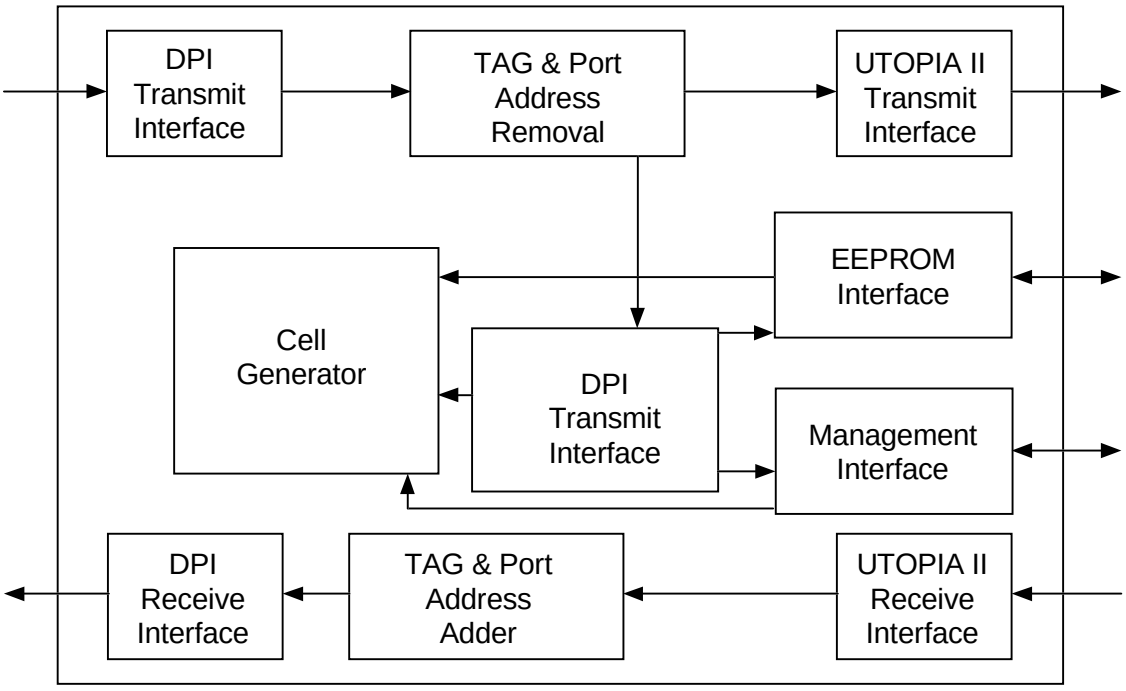

Figure 8. 77V011 Block Diagram

Figure 8 is a high level block diagram showing the logical pieces of the 77V011.

The 77V011 is made up of a number of logical pieces. The DPI Receive Interface transfers cells from the 77V011 to Switchstar or other DPI devices. The DPI Transmit Interface transfers cells from SwitchStar to the 77V011. In-Stream cells are received over the DPI Transmit interface. In both cases four and eight bit data buses are supported.

The UTOPIA 2 Receive interface is a master interface used to transfer cells from a UTOPIA 2 PHY to the 77V011. The UTOPIA 2 Transmit interface is used to transfer cells from the 77V011 to a UTOPIA 2 PHY. In both cases eight and sixteen bit data buses are supported.

The Management interface is used to read and write to PHY registers during normal operation and configure the pin configurable registers during reset. This interface provides support for both the UTOPIA 2 Parallel Interface and the Utility Bus used by many PHYs for register configuration. This application note will only focus on the Utility Bus for PHY configuraiton.

The EEPROM interface provides access to an optional external EEPROM. This EEPROM loads a unique header for each 77V011 at power-up in systems with multiple 77V011s. This provides each 77V011 with its own In-Stream headers for sending configuration commands without having to program each device individually at power-up.

The TAG and Port Address Adder block adds up to a four byte TAG to an ATM cell as it goes through the 77V011. The TAG and Port Address Removal block removes the appropriate field from an ATM cell as it goes through the 77V011.

The Cell Receiver and Cell Generator blocks work with the In-Stream cells to configure the 77V011 for various tasks. In general the Cell Receiver block interprets In-Stream cells and routes commands to the appropriate logic block, while the Cell Generator generates reply In-Stream cells back to the host device. As cells come in through the TxDPI side In-Stream cells are routed to the Cell Receiver block, while data cells exit through the UTOPIA 2 side. The Cell Receiver block then performs the tasks that the In-Stream cell requested, such as driving the Management Interface,

accessing the EEPROM, or accessing the various registers. The Management Interface controls the PHYs, which reply back to the Cell Generator, which generates a cell back to the RxDPI bus.

In-Stream Programming

The 77V011 supports In-Stream (In-band) programming of the configuration registers and management interface, and the registers of the corresponding PHYs. This mechanism allows for all programming commands to be encapsulated within certain ATM cells that are recognized by the 77V011 as configuration commands, therefore simplifying the nessary controlling logic interface. Cells are received on the DPI Transmit interface, identified and sent to the internal cell interpreter for decoding and execution. All In-Stream cells are transmitted round-robin, thus giving each subport and the cell generator equal priority. In order to filter In-stream cells from regular ATM cells a unique cell header is assigned, with a default value of 0x000001F. The 77V011 supports the following set of In-Stream functions: Discover/Identify, Reset, Register Read, Register Write, Event Notification, and Reply Notification. The In-Stream protocol uses the concept of a virtual register. This can be directly mapped to memory, control and command registers. The address map of the register is given in the 77V011 datasheet. The address range of the V011 registers range from 0x008000 to 0x008025. An In-Stream programming cells' format is as shown in table 1.

ATM Header, Bytes 1-5	Transaction ID, Bytes 6-7	Message Type, Byte 8	Device ID, Bytes 9-15	Message Data and/or Padding, Bytes 16-51	Trailer Bytes 52-53

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Table 1. In-Stream Cell Format

Table 2 shows example values for each byte of an In-stream cell used for a register read operation.

In-Stream Header	0x00 00 01 F0	Bytes 1-4
HEC	0xXX (Calculated by PHY)	Byte 5 (Processed by PHY layer)
Transaction ID	0x00 01	Bytes 6-7, User Defined
Message Type	0x45 (01000101)	Byte 8, Bit 6 = 1: Acknowledge Requested, Bit 5 = 0: Command Cell, Bits 4-0 = 00101: Read Register
Device ID	0x01 00 00 00 00 00 00 00	Bytes 9-15, Byte 9: Device ID for 011 and 012 is 0x01, Bytes 10-15 are not used
Message Data: Valid Bytes	0x01	Byte 16, Number of valid bytes to be read or written to
Base Address	0x00 80 00	Bytes 17-19, Base Register Address, this value is incremented once this register is read
Data/Padding	0x00 ..... 0x00	Bytes 19-15, set to zero for padding because read operation is being performed
Trailer	To be calculated by 77V011	

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Table 2. In-Stream Cell with example values provided

For a detailed description of these commands see the 77V011 data sheet. An In-Stream cell can be used to configure the registers of the 77V011 as shown in Appendix A. The following section describes the register definitions used in the example.

Register Description

Example register values (presented in Appendix A) are used for programming the 77V011 for eight subports. A four byte TAG is added to the beginning of the cell and then removed from the outgoing cell to take full advantage of the TAG routing capabilities of the 77V011. The HEC byte is added in the transmit direction and removed in the receive direction. The DPI interface uses a 4-bit data bus, while the UTOPIA2 interface uses an 8 bit data bus.

In the example the Stall Tx pipeline is not stalled (set to 0x00) if the PHY transmit FIFO is full, the cells are just dropped. A related field, the Stall Tx Cycles is also set to 0x00, since the Stall Tx is 0x00.

The DPI mode field selects "switch mode" because the 77V011 will be used with SwitchStar. In this example the Utility Bus is used to configure the PHYs, therefore the UTOPIA2 management mode is set to 0. An alternative to the Utility Bus is the UTOPIA2 Parallel Management Bus, however this example uses the Utility Bus.

The example takes advantage of the external EEPROM to write from the EEPROM to both the In-Stream Cell header and In-Stream subport registers at reset, therefore this bit is set to a "1".

During normal operation the PHY Reset is not asserted, therefore it's set to a "0". It is used to reset the PHY during normal operation. Initially all address and counter registers are zero, as no cells have been transmitted or received.

The In-Stream subport address defaults to an address of 0x00, while the Tx Subport width defaults to 0x5. Both values are acceptable for this example does not replace the subport address in outgoing cells.

The Pin Controls register, 801A, sets Override Pin Configuration to a "1", giving read/write control to the pin configuration registers. The Control A and B registers are set to a "1" to drive external LEDs as an example application of these signals. The Control registers could be used differently if a user chose to do so. The EEPROM registers are configured to select the EEPROM registers wherever necessary.

The UTOPIA Rx and Tx counters are shown with a default value of 0x00 because no cells are running through the 77V011 yet.

The Rx Subport width is set to 0x3 because three bits are needed to decode 8 subports, while the Rx Bit location is maintained at its default value of 0x5 because this is acceptable for this example.

Hardware Examples

RESET OPERATION

When the 77V011 powers up at reset certain signals must be configured with pull-up or pull-down resistors. This insures the 77V011 will power up in a desired manner. The signals of importance are the MBUS(11:0), which configures the TAG and sets the DPI and UTOPIA bus widths, as well as the HEC byte. The MGMT(3:2) controls the particular management mode, whether it is UTOPIA2 parallel management mode, or the Utility Bus. It also controls the DPI mode used, whether it is in Switch mode or Normal mode. The TxADDR(3:0) configures the subport byte location and access to the EEPROM. These signals can also be re-programmed after reset in the register table as shown in the Register Values section if the 77V011 configuration needs to be changed after power up. The configuration used below duplicates the values programmed into the registers in the example register section. Be sure to use a series resistor for both the pull-up and pull-down configurations.

	Pin Name	Definition
GND	MBUS0	Tx TAG Size
GND	MBUS1	Tx TAG Size
V_{DD}	MBUS2	TxTAG Size
GND	MBUS3	TxTAG Location
V_{DD}	MBUS4	Tx Add HEC
GND	MBUS5	Rx TAG Size
GND	MBUS6	Rx TAG Size
V_{DD}	MBUS7	Rx TAG Size
GND	MBUS8	Rx TAG Location
V_{DD}	MBUS9	Rx HEC - HEC must be removed to add four bytes
GND	MBUS10	DPI Size
GND	MBUS11	UTOPIA 2 Size
GND	MGMT2	MGMT2 - MMODE
GND	MGMT3	DPI Mode
GND	TxADDR0	TxADDR0 - Subport Byte location = 0
GND	TxADDR1	TxADDR1
GND	TxADDR2	TxADDR2
V_{DD}	TxADDR3	Init. from EEPROM

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Table 3. External Pin Configuration

The $\overline{SYSRST}$ pin or an In-Stream cell carrying the Reset command will reset the 77V011 and the PHY devices. $\overline{SYSRST}$ should be asserted low for a minimum of 100ns, while the In-Stream reset command will keep the 77V011 in reset for 35 SYSCLK cycles. The 77V011 will stay in reset for 16 SYSCLK cycles after the deassertion of $\overline{SYSRST}$, or the In-Stream reset command. All outputs are tri-stated starting two SYSCLK cycles after the assertion of $\overline{SYSRST}$ or the In-Stream reset command, and will stay tri-stated 24 SYSCLK cycles after the deassertion of $\overline{SYSRST}$ or the In-Stream command. The $\overline{PHYRST}$ pin will then assert low resetting the PHY devices for eight SYSCLK cycles, after which $\overline{PHYRST}$ will deassert high. In some PHY devices eight cycles are not enough to reset the PHY. If this is the case a pull down resistor should be connected to the $\overline{PHYRST}$ pin, this will allow the $\overline{PHYRST}$ to be asserted as soon as it is tri-stated, which provides additional time for the $\overline{PHYRST}$ to be low.

HARDWARE INTERFACE BETWEEN THE 77V011, SWITCHStAR, AND PHYs

Figure 9 is an expansion of the Access Switch example used earlier in this application note, with an emphasis on the 77V011 as a subporting solution. The 77V011 can address different PHYs as needed, but in this case only eight are used. The example schematic shown in Appendix B provides further detail on how to design a subporting solution using the 77V011, the 77V1254 Quad PHY (four PHYs in one package), and the 77V400.

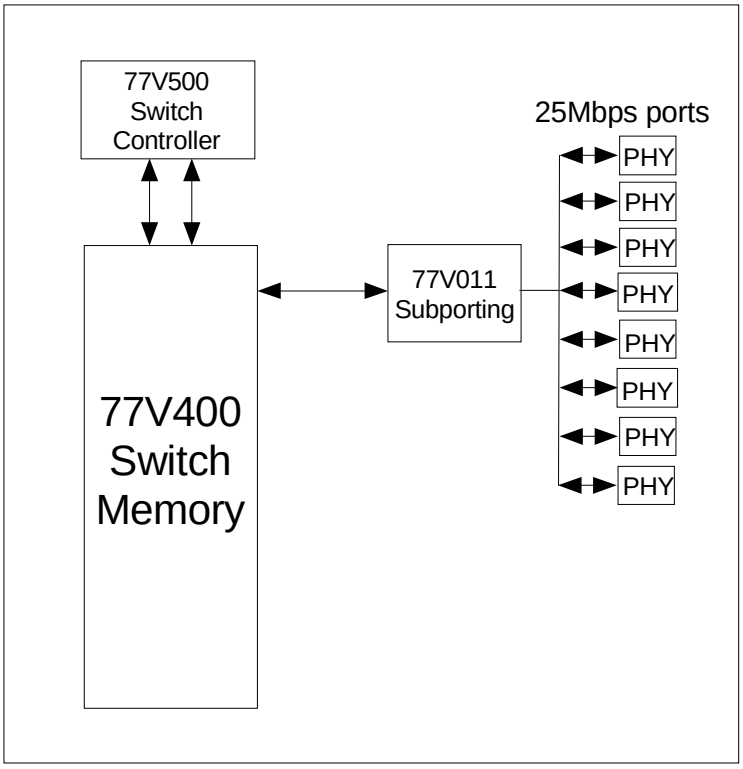

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Figure 9. Subporting with the 77V011

The RxAddr(4-0) and TxAddr(4-0) both interface with the 77V011. This allows the V011 to address up to 31 PHYs. The U2 TxCLK, TxSOC, $\overline{\text{TxENB}}$, RxCLK, $\overline{\text{RxENB}}$ are all signals coming from the 77V011. The U2 RxDATA bus is output from the PHY into the 77V011, while the U2 TxDATA is output from the 77V011 to the PHY. Note that the RxSOC, RxCLAV are both active high outputs from the PHY to the 77V011. Pull down resistors are necessary to prevent the signals from inadvertently floating high at the wrong time. The TxCLAV is output from the PHY to the 77V011. Note that only signals 7-0 are active on the UTOPIA2 data bus. The U2_RxDATA(15-8) are tied low through a 1k resistor because they are inputs, while the U2_TxDATA(15-8) are left floating because they are outputs.

The DATA(7-0) is the Utility Data bus and is used to transfer data between the PHY and the 77V011. Note it can also serve as the U2 Management Data bus, but not in this example. The ADDR(5-0) represents the first six bits of the Management Address Bus. These bits are addressing bits for the Utility bus output from the V011 to the PHY. The additional six bits are used as handshaking signals between the PHY and the 77V011. The $\overline{\text{SEL}}$ signal is a chip select used to validate a read or write on the Utility Bus. The RW/$\overline{\text{WR}}$ is an active low write enable used to control Utility Bus writes. The DS/$\overline{\text{RD}}$ is an active low read enable used to control the Utility Bus reads. The Bus mode pin is used to select between an Intel or Motorola style control interface. The RDY/$\overline{\text{DTACK}}$ signal is output from the PHY to the 77V011 and indicates completion of activity on the Utility bus. The $\overline{\text{INT}}$ is an interrupt from the PHY to the 77V011. This $\overline{\text{INT}}$ must be cleared by the controlling CPU before another interrupt can occur. Both the RDY/$\overline{\text{DTACK}}$ and $\overline{\text{INT}}$ are active low signals, therefore a pull-up resistor is required to prevent them from inadvertently becoming active.

There are additional DPI signals on the 77V011 that interface with the DPI signals on the 77V400. These include the DRxDATA(7-0) bus of the 77V400. The DTxCLK is generated by the 77V011, while the DTxFRM and DTxDATA are output from the 77V400.

When using 8-bit dpi mode two 77V400 ports must be combined to create an 8-bit port. For instance, if ports zero and one are combined to create an 8-bit DPI port, then the I/OFRM0 and I/OCLK0 signals of port zero are used, while the I/OFRM1 and I/OCLK1 signals of port 1 are disabled. The input frame and clock signals are pulled up to Vcc, while the output frame and clock signals are pulled down to GND. The diagram below illustrates this interface.

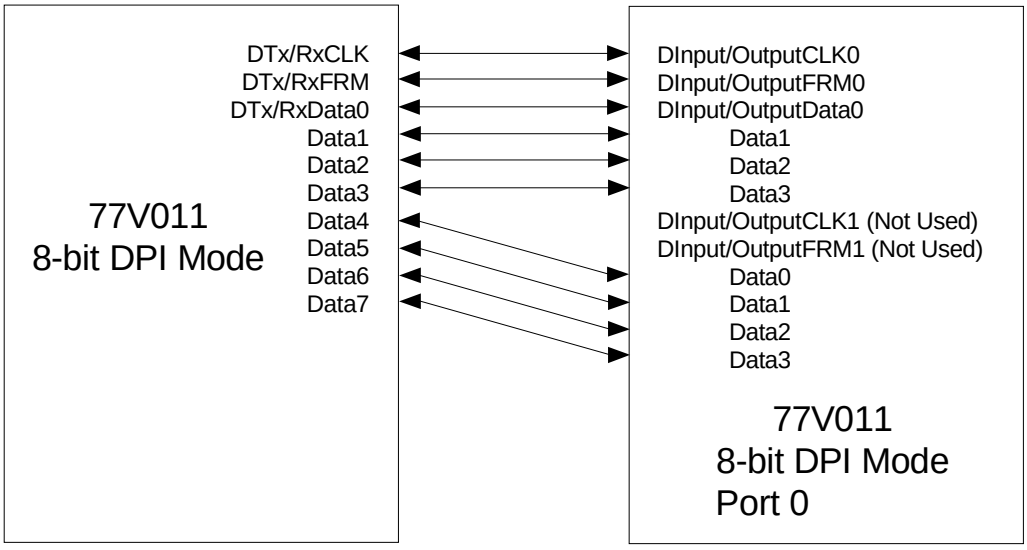

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Figure 10. 8-bit DPI Interface

Other signals of interest are the EEPROM signals, EEDIN, EEDOUT, EECLK, $\overline{\text{EECS}}$, which control access to the external EEPROM.

Conclusion

The 77V011 DPI to U2 translation device provides a subporting solution for use with the 77V500 and 77V400. It expands the capabilities of SwitchStar by providing up to 31 subports from a single 155Mbps port.

The 77V011 provides a translation between the U2 format used by many PHYs and the DPI format used by the 77V400, allowing for a simple interface between an external WAN and the SwitchStar Switching fabric. Both 8 and 16 bit U2 interfaces are supported, while 4 and 8 bit DPI interfaces are supported.

Additional routing flexibility is provided with TAG routing which gives the 77V011 the ability to add or remove up to 4 bytes from an ATM cell.

There is support for cell sizes from 52 to 56 bytes on the DPI interface.

A user controlled option provides the capability to use either the Utility Bus or the Parallel Manager management interface for configuring and reading status of PHY registers.

In-Stream programming allows for simplified control of the 77V011 by sending commands via special ATM cells designated for commands.

Counters provide cell accounting in both the receive and transmit directions.

Appendix A

EXAMPLE REGISTER VALUES

The following are example values for programming the 25 registers of the 77V011 for eight subports (See the 77V011 data sheet for detailed descriptions of each register):

REGISTER NAME	ADDRESS	BIT LOCATION	BIT NAME	VALUE	DESCRIPTION
Device ID	8000	(7:0)	Device Version Number	0x10	Default Value
Config. 1	8001	0	Drop Tx Cell	1	Drop cells with invalid subport addresses
		1	Copy EFCI	1	OR the EFCI bit to the 4 byte TAG area
		2	Rx Move PT/CLP	1	Move the PT/CLP to the 4 byte TAG area
		3	Tx Move PT/CLP	1	Move the PT/CLP to the 4 byte TAG area
		(7:4)	Not Used		
Config. 2	8002	(1:0)	Stall Tx	0x00	Drop the Cells
		(6:2)	Max Subports	0x7	Maximum of 8 subports are used
		7	Not Used		
Config. 3	8003	(7:0)	Stall Tx Cycles	0x00	Drop the Cells
Tx TAG	8004	(2:0)	TxTAG Size	4	Four bytes removed from ATM cell in this example
		3	Tx Add HEC	1	Add HEC placeholder in transmit direction
		4	TxTAG Location	0	Add TAG to beginning of beginning of cell
		(7:5)	Not Used		
Rx TAG	8005	(2:0)	RxTAG Size	4	Four bytes added to ATM cell
		3	Rx Remove HEC	1	Remove HEC byte from cell
		4	RxTAG Location	0	Receive TAG is at beginning of cell
		(7:5)	Not Used		
Mode Select	8006	0	DPI Size	0	4-bit DPI Tx and Rx data bus
		1	DPI Mode	0	Use "Switch mode" (output)
		2	UTOPIA2 Size	0	8-bit UTOPIA2 Tx and Rx data bus
		3	UTOPIA2 Management Mode	0	Use Utility Bus Style
		4	Init from EEPROM	1	Write five byte value from EEPROM to registers at reset
		(7:5)	Not Used		
PHY Reset	8007	0	PHY Reset	0	"0" indicates no Reset
		(7:1)	Not Used		
Notification Mask	8008	0	PHY Int Mask	0	
		1	Rx Address Error	1	Generate Notification cell when a Rx Out of range address error occurs
		(7:2)	Not Used		

Status	8009	0	PHY Interrupt	0	"1" detects PHY Int., "0" means no Int.
		1	Address Range Error	0	"1" indicates Address Range Error has occurred
		2	Tx Cell Dropped	0	"1" indicates a cell was dropped because the PHY did not respond
		(7:3)	Not Used		
Timeout Status	800A	0	PHY Int Status	0	"0" indicates no Interrupt detected
		1	Address Error Status	0	"1" indicates Address Range Error occurred more than 25ms ago and has not been cleared
		(7:2)	Not Used		
Rx Out of Range	800B	(4:0)	Rx Out of Range Subport	0x00	Outputs subport address of cell containing an invalid Cell header
		(7:5)	Not Used		
Rx Out of Range Address Mask Byte 2	800C	(7:0)	Address Mask Register (23:16)	0x00	Used to Validate cells on Rx UTOPIA I/F
Rx Out of Range Address Mask Byte 1	800D	(7:0)	Address Mask Register (15:8)	0x00	Used to Validate cells on Rx UTOPIA I/F
Rx Out of Range Address Mask Byte 0	800E	(7:0)	Address Mask Register (7:0)	0x00	Used to Validate cells on Rx UTOPIA I/F
In-Stream Cell Header Byte 3	800F	(7:0)	In-Stream Header (31:24)	0x00	In-Stream Cell Header
In-Stream Cell Header Byte 2	8010	(7:0)	In-Stream Header (23:16)	0x00	In-Stream Cell Header
In-Stream Cell Header Byte 1	8011	(7:0)	In-Stream Header (15:8)	0x01	In-Stream Cell Header
In-Stream Cell Header Byte 0	8012	(7:0)	In-Stream Header (7:0)	0xF2	In-Stream Cell Header
Subport Config. 1	8013	(4:0)	In-Stream Subport	0x00	Subport address used to filter In-Stream cells
		(7:5)	Tx Subport Width	0x3	3 bits needed for eight subports
Modify Tx Subport	8014	(4:0)	New Subport	0x00	Do not replace subport address in outgoing cells
		5	Replace Subport	0	Do not replace subport address in transmit cells
		(7:6)	Not Used		
Tx Subport Position	8015	(2:0)	Tx Byte Location	0x0	
		(5:3)	Tx Bit Location	0x5	
		(7:6)	Not Used		

TAG Byte 3	8016	(7:0)	TAG(31:24)	0x00	TAG added to cell
TAG Byte 2	8017	(7:0)	TAG(23:16)	0x00	TAG added to cell
TAG Byte 1	8018	(7:0)	TAG(15:8)	0x01	TAG added to cell
TAG Byte 0	8019	(7:0)	TAG(7:0)	0xF2	TAG added to cell
Pin Controls	801A	0	Override Pin Configuration	1	Pin configurable registers are read/writeable
		1	Control A	1	CNTRL_A = "1" - use to drive an LED
		2	Control B	1	CNTRL_B = "1" - use to drive an LED
		3	EEPROM mux select	1	EEPROM will be connected to EEPROM registers
		4	EEPROM clock out	0	
		5	EEPROM chip select	0	EEPROM interface is selected
		6	EEPROM Out	0	
		7	EEPROM In	0	
UTOPIA Rx Cell Counter Byte 3	801B	(7:0)	Rx Cell Counter (31:24)	0x00	Counter for cells transferred on the receive UTOPIA2 bus
UTOPIA Rx Cell Counter Byte 2	801C	(7:0)	Rx Cell Counter (23:16)	0x00	Counter for cells transferred on the receive UTOPIA 2 bus
UTOPIA Rx Cell Counter Byte 1	801D	(7:0)	Rx Cell Counter (15:8)	0x00	Counter for cells transferred on the receive UTOPIA2 bus
UTOPIA Rx Cell Counter Byte 0	801E	(7:0)	Rx Cell Counter (7:0)	0x00	Counter for cells transferred on the receive UTOPIA2 bus
UTOPIA Tx Cell Counter Byte 3	801F	(7:0)	Tx Cell Counter (7:0)	0x00	Counter for cells transferred on the transmit UTOPIA2 bus
UTOPIA Tx Cell Counter Byte 2	8020	(7:0)	Tx Cell Counter (7:0)	0x00	Counter for cells transferred on the transmit UTOPIA2 bus
UTOPIA Tx Cell Counter Byte 1	8021	(7:0)	Tx Cell Counter (7:0)	0x00	Counter for cells transferred on the transmit UTOPIA2 bus
UTOPIA Tx Cell Counter Byte 0	8022	(7:0)	Tx Cell Counter (7:0)	0x00	Counter for cells transferred on the transmit UTOPIA 2 bus
Subport Config. 2	8023	(2:0)	Rx Subport Width	0x3	Eight bits will be used for subport Addressing in the receive direction
		(7:3)	Not Used		
Rx Subport Position	8024	(2:0)	Rx Byte Location	0x2	Indicates what byte of the receive cell header the subport starts in
		(5:3)	Rx Bit Location	0x5	Indicates what bit of the byte defined by Rx Subport Position register the MSB Starts in
		(7:6)	Not Used		

Appendix B

SOFTWARE EXAMPLES USING SWBIOS

The 77950 is an ATM demonstration board for the IDT SwitchStar chipset. It is an eight port, 155Mbps/port switch using the 77V400 Switching memory, the 77V500 switch controller, and the 77V550 Switch manager. There are 8 slots available for line cards. The 77956 is a line card designed to demonstrate the capabilities of the 77V011 subporting device.

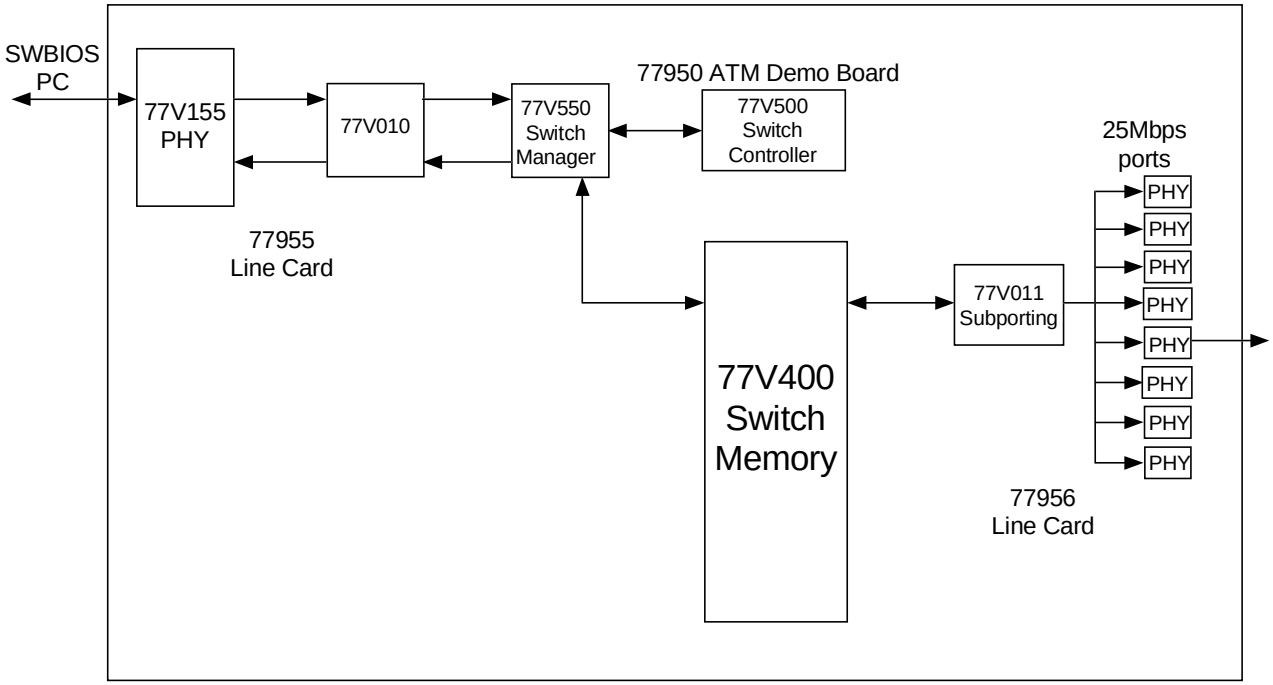

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Figure 11.77950 ATM Demo Board and the 77956 Line Card

Figure 10 shows two line cards, the 77950 and 77956, along with the 77V500 and 77V400. The 77950 board is designed for use with a PC running SWBIOS. The SWBIOS software allows user access to the 77V500, the 77V011, and its PHYs. A simple scripting language and GUI interface are used to send command information in via the 77955 line card to program the 77V500, and the 77V011 on its line card.

The following are programming examples using the 77956 linecard (8 Port 25 Mbps/port 77V011 card) designed for use with the 77950 demo board. There are five basic command procedures available from the pull-down menus supported by SWBIOS for use with the 77956 linecard. These commands are listed in the SWBIOS User's Guide. These are: Reset 77V011, Reset PHY, Configuration and Status, Utility Bus Access, EEPROM Access. The Reset 77V011, and Reset PHY are self-explanatory. The 77V011 Configuration and Status command allows the user to access the various internal registers of the 77V011. "Writing" into the registers causes them to be reconfigured while "Reading" causes them to output current values. The Utility Bus command allows access to the internal registers of the PHY connected to the 77V011. When using In-stream programming the Utility Bus is automatically configured by the 77V011. The EEPROM Access command allows the user to write or read the external optional EEPROM.

In addition to commands available via pull-down menus within SWBIOS, there are also written scripting commands. For the 77V011 there are three relevant commands, Sdpdbg—set the SDP verbose, sdptx—send an in-stream command to the line card, and sdprx—process a SDP cell received from a line card. The following details the arguments of the SDP commands, see the SWBIOS User Guide for more details:

Before sending sdptx and sdprx commands it is necessary to initialize

the 77V500 using the following commands, see the SWBIOS User Guide for details on the individual commands and their parameters:

```
Init 0 0 7 0 0 0 0 1 0 0 0 0 0 0 0 3 2 0
Ldcfg 0 0 0 4 0 0 4 0 1
Parm 0 0 0 0
Sel 0
start
```

The following example shows the arguments for the sdptx command which can be used to write and read to and from the registers in the 77V011:

```
// sdptx vpi vci trans_id ackreq msg_id cnt reg_addr    data....

//Read data from registers from 0x00801E to 0x008021
        sdptx 0 0x70 0x1 1 5 0x04 0x00 0x80 0x1E
        sdptx 0 0x70 0x1 1 5 0x04 0x00 0x80 0x1E
```

The above example reads data from the 77V011 counter registers.

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