Renesas RA Family

24-Bit Sigma-Delta A/D Converter Performance for RA2A1

Introduction
This application note describes the performance and calibration functions of the 24-bit sigma-delta A/D converter integrated into RA2A1.

Target Device
RA2A1 MCU Group

Conditions
Unless otherwise specified, typical data are based on VCC = AVCC0 = AVCC1 = 3.3 V, VSS = AVSS0 = AVSS1 = 0 V, Ta = 25 °C

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1. Overview

A 24-bit sigma-delta A/D converter with a programmable gain instrumentation amplifier is built into the RA2A1 MCU Group. The input mode can be selected as differential input mode or single-ended input mode for each channel. Signals from the input multiplexers pass through the programmable gain instrumentation amplifier (PGA) and enter the sigma-delta A/D converter. The A/D conversion results are filtered through the SINC3 digital filter and stored in an output register.

The 24-bit Sigma-Delta A/D Converter has a calibration function. Calibration allows high-precision A/D conversion by calculating the offset error correction value and gain error correction value under the conditions of use. Calibration must be performed when using the differential input mode of the 24-bit sigma-delta A/D converter for the first time after reset.

This application note explains the 24-bit sigma-delta A/D converter analog input and timing parameters, SNR and SINAD characteristics, AD conversion current consumption, and how to perform calibration.

![Figure 1. SDADC24 Block Diagram](image)

Table 1. SDADC24 I/O Pins

<table>
<thead>
<tr>
<th>Pin name</th>
<th>I/O</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>AVCC1</td>
<td>Input</td>
<td>Analog block power supply pin</td>
</tr>
<tr>
<td>AVSS1</td>
<td>Input</td>
<td>Analog block power supply ground pin</td>
</tr>
<tr>
<td>ADREG</td>
<td>I/O</td>
<td>Power supply pins for PGA and the sigma-delta A/D converter</td>
</tr>
<tr>
<td>SBIAS/VREFI</td>
<td>Input</td>
<td>External reference voltage input pin (VREFI)</td>
</tr>
<tr>
<td></td>
<td>Output</td>
<td>Sensor Power supply pin (SBIAS)</td>
</tr>
<tr>
<td>ANSDP to ANSD3P,</td>
<td>Input</td>
<td>Analog input pins</td>
</tr>
<tr>
<td>ANSDON to ANSD3N</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
2. Utilizing Data Sheet Parametric Values

This chapter describes the electrical characteristics of the 24-Bit Sigma-Delta A/D Converter.

2.1 Analog Inputs Parameters

This section describes analog inputs. Sections 2.1.1 and 2.1.2 show the ranges of input voltage in differential input mode and single-ended input mode.

2.1.1 Range of Input Voltage in Differential Input Mode

Table 2 shows analog input characteristics in differential input mode.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
<th>Test Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Full-scale range</td>
<td>FSR</td>
<td>-</td>
<td>± 0.8/GTOTAL</td>
<td>-</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Analog input in differential input mode</td>
<td>VID</td>
<td>-0.8/GTOTAL</td>
<td>0.8/GTOTAL</td>
<td>V</td>
<td>VID = ANSDnP, ANSDnN, or AMP00 - AMP10 (n = 0 to 3), dOFR = 0 mV</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Vi</td>
<td>0.2</td>
<td>-</td>
<td>1.8</td>
<td>V</td>
<td>Vi = ANSDnP, ANSDnN, or AMP00, or AMP10 (n = 0 to 3)</td>
</tr>
<tr>
<td>Common mode input voltage range</td>
<td>VCOM</td>
<td>0.2+([VID]×GSET1)/2</td>
<td>1.0</td>
<td>1.8-([VID]×GSET1)/2</td>
<td>V</td>
<td>dOFR = 0 mV</td>
</tr>
<tr>
<td></td>
<td>IIN</td>
<td>-</td>
<td>2</td>
<td>-</td>
<td>nA</td>
<td>V = 1 V</td>
</tr>
<tr>
<td></td>
<td>IINFR</td>
<td>-</td>
<td>1</td>
<td>-</td>
<td>nA</td>
<td>VID = 0 V, VCOM = 1 V</td>
</tr>
<tr>
<td></td>
<td>ZIN</td>
<td>-</td>
<td>500</td>
<td>-</td>
<td>Mohm</td>
<td>VID = 1 V, VCOM = 1 V</td>
</tr>
</tbody>
</table>

In differential input mode, the multiplicity factor of gain (GTOTAL) can be changed from \( \times 1 \) to \( \times 32 \) by a combination of the gain of the previous-stage amplifier (GSET1) and the gain of the next-stage amplifier (GSET2).

In the expressions that follow, \( V_{SIG} \) is the differential voltage amplitude, \( V_{COM} \) is the in-phase input voltage, and \( dOFR \) is the value calculated by converting the output voltage of the D/A converter for offset voltage adjustment into input voltage. The range of input voltage for one amplifier stage is from 0.2 V to 1.8 V. Therefore, signals that pass through the previous-stage amplifier of the instrumentation amplifier and enter to the next-stage amplifier must satisfy the condition indicated by Expression 1.

In addition, signals that pass through the previous-stage amplifier of the instrumentation amplifier and exit from the next stage amplifier must satisfy the condition indicated by Expression 2.

Expression 1:

\[
0.2 \text{ V} + \frac{|V_{SIG}| \times G_{SET1}}{2} \leq V_{COM} \leq 1.8 \text{ V} - \frac{|V_{SIG}| \times G_{SET1}}{2}
\]
Expression 2:
\[-0.8 \text{ V} \leq (V_{\text{SIG}} + d_{\text{OFR}}) \times G_{\text{TOTAL}} \leq 0.8 \text{ V}\]

When \(d_{\text{OFR}} = 0 \text{ mV}\), the input signal can be equal to the full-scale differential input voltage at full scale. When \(V_{\text{SIG}} = V_{\text{ID}}\) (full-scale differential input voltage), \(V_{\text{COM}}\) can be represented using Expression 3.

Expression 3:
\[0.2 \text{ V} + \frac{|V_{\text{ID}}| \times G_{\text{SET1}}}{2} \leq V_{\text{COM}} \leq 1.8 \text{ V} - \frac{|V_{\text{ID}}| \times G_{\text{SET1}}}{2}\]

Differential input mode

\[
\begin{align*}
\text{V}_{\text{COM}} & \quad \text{V}_{\text{SIG}} \\
\text{1.8 V} & \quad \text{0.2 V} \\
\text{+0.4 V / (G}_{\text{TOTAL}} & \quad -0.4 V / (G}_{\text{TOTAL}} \\
\text{Ex.) G}_{\text{TOTAL}} = G_{\text{SET1}} = \times 1, d_{\text{OFR}} = 0 \text{ mV} \\
\text{V}_{\text{COM}} & \quad \text{V}_{\text{SIG}} \\
\text{1.8 V} & \quad \text{1.4 V} \\
\text{+0.2 V} & \quad -0.2 V \\
\text{Ex.) G}_{\text{TOTAL}} = G_{\text{SET1}} = \times 2, d_{\text{OFR}} = 0 \text{ mV}
\end{align*}
\]

Figure 2. Range of Input Voltage in Differential Input Mode
Figure 3 shows the transition of the amplitude of differential input voltage for each channel of the programmable gain instrumentation amplifier (PGA).

![Diagram showing the transition of differential input voltage for each channel of the PGA](image)

**Figure 3. Transition of Differential Input Voltage for Each Channel of the PGA**

### 2.1.2 Range of Input Voltage in Single-ended Input Mode

Table 3 shows the analog input characteristics in single-ended input mode.

**Table 3. Analog Input Characteristics in Single-ended Input Mode**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
<th>Test Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Analog Input in single-ended input mode</td>
<td>$V_i$</td>
<td>0.2</td>
<td>-</td>
<td>1.8</td>
<td>V</td>
<td>$V_i = \text{ANSDnP, ANSDnN, AMP0O or AMP1O (n = 0 to 3), }$ $V_{\text{COM}} = 1.0 \text{ V, } d_{\text{OFR}} = 0 \text{ mV, } G_{\text{SET1}} = 1, G_{\text{SET2}} = 1, \text{ and } OSR = 256$</td>
</tr>
<tr>
<td>Input absolute current</td>
<td>$I_i$</td>
<td>-</td>
<td>2</td>
<td>-</td>
<td>nA</td>
<td>$V_i = 1 \text{ V}$</td>
</tr>
</tbody>
</table>

The single-ended input mode supports only $d_{\text{OFR}} = 0 \text{ mV, } G_{\text{SET1}} = 1, G_{\text{SET2}} = 1$, and Oversampling Ratio (OSR) = 256.

In positive-side single-ended input mode, the signal from the input multiplexer is connected to the non-inverting input of the PGA. The bias voltage ($V_{\text{BIAS}} = 1.0 \text{ V (typical)}$) is connected to the inverting input of the PGA to provide a reference voltage. In negative-side single-ended input mode, the signal from the input multiplexer is connected to the inverting input of the PGA, and the internal bias voltage is connected to the non-inverting input of the PGA. The differential signal output is in the range from 0.2 V to 1.8 V.
Range of the input voltage (Vi) must satisfy the following expression:

\[ 0.2 \, \text{V} \leq V_{i} \leq 1.8 \, \text{V} \]

**Figure 4. Range of Input Voltage in Single-ended Input Mode**

### 2.2 Timing Parameters

Table 4 shows the timing parameters of the 24-Bit Sigma-Delta A/D Converter.

**Table 4. Timing Parameters of 24-Bit Sigma-Delta A/D Converter**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
<th>Test Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Over sampling frequency</td>
<td>F_{OS}</td>
<td>-</td>
<td>1</td>
<td>-</td>
<td>MHz</td>
<td>Normal A/D conversion mode</td>
</tr>
<tr>
<td></td>
<td></td>
<td>-</td>
<td>0.125</td>
<td>-</td>
<td></td>
<td>Low-power A/D conversion mode</td>
</tr>
<tr>
<td>Output data rate</td>
<td>f_{DATA1}</td>
<td>0.48828</td>
<td>-</td>
<td>15.625</td>
<td>ksp</td>
<td>Normal A/D conversion mode</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Low-power A/D conversion mode</td>
</tr>
<tr>
<td></td>
<td>f_{DATA2}</td>
<td>61.03615</td>
<td>-</td>
<td>1953.125</td>
<td>sps</td>
<td>Low-power A/D conversion mode</td>
</tr>
</tbody>
</table>

A/D conversion is performed by the SDADC24 reference clock generated by the SDADCKCLK. Set the SDADC24.STC1.CKDIV[3:0] bits so that the SDADC24 reference clock is output at 4 MHz. In normal A/D conversion mode, the oversampling frequency is 1 MHz. In low-power A/D conversion mode, the oversampling frequency is 0.125 MHz.

The oversampling ratio can be selected from 64, 128, 256, 512, 1024, or 2048 by SDADC24.PGACn.PGAOSR[2:0] bits (n = 0 to 4).

The equation for calculating the output data rate is as follows:

\[
\text{Output data rate (sps)} = \frac{\text{Over sampling frequency}}{\text{Oversampling ratio}}
\]

Down sampling of the A/D conversion result is performed by the SINC3 digital filter.

Figure 5 shows a block diagram of the digital filter. Three accumulators and three differentiators are connected in a cascade format. For the A/D converter to become stable, the required settling time must be satisfied. Table 5 shows settling time 1 and settling time 2, which are defined as follows:

- **Settling time 1** — The time from ADC2.SDADST bit rising to A/D conversion end interrupt. See settling time 1 in Figure 6.
- **Settling time 2** — The time from the last A/D conversion end interrupt before channel switching to the first A/D conversion end interrupt after channel switching. See settling time 2 in Figure 6.
from ADC
- Normal A/D conversion mode: Fin = 1 MHz
- Low-power A/D conversion mode: Fin = 0.125 MHz

\[
\begin{align*}
&M = \text{OSR} = 64, 128, 256, 512, 1024, 2048 \\
&\text{Gain adjust} = \text{bit shift} \\
&\text{to register} (f_{out} = f_{in}/M)
\end{align*}
\]

Figure 5. Digital Filter Block Diagram

Table 5. Settling Time for Each Operation Mode

<table>
<thead>
<tr>
<th>Item</th>
<th>Normal A/D Conversion Mode</th>
<th>Low-power A/D Conversion Mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>Setting time 1</td>
<td>Min: 3T + 129 (\mu)s + 2PCLKB + 9 ADC reference clock(^1)</td>
<td>3T + 1032 (\mu)s + 2PCLKB + 9 ADC reference clock(^1)</td>
</tr>
<tr>
<td></td>
<td>Max: 3T + 129 (\mu)s + 3PCLKB + 10 ADC reference clock(^1)</td>
<td>3T + 1032 (\mu)s + 3PCLKB + 10 ADC reference clock(^1)</td>
</tr>
<tr>
<td>Setting time 2(^2)</td>
<td>Min: 3T + 129 (\mu)s - 1PCLKB</td>
<td>3T + 1032 (\mu)s - 1PCLKB</td>
</tr>
<tr>
<td></td>
<td>Max: 3T + 129 (\mu)s + 1PCLKB</td>
<td>3T + 1032 (\mu)s + 1PCLKB</td>
</tr>
</tbody>
</table>

Note: The settling time is automatically generated by the AUTOSCAN built-in sequencer.

3T is the time that is 3 times as long as the sampling time (3 x 1 / fout).

Notes:
1. Normal A/D conversion mode: 4 MHz, low-power A/D conversion mode: 500 kHz.
2. Since the A/D converter and the control circuit are asynchronous, a variation of ± 1PCLKB occurs at the interrupt output timing. There is no variation in the A/D conversion interval, and it is executed at equal intervals.

Figure 6. AUTOSCAN Sequence
2.3 24-Bit Sigma-Delta A/D Converter Characteristics

Table 6 shows SNR, SINAD, and ENOB characteristics evaluation results of the 24-Bit Sigma-Delta A/D Converter.

The SNR and SINAD are very important in many applications because they describe the smallest input signal that the converter can resolve. In closed loop systems, detecting small changes in input signals allows better control loop performance.

SNR: Signa-to-noise ratio (dB)
The RMS signal level to the total RMS noise

SINAD: Signal-to-noise and distortion (dB)
The RMS level of input signal/sum RMS value of all noise and distortion excluding DC

ENOB: Effective number of bits
ENOB = (SINAD – 1.76 dB) / 6.02 dB

ENOB (RMS): Effective Resolution
ENOB (RMS) = log2 (VFullscale / Noise_RMS)
Noise_RMS is input-referred noise at V_ID = 0 V. VFullscale is peak-to-peak value of FSR.

Table 6. SNR, SINAD, and ENOB Evaluation Results of 24-Bit Sigma-Delta A/D Converter

Conditions: VCC = AVCC0 = AVCC1 = 3.3 V, VSS = AVSS0 = AVSS1 = 0 V, V_COM = 1.0 V. The electrical specifications are applied at differential input mode, external clock input used, F_OSR = 1 MHz, d_OFR = 0 mV, unless otherwise specified.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Typ</th>
<th>Unit</th>
<th>Test Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Signal to Noise Ratio</td>
<td>SNR</td>
<td>76.0</td>
<td>dB</td>
<td>G_SET1 = 1, G_SET2 = 1, PGACn.PGAAVE[1:0] = 00b or 01b</td>
</tr>
<tr>
<td></td>
<td></td>
<td>85.1</td>
<td></td>
<td>OSR = 64</td>
</tr>
<tr>
<td></td>
<td></td>
<td>89.1</td>
<td></td>
<td>OSR = 128</td>
</tr>
<tr>
<td></td>
<td></td>
<td>92.2</td>
<td></td>
<td>OSR = 256</td>
</tr>
<tr>
<td></td>
<td></td>
<td>95.2</td>
<td></td>
<td>OSR = 512</td>
</tr>
<tr>
<td></td>
<td></td>
<td>98.2</td>
<td></td>
<td>OSR = 1024</td>
</tr>
<tr>
<td></td>
<td></td>
<td>73.1</td>
<td>dB</td>
<td>G_SET1 = 8, G_SET2 = 4, PGACn.PGAAVE[1:0] = 00b or 01b</td>
</tr>
<tr>
<td></td>
<td></td>
<td>73.1</td>
<td></td>
<td>OSR = 64</td>
</tr>
<tr>
<td></td>
<td></td>
<td>78.2</td>
<td></td>
<td>OSR = 128</td>
</tr>
<tr>
<td></td>
<td></td>
<td>81.3</td>
<td></td>
<td>OSR = 256</td>
</tr>
<tr>
<td></td>
<td></td>
<td>84.2</td>
<td></td>
<td>OSR = 512</td>
</tr>
<tr>
<td></td>
<td></td>
<td>87.2</td>
<td></td>
<td>OSR = 1024</td>
</tr>
<tr>
<td></td>
<td></td>
<td>89.8</td>
<td></td>
<td>OSR = 2048</td>
</tr>
<tr>
<td>Signal to Noise and Distortion Ratio</td>
<td>SINAD</td>
<td>74.4</td>
<td>dB</td>
<td>G_SET1 = 1, G_SET2 = 1, PGACn.PGAAVE[1:0] = 00b or 01b</td>
</tr>
<tr>
<td></td>
<td></td>
<td>84.1</td>
<td></td>
<td>OSR = 64</td>
</tr>
<tr>
<td></td>
<td></td>
<td>87.8</td>
<td></td>
<td>OSR = 128</td>
</tr>
<tr>
<td></td>
<td></td>
<td>90.1</td>
<td></td>
<td>OSR = 256</td>
</tr>
<tr>
<td></td>
<td></td>
<td>91.7</td>
<td></td>
<td>OSR = 512</td>
</tr>
<tr>
<td></td>
<td></td>
<td>93.0</td>
<td></td>
<td>OSR = 1024</td>
</tr>
<tr>
<td></td>
<td></td>
<td>72.2</td>
<td>dB</td>
<td>G_SET1 = 8, G_SET2 = 4, PGACn.PGAAVE[1:0] = 00b or 01b</td>
</tr>
<tr>
<td></td>
<td></td>
<td>72.2</td>
<td></td>
<td>OSR = 64</td>
</tr>
<tr>
<td></td>
<td></td>
<td>77.9</td>
<td></td>
<td>OSR = 128</td>
</tr>
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<td></td>
<td></td>
<td>81.0</td>
<td></td>
<td>OSR = 256</td>
</tr>
<tr>
<td></td>
<td></td>
<td>83.7</td>
<td></td>
<td>OSR = 512</td>
</tr>
<tr>
<td></td>
<td></td>
<td>86.1</td>
<td></td>
<td>OSR = 1024</td>
</tr>
<tr>
<td></td>
<td></td>
<td>87.7</td>
<td></td>
<td>OSR = 2048</td>
</tr>
<tr>
<td>Parameter</td>
<td>Symbol</td>
<td>Typ</td>
<td>Unit</td>
<td>Test Conditions</td>
</tr>
<tr>
<td>-------------------------------</td>
<td>--------</td>
<td>-----</td>
<td>------</td>
<td>------------------------------------------------------</td>
</tr>
<tr>
<td>Effective number of bits</td>
<td>ENOB</td>
<td>12.1</td>
<td>bit</td>
<td>$G_{\text{SET1}} = 1$, $G_{\text{SET2}} = 1$,</td>
</tr>
<tr>
<td></td>
<td></td>
<td>13.7</td>
<td></td>
<td>$\text{PGACn.PGAAVE}[1:0] = 00b$ or $01b$,</td>
</tr>
<tr>
<td></td>
<td></td>
<td>14.3</td>
<td></td>
<td>$\text{OSR} = 64$</td>
</tr>
<tr>
<td></td>
<td></td>
<td>14.7</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>14.9</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>15.2</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>11.7</td>
<td>bit</td>
<td>$G_{\text{SET1}} = 8$, $G_{\text{SET2}} = 4$,</td>
</tr>
<tr>
<td></td>
<td></td>
<td>12.6</td>
<td></td>
<td>$\text{PGACn.PGAAVE}[1:0] = 00b$ or $01b$,</td>
</tr>
<tr>
<td></td>
<td></td>
<td>13.2</td>
<td></td>
<td>$\text{OSR} = 64$</td>
</tr>
<tr>
<td></td>
<td></td>
<td>13.6</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>14.0</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>14.3</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>14.3</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Effective Resolution</td>
<td>ENOB</td>
<td>14.1</td>
<td>bit</td>
<td>$G_{\text{SET1}} = 1$, $G_{\text{SET2}} = 1$,</td>
</tr>
<tr>
<td></td>
<td></td>
<td>15.6</td>
<td></td>
<td>$\text{PGACn.PGAAVE}[1:0] = 00b$ or $01b$,</td>
</tr>
<tr>
<td></td>
<td></td>
<td>16.3</td>
<td></td>
<td>$V_{\text{fullscale}} = 1.6$ V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>16.8</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>17.3</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>17.8</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>13.6</td>
<td>bit</td>
<td>$G_{\text{SET1}} = 8$, $G_{\text{SET2}} = 4$,</td>
</tr>
<tr>
<td></td>
<td></td>
<td>14.5</td>
<td></td>
<td>$\text{PGACn.PGAAVE}[1:0] = 00b$ or $01b$,</td>
</tr>
<tr>
<td></td>
<td></td>
<td>15.0</td>
<td></td>
<td>$V_{\text{fullscale}} = 0.05$ V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>15.5</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>16.0</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>16.4</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Figure 7. SNR versus OSR**
Figure 8. SINAD versus OSR

Figure 9. Dependence of SNR on $GSET_1$

Figure 10. Dependence of SNR on $GSET_2$
Figure 11. Dependence of SINAD on GSET1

Figure 12. Dependence of SINAD on GSET2

Figure 13. Power versus Frequency (GSET1 = 1, GSET2 = 1, OSR = 64)
Figure 14. Power versus Frequency (GSET1 = 1, GSET2 = 1, OSR = 256)

Figure 15. Power versus Frequency (GSET1 = 1, GSET2 = 1, OSR = 2048)

Figure 16. Power versus Frequency (GSET1 = 8, GSET2 = 4, OSR = 64)
2.3.1 Improve Accuracy by Averaging A/D Conversion Result

The 24-Bit Sigma-Delta A/D Converter has an averaging function. When averaging is used, multiple conversions are performed and the results are averaged. The output data can be averaged 8, 16, 32, or 64 times. This can suppress the influence of sudden noise and improve the accuracy of the conversion result.

Table 7. Performance Evaluation Result by Averaging A/D Conversion Result

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Typ</th>
<th>Unit</th>
<th>Test Conditions</th>
<th>No averaging</th>
<th>8 times average</th>
<th>16 times average</th>
<th>32 times average</th>
<th>64 times average</th>
</tr>
</thead>
<tbody>
<tr>
<td>Signal to Noise Ratio V_{id} = 0 V</td>
<td>SNR</td>
<td></td>
<td>dB</td>
<td>G_{SET1} = 1, G_{SET2} = 1, OSR = 256</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>89.1</td>
<td></td>
<td></td>
<td>No averaging</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>95.9</td>
<td></td>
<td></td>
<td>8 times average</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>98.8</td>
<td></td>
<td></td>
<td>16 times average</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>101.5</td>
<td></td>
<td></td>
<td>32 times average</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>104.3</td>
<td></td>
<td></td>
<td>64 times average</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SINAD</td>
<td></td>
<td>88.1</td>
<td>dB</td>
<td>G_{SET1} = 1, G_{SET2} = 1, OSR = 256</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>91.8</td>
<td></td>
<td></td>
<td>No averaging</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>8 times average</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Parameter</td>
<td>Symbol</td>
<td>Typ</td>
<td>Unit</td>
<td>Test Conditions</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>-----------</td>
<td>--------</td>
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<td>------</td>
<td>-----------------</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Signal to Noise and Distortion Ratio</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$f_{in} = 10$ Hz</td>
<td></td>
<td>92.9</td>
<td>16 times average</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>94.1</td>
<td>32 times average</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>95.4</td>
<td>64 times average</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Effective number of bits</td>
<td>ENOB</td>
<td>14.3</td>
<td>bit</td>
<td>$G_{SET1} = 1, G_{SET2} = 1,$</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$f_{in} = 10$ Hz</td>
<td></td>
<td></td>
<td></td>
<td>$OSR = 256$</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>15.0</td>
<td>8 times average</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>15.1</td>
<td>16 times average</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>15.3</td>
<td>32 times average</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>15.6</td>
<td>64 times average</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Effective Resolution</td>
<td>ENOB (RMS)</td>
<td>16.3</td>
<td>bit</td>
<td>$G_{SET1} = 1, G_{SET2} = 1,$</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>$OSR = 256,$</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>$V_{fullscale} = 1.6$ V</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>17.4</td>
<td>8 times average</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>17.9</td>
<td>16 times average</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>18.4</td>
<td>32 times average</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>18.8</td>
<td>64 times average</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Figure 19. SNR versus Average Times

Figure 20. SINAD versus Average Times
2.4 Sensor Bias (SBIAS) Characteristics

Table 8 shows SBIAS drift characteristics evaluation results. The average value ± 1σ of the evaluation results is defined as the typical and the average value ± 5σ of the evaluation results is defined as the maximum.

**Table 8. SBIAS Drift Characteristics Evaluation Result**

Conditions: VCC = AVCC0 = AVCC1 = 2.7V to 5.5 V, VSS = AVSS0 = AVSS1 = 0 V, Ta = –40 °C to 105°C, SDADCSTC1.VREFSEL = 0, Connect the SBIAS/VREFI pin to AVSS1 pin by a 0.22 μF (-20% to +20%).

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Typ*1</th>
<th>Max*2</th>
<th>Unit</th>
<th>Test Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>SBIAS drift</td>
<td>ΔE_{SBIAS}</td>
<td>18.7</td>
<td>89.1</td>
<td>ppm/°C</td>
<td>SBIAS = 0.8 V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>16.6</td>
<td>79.0</td>
<td></td>
<td>SBIAS = 1.0 V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>14.8</td>
<td>73.4</td>
<td></td>
<td>SBIAS = 1.2 V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>14.2</td>
<td>69.4</td>
<td></td>
<td>SBIAS = 1.4 V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>13.2</td>
<td>66.6</td>
<td></td>
<td>SBIAS = 1.6 V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>12.6</td>
<td>64.7</td>
<td></td>
<td>SBIAS = 1.8 V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>12.1</td>
<td>63.6</td>
<td></td>
<td>SBIAS = 2.0 V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>11.9</td>
<td>62.7</td>
<td></td>
<td>SBIAS = 2.2 V</td>
</tr>
</tbody>
</table>

Note: SBIAS drift is calculated by (Max (SBIAS error (T (-40°C) to T (125°C))) - Min (SBIAS error (T (-40°C) to T (125°C)))) / (125°C - (-40°C))

Notes:
1. Average ± 1σ
2. Average ± 5σ

![Figure 21. Drift versus SBIAS](image)

![Figure 22. SBIAS Drift Histogram](image)
2.5 Operating and Standby Current

Table 9 to Table 11 show operating current evaluation results of the A/D converter module-stop state, A/D conversion wait state, and A/D conversion state.

Table 9. Operating Current Evaluation Result of A/D Converter in Module-stop State

Conditions: VCC = AVCC0 = AVCC1 = 3.3 V, VSS = AVSS0 = AVSS1 = 0 V, HOCO clock oscillation frequency = 64 MHz, PCLKB = 32 MHz, MSTPCRD.MSTPD17 = 1b, SDADCCKCR.SDADCCKEN = 0b, SDADCCKCR.SDADCCKSEL = 1b, STC2.BGRPON = 0b, STC2.ADCPON = 0b, ADC2.SDADST = 0b

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Typ</th>
<th>Unit</th>
<th>Test Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Analog power supply current</td>
<td>$I_{AVCC}$</td>
<td>0.1</td>
<td>$\mu A$</td>
<td></td>
</tr>
</tbody>
</table>

Table 10. Operating Current Evaluation Result in A/D Conversion Wait State

Conditions: VCC = AVCC0 = AVCC1 = 3.3 V, VSS = AVSS0 = AVSS1 = 0 V, HOCO clock oscillation frequency = 64 MHz, PCLKB = 32 MHz, MSTPCRD.MSTPD17 = 0b, SDADCCKCR.SDADCCKEN = 1b, SDADCCKCR.SDADCCKSEL = 1b, STC2.BGRPON = 1b, STC2.ADCPON = 1b, ADC2.SDADST = 0b

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Typ</th>
<th>Unit</th>
<th>Test Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Analog power supply current</td>
<td>$I_{AVCC}$</td>
<td>0.90</td>
<td>mA</td>
<td>SDADCSTC1.VREFSEL = 0, SBIAS=2.2V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Normal A/D conversion mode</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0.62</td>
<td></td>
<td>Low power A/D conversion mode</td>
</tr>
</tbody>
</table>

Table 11. Operating Current Evaluation Result in A/D Conversion State

Conditions: VCC = AVCC0 = AVCC1 = 3.3 V, VSS = AVSS0 = AVSS1 = 0 V, HOCO clock oscillation frequency = 64 MHz, PCLKB = 32 MHz, MSTPCRD.MSTPD17 = 0b, SDADCCKCR.SDADCCKEN = 1b, SDADCCKCR.SDADCCKSEL = 1b, STC2.BGRPON = 1b, STC2.ADCPON = 1b, ADC2.SDADST = 1b

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
<th>Test Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Analog power supply current</td>
<td>$I_{AVCC}$</td>
<td>0.97</td>
<td>1.11</td>
<td>mA</td>
<td>SDADCSTC1.VREFSEL = 0, SBIAS=2.2V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0.77</td>
<td>0.90</td>
<td>Normal A/D conversion mode</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Low power A/D conversion mode</td>
</tr>
<tr>
<td>Reference power supply current</td>
<td>$I_{REFI}$</td>
<td>6.0</td>
<td>7.0</td>
<td>$\mu A$</td>
<td>SDADCSTC1.VREFSEL = 1, VREFI = 0.8V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>18.0</td>
<td>22.0</td>
<td>SDADCSTC1.VREFSEL = 1, VREFI = 2.4V</td>
</tr>
</tbody>
</table>

3. Calibration Function

Calibration allows high-precision A/D conversion by calculating the offset error correction value and gain error correction value under the conditions of use. The calibration function performs A/D conversion of the internal or user-specified reference voltage, and then determines the most appropriate correction value from the error included in the conversion result. Calibration is started when 1 is written to the CLBSTR.CLBST bit. A/D conversion is performed several times to calculate the correction factor.

The calibration function should be performed in an environment where the analog block power supply, reference power supply, analog inputs, and SDADC24 reference clock are stable. If calibration is performed in an unstable environment, A/D conversion accuracy might deteriorate.
Table 12. Settings and Operations of Calibration

<table>
<thead>
<tr>
<th>Control register bits</th>
<th>Calculating correction factors for calibration</th>
</tr>
</thead>
<tbody>
<tr>
<td>PGACn.PGASEL</td>
<td>CLBC.CLBMD[1:0]</td>
</tr>
<tr>
<td>0 (Differential input</td>
<td>Don’t care</td>
</tr>
<tr>
<td>00</td>
<td>0</td>
</tr>
<tr>
<td>01</td>
<td>1</td>
</tr>
<tr>
<td>10</td>
<td>1</td>
</tr>
</tbody>
</table>

Note: The correction factors are not calculated for the channels set in single-ended input mode.

Calibration must be performed in the following cases:
- When differential input mode is used for the first time after reset.
- When the VREF mode is switched between external VREF mode and internal VREF mode using the STC1.VREFSEL bit in differential input mode.
- When the voltage is switched between the SBIAS output voltage and VREFI input voltage using the STC1.VSBIAS[3:0] bits in differential input mode.
- When the mode is switched from normal A/D conversion mode to low-power A/D conversion mode, or vice versa in differential input mode.
- When the gain is changed for the same channel in differential input mode.

Notes:
1. Bits for the channel number of an A/D conversion result (ADCR.SDADCRC[2:0]), bit for displaying the status of an A/D conversion result (ADCR.SDADCRS), and bits for the A/D converter conversion result (ADCR.SDADCRRD[23:0]) are not updated during internal or external calibration.
2. When performing internal or external calibration, set the Automatic Scan Mode Selection bit of the Sigma-Delta A/D Converter Control Register 1 (ADC1) to 1 for single scan. For details, see section 3.4.3, Self-Diagnosis Flow of PGA Offset and section 3.4.4, Disconnection Detection Assist Flow.
3. The dOFR voltage cannot be set to a value other than 0 mV (PGACn.PGAOFS[4:0] = 00000b (n = 0 to 4)) during calibration operation.
4. For external calibration operation, multiple channel settings cannot be set to PGACn.PGACVE = 1 (n = 0 to 4) at the same time.

3.1 Internal Calibration Operation Mode

In internal calibration operation mode, offset and gain error correction values are calculated by the internal analog input generated based on the internal reference voltage. The correction values for multiple input channels can be calculated by only one calibration operation. After calibration is started by the CLBSTR.CLBST bit, the offset and gain error correction values are calculated for all input channels set as the calibration targets. Calibration is complete after a calibration completion interrupt (SDADC_CALIEND) is generated. For details on the setting, see Figure 30.

3.2 External Calibration Operation Mode

In external calibration operation mode, calibration is performed based on the user-specified reference voltage. The offset calibration calculates the correction value for the A/D conversion result corresponding to the differential analog input at the time of the offset calibration (VIDOCAL) to be corrected to 0. Gain calibration calculates the correction value for the A/D conversion result corresponding to the value (VIDGCAL - VIDOCAL) calculated by subtracting the differential analog input at the time of the offset calibration (VIDOCAL) from the differential analog input at the time of the gain calibration (VIDGCAL) to be corrected to $2^{23} - 1$. The correction value for one channel is calculated by one calibration operation. To
calculate the offset and gain error correction values, two calibration operations must be performed. When each calibration completes, a calibration completion interrupt (SDADC_CALIEND) is generated. Set the reference voltage for the input channel before each calibration operation is performed (before setting the CLBSTR.CLBST bit to 1). Table 13 shows the user-specified reference voltage in external calibration operation mode. For details on the setting, see Figure 31.

Table 13. User-specified Reference Voltage in External Calibration Operation Mode

<table>
<thead>
<tr>
<th>User-specified reference voltage</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>The differential analog input at the time of the external offset calibration (VIDOCAL)</td>
<td>ANSDnP – ANSDnN (n = 0 to 3) or OPAMP0 - OPAMP1</td>
<td>*1</td>
<td>0</td>
<td>*1</td>
</tr>
<tr>
<td>The differential analog input at the time of the external gain calibration (VIDGCAL)</td>
<td>0.4/GTOTAL</td>
<td>0.8/GTOTAL</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>VIDGCAL - VIDOCAL</td>
<td>0.4/GTOTAL</td>
<td>0.8/GTOTAL</td>
<td>V</td>
<td></td>
</tr>
</tbody>
</table>

Note 1. VIDOCAL and VIDGCAL must be used in a range that satisfies the minimum and maximum values of VIDGCAL - VIDOCAL.

Figure 24. External Calibration

3.3 Recalibration Omitted
When using the differential input mode with the same STC1.SDADLPM, STC1.VSBIAS[3:0], STC1.VREFSEL and PGACn.PGAGC[4:0] bit settings as in the calibration execution, store the values of the GCVLR and OCVLR registers after calibration to the data flash. Recalibration can be omitted by copying the stored value to the GCVLR and OCVLR register from the next time. For details on the settings, see Figure 32.

However, when there is a large temperature change or there is a change in the user environment or use conditions, it is necessary to perform re-calibration.

3.4 Calibration Control Flows
Figure 26 to Figure 32 show the startup flow and calibration flow of the SDADC24.

Figure 25. Overview of Flows
3.4.1 Analog Power Supply Activation Flow

Figure 26 shows the flow for analog power supply activation.

1. Start analog power activation

   MSTPCRD.MSTPD17 = 0

   Set STC1.VREFSEL
   Set STC1.VSBIAS[3:0]
   Set STC1.CLKDIV[3:0]
   Set STC1.SDADLPM

   SDADCCKR.SDADCCKEN = 1
   (System Control Resister)

2. STC2.BGRPON = 1

   Wait for the stabilization wait time
   of ADBGR, SBIAS and ADREG
   by 2 ms

3. STC2.ADCPON = 1

   Wait for the stabilization wait time
   of VBIAS, PGA and sigma-delta
   A/D converter Power ON
   (automatic process by hardware)

4. End analog power activation

   Section where the execution or
   setting order cannot be changed

   Section processed by hardware
   automatically

Cancel the module-stop state.
Set the reference voltage for sensors
(internal or external VREF mode).
Set the 24-bit sigma-delta A/D converter reference clock division.
Set the A/D conversion operation mode:
0: Normal A/D conversion mode
1: Low-power A/D conversion mode.
Supply the 24-bit sigma-delta A/D converter clock (SDADCLK).

Turn on the power of ADBGR, SBIAS, and ADREG.

Turn on the power of VBIAS, PGA, and sigma-delta A/D converter.

Note: The stabilization wait time of VBIAS, PGA and
sigma-delta A/D converter Power ON are delayed
for 20 μs automatically by the internal hardware
processing. If an A/D conversion start trigger is
asserted during this wait, A/D conversion start
must be delayed after a 20 μs wait.

Figure 26. Analog Power Supply Activation Flow
3.4.2 Input Multiplexer Setting Flow
Figure 27 shows the flow for input multiplexer setting.

![Diagram of Input Multiplexer Setting Flow]

- Start input multiplexer setting
- Set PGACn.PGAOSR[2:0] Set the oversampling ratio.
- Set PGACn.PGAGC[4:0] Set the gain.
- Set PGACn.PGAOF[4:0] Set DAC output voltage for offset adjustment.
- Set PGACn.PGASEL Select single-ended input/differential input.
- Set PGACn.PGAPOL Select the polarity of single-ended input (only for single-ended mode).
- Set PGACn.PGAASN Specify the A/D conversion count.
- Set PGACn.PGAAVE[1:0] Select the averaging operation. Select the average data count.
- Set PGACn.PGAREV Select whether to reverse the A/D conversion results of single-ended input (only for negative-side single-ended mode).
- Set PGACn.PGACTN[2:0] Set the A/D conversion count.

Figure 27. Input Multiplexer Setting Flow
### 3.4.3 Self-Diagnosis Flow of PGA Offset

Figure 28 shows the flow for self-diagnosis of PGA offset.

![Diagram](image)

Figure 28. Self-diagnosis Flow for PGA Offset

Note: 1. The results of PGA offset self-diagnosis can be checked from A/D conversion results.
3.4.4 Disconnection Detection Assist Flow

Figure 29 shows the flow for disconnection detection assist.

```
Start disconnection detection assist

ADC1.SDADTMD = 0
ADC1.SDADSCM = 1
Set ADC1.SDADBMP[4:0]

PGA Cn.PGAOFS[4:0] = 00000b
PGA Cn.PGASEL = 1

Start disconnection detection

Note: Start disconnection detection after setting the input voltage for the target channels.

Set a software trigger.
Set single scan mode.
Allow A/D conversion for the detection-target channels (support multi-channel).

Set DAC output voltage for offset adjustment to 0 mV.
Set single-ended input mode for the detection-target channels.

Set the single-ended polarity to the positive or negative side.
Set disconnection detection assist.
Start disconnection detection.
Note: Start disconnection detection after setting the input voltage for the target channels.

Abort A/D conversion

A/D scan completion interrupt

Yes
No

Check the A/D conversion results

ADC2.SDADST = 0

Stop A/D conversion (optional).

Note: This step must be performed once for all single-ended input whether the channel is positive side or negative side.

Check the disconnection detection results.

Set to “do not detect disconnection”.

Set as appropriate.

Set PGACn.PGAPOL
Set PGACn.PGASEL

Yes
No

Completed on the positive and negative sides

ADC1.PGADISA = 0

Set PGACn.PGAPOL
Set PGACn.PGASEL

End disconnection detection assist

---

Figure 29. Disconnection Detection Assist Flow

Note 1. The disconnection detection status can be checked from the A/D conversion results.
```
3.4.5 Internal Calibration Flow

Figure 30 shows the flow for internal calibration.

```
5) Internal calibration flow

Start internal calibration

PGACh.PGAOF$[4:0] = 00000b
PGACh.PGASEL = 0
Set PGACn.PGACVE

CLBC.CLBMD[1:0] = 00b

Set DAC output voltage for offset adjustment to 0 mV.
Calculate the calibration correction factor.
Select Enable (multiple channels can be selected).

Select internal calibration mode.

Select single scan mode.

Start internal calibration.

Confirm that calibration started.

CLBSTR.CLBST = 1

Confirms that CLBSSR.CLBSS is changed from 0 to 1

Calibration completion interrupt

No

Yes

End internal calibration

Section where the execution or setting order cannot be changed
```

Figure 30. Internal Calibration Flow
3.4.6 **External Calibration Flow**

Figure 31 shows the flow for external calibration.

- **Start external calibration**
  - PGA\(_n\).PGAOF\([4:0]\) = 00000b
  - PGA\(_n\).PGASEL = 0
  - Set PGAC\(_n\).PGACVE

- **CLBC.CLBM\([1:0]\) = 01b**

- **ADC1.SDADSCM = 1**

- **CLBSTR.CLBST = 1**
  - Confirm that CLBSR.CLBSS is changed from 0 to 1

- **Calibration completion interrupt**
  - No
  - Yes

- **CLBMD\([1:0]\) = 10b**

- **CLBSTR.CLBST = 1**
  - Confirm that CLBSS is changed from 0 to 1

- **Calibration completion interrupt**
  - No
  - Yes

- **End external calibration**

**Note:** Select only one channel as the target channel.
- Set DAC output voltage for offset adjustment to 0 mV.
- Calculate the calibration correction factor.
- Select differential input.
- Select Enable calibration
- Set only one channel to PGAC\(_n\).PGACVE = 1.
- Set remaining channels to PGAC\(_n\).PGACVE = 0.

Select external offset calibration mode.

Select single scan mode.

Start external offset calibration.
- Note: Before starting calibration, set the input voltage for offset calibration of the target channel.
- Confirm that calibration started.

Select external gain calibration mode.
- Note: Before starting calibration, set the input voltage for gain calibration of the target channel.
- Start external gain calibration.
- Confirm that calibration started.

Section where the execution or setting order cannot be changed

**Figure 31. External Calibration Flow**

**Note:** To perform external calibration for multiple channels, repeat this flow for each channel.
3.4.7 Recalibration Omitted Flow

Figure 32 shows the flow for omitting recalibration.

Recalibration omitted flow

1. Reset release
2. Set SDADC24 registers
3. Use SDADC24 in differential input mode
   - Yes
   - No
4. Have you ever performed a calibration?
   - No
   - Yes
   - The same STC1.SDADLP, STC1.VSBIAS[3:0], STC1.VREFSEL and PGA.Cn.PGAGC[4:0] bits setting as in the calibration function execution
      - No
      - Yes
5. Set 1 to the CLBB0WI bit in the CLBPR register
6. Set 1 to the CLBPRO bit in the CLBPR register
7. Copy the calibration correction value stored in the data flash to the GCVLrn and OCVLrn registers (n = 0 to 4)
8. Clear the CLBPRO bit in the CLBPR register
9. Clear the CLBB0WI bit in the CLBPR register
10. Start A/D conversion of SDADC24
    (see Sigma-Delta A/D converter conversion flow)

Figure 32. Recalibration Omitted Flow
Website and Support

Visit the following vanity URLs to learn about key elements of the RA family, download components and related documentation, and get support.

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RA Product Support Forum  www.renesas.com/ra/forum
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(Rev.4.0-1 November 2017)

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