

By Stanley Hronik

INTRODUCTION

IDT's ALVC and LVC logic families are high performance bus interface components intended for low voltage applications. These components are fully compatible with industry standard components with similar designations, and they are specified for both 3.3V and 2.5V operation.

ALVC components are intended for very fast low voltage applications that have a uniform voltage on all interfaces. ALVC is built using state of the art 3.3V processing to gain maximum speed.

LVC components are built for 5V tolerance and hot insertion applications. LVC components have no clamp diodes to V_{DD} on either inputs or outputs, making the interface tolerant to voltages higher than V_{DD} . LVC can also be used in 2.5V systems to achieve 3.3V or 5V tolerance.

TABLE OF CONTENTS

SCOPE	1
ALVC AND LVC LOGIC FAMILIES	1
Operating Conditions	2
Gate Array Design Approach	2
DC ELECTRICAL CHARACTERISTICS	2
Input Characteristics	3
Non Bus-hold Inputs	3
Bus-hold Inputs	4
Unused and Floating Inputs	5
Output Characteristics	6
ALVC16xxx Output Structure	6
ALVC162xxx Output Structure	7
LVC16xxx Output Structure	8
LVC162xxx Output Structure	10
Temperature Effects and DC Drive	11
I/O Port Characteristics	12
Connecting Outputs Together	12
Bus Contention	12
AC ELECTRICAL CHARACTERISTICS	12
Delay as a Function of Supply Voltage	13
Performance Under Temperature	14
Rise and Fall times	15
Delay as a Function of Load	17
Number of Outputs Switching	18
Output Enables	18
Setup and Hold Times	19
Skew	19
Metastability	19
Undershoot and Overshoot	19
EMI/RFI Problems	20

POWER DISSIPATION	20
Leakage Currents (I_{DD})	20
Input Leakage (ΔI_{DD})	21
Dynamic Switching Current (Q_{dxf})	21
Current Due to Loading	22
CONCLUSIONS	22

SCOPE

This application note is intended as a designer's guide to component selection and usage. The data contained within this document is typical data taken at 25°C and 3.3V V_{DD} , except where otherwise noted. The data has been derived from component characterization where in most cases, the component selected is an ALVCH16x244 or LVCH16x244 type.

Both ALVCH and LVCH have bus-hold on the device bus inputs. Selected components of both families are also available without bus-hold and are designated as ALVC and LVC. ALVC and LVC are fully spec compatible with the bus-hold versions except for the input characteristics associated with bus-hold. Throughout this document references to ALVC and LVC also apply to ALVCH and LVCH except when noted.

Double-Density refers to IDT's family of 48 and 56 pin logic functions. IDT's Quad Density (36 bit) families contain two double density die in a single package, and therefore the data also applies to LVCH36xxx and ALVCH36xxx components except for characteristics affected by packaging.

The data is intended as a design guideline only. For "guaranteed" specifications the IDT Logic Data Book provides full specifications over V_{DD} , temperature and process.

ALVC AND LVC LOGIC FAMILIES

There are several families of parts for use in various applications. All families are designed for use in 3.3V and 2.5V systems and all families represent state of the art speed performance. The individual families and their uses are as follows:

- 1) ALVCH16xxx, Maximum speed performance driving moderate to heavily loaded buses and backplanes. All outputs have $\pm 24mA$ drivers and all data path inputs have bus-hold.
- 2) ALVC16xxx, Identical to ALVCH16xxx except without bus-hold. These parts are ideal for use in applications with thevenin termination or pull up resistors.
- 3) ALVCH162xxx, Excellent low noise performance driving light to moderately loaded buses. These devices have $\pm 12mA$ drivers on at least one port and all data path inputs have bus-hold. In point to point

applications, no additional termination should be needed. A few devices in this family are designed with one port driving $\pm 12\text{mA}$ and the other driving $\pm 24\text{mA}$.

4) ALVC162xxx, Identical to ALVCH162xxx except without bus-hold. These parts are ideal for use in applications with thevenin termination or pull up resistors on the inputs.

5) ALVCHR162xxx, LVCR162xxx, Bidirectional parts with all ports having $\pm 12\text{mA}$ drivers. Parts of this type are simple variations of the ALVC(H)162xxx families.

6) LVCH16xxx, 5V tolerant on all ports and capable of hot insertion. These provide excellent speed performance driving moderate to heavily loaded buses and backplanes. All outputs have $\pm 24\text{mA}$ drivers and all data path inputs have bus-hold.

7) LVC16xxx, Identical to LVCH16xxx except without bus-hold. These parts are ideal for use in applications with thevenin termination or pull up resistors on the inputs.

8) LVCH162xxx, 5V tolerant on all ports and capable of hot insertion. These provide excellent low noise performance driving light to moderately loaded buses. All outputs have $\pm 12\text{mA}$ drivers and all data path inputs have bus-hold. In point to point applications, no additional termination should be needed.

9) LVC162xxx, Identical to LVCH162xxx except without bus-hold. These parts are ideal for use in applications with thevenin termination or pull up resistors on the inputs.

10) LVCHR162xxx, LVCR162xxx, These are bidirectional parts with all ports having $\pm 12\text{mA}$ drivers. Parts of this type are simple variations of the LVC(H)162xxx families.

All families have Balanced Drive, utilizing internal series resistors to control the rising and falling edges of the output waveforms. Balanced Drive provides superior low noise performance by controlling the output edge rates and providing partial series termination of all output signals without sacrificing speed performance. In most applications, additional line termination is unnecessary, but can be added if the application has lengthy transmission lines or other termination needs. The symmetric drive capability will drive a transmission line both HIGH and LOW with similar edge rates, solving most line balance and termination problems.

All families also have industry standard pin outs, and functionality allowing plug in replacement if a family transition is required.

Operating Conditions

All IDT 3.3V Double Density components are specified over the extended temperature range of -40°C to 85°C . The full temperature range specification gives guaranteed performance over a wide range of both indoor and outdoor applications. Some of these may include operation in hot enclosed systems, automotive engine compartments, outdoor equipment in freezing environments and a multitude of hostile

industrial applications. With specifications guaranteed over a wide operating range, superior performance can be expected under nominal conditions.

Both the LVC and ALVC families are guaranteed over several JEDEC operating voltages including the $3.3\text{V} \pm 0.3\text{V}$ Normal Range for 3.3V, the 2.7V to 3.6V Wide Range for 3.3V, and the $2.5\text{V} \pm 0.2\text{V}$ Normal Range for 2.5V operation.

These defined limits for V_{DD} and temperature are test conditions under which the components are tested and guaranteed to operate at data sheet specifications. The components will operate beyond these established test limits if kept within the absolute maximum ratings as defined in each data sheet. Typically components built using CMOS technology will increase in speed under cold conditions and higher V_{DD} levels. CMOS tends to slow down under hot conditions with lower V_{DD} levels.

Component manufacturers frequently place moisture sensitivity ratings on their components. These ratings are used to restrict the air exposure time of components between the time of removing new components from their factory packing materials to final board assembly. IDT standard logic components have no moisture sensitivity and therefore have no restrictions on the air exposure time before final assembly.

Gate Array Design Approach

All IDT Double Density logic is built using standard gate arrays with a "sea of gates". IDT LVC16xxx parts are built from one array type and ALVC16xxx parts are built from a different array type. The arrays allow a final metal mask variation that gives the unique part type logic characteristics. The final metal mask allows a selection of output characteristics between the $\pm 24\text{mA}$ and $\pm 12\text{mA}$ versions and a choice of whether the component will or will not have bus-hold.

Using the standard gate array approach, IDT maintains a high level of consistency from component to component and logic family to logic family. This eases component qualification for most users because a single component qualification can be used to qualify a whole family of products.

DC ELECTRICAL CHARACTERISTICS

Included in the DC Electrical Characteristics are device input and output impedances, drive capabilities and breakdown limitations. The guaranteed DC test limits are shown in the IDT Logic Data Book in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table and OUTPUT DRIVE CHARACTERISTICS table for each component.

When calculating loading, drive capabilities, power dissipation and line termination needs, additional information beyond the data book specifications is often required. This information is supplied here.

Input Characteristics

The input structure of IDT ALVC logic is shown in Figure 1. The structure consists of the gates to a P-Channel and an N-Channel FET. A parasitic clamp diode connects the input to ground, and another connects the input to V_{DD} . These clamp diodes are part of the ESD protection structure for these devices. Components that combine an input with an output (forming an I/O port) will also have these clamp diodes.

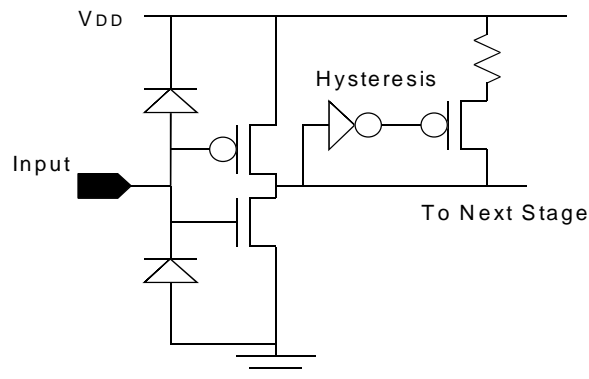


Figure 1, Input Structure for ALVCH and ALVC

The input structure of IDT LVC logic is shown in Figure 2. The structure is similar to the ALVC of Figure 1 except there are no clamp diodes to V_{DD} . This feature allows the input voltage to rise above V_{DD} giving the part the capability of being used for 5V tolerance or for hot insertion. LVC components that combine an input with an output (forming an I/O port) have no clamp diodes to V_{DD} on the I/O port.

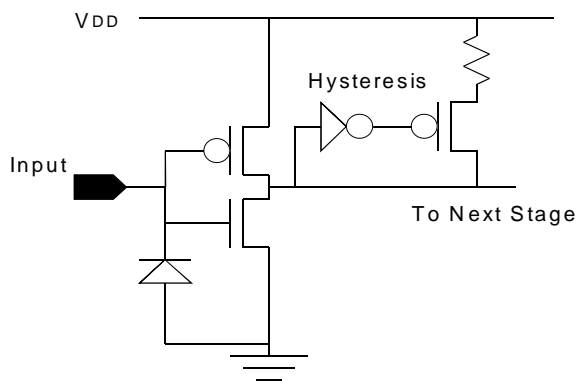


Figure 2, Input Structure for LVCH and LVC

Contained within the input structure of both ALVC and LVC is a hysteresis circuit that provides a weak positive feedback into the input causing a small difference between V_{IH} (logic HIGH threshold) and V_{IL} (logic LOW threshold). This helps to reduce noise induced switching and oscillations that may occur when the input voltage level hovers near the input toggle point as it might with a slowly ramping input.

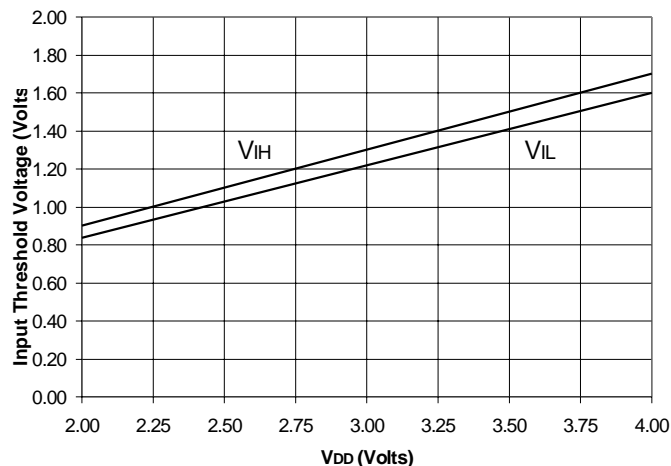


Figure 3, Input Threshold Voltage (V_{ih}/V_{il})

The input threshold voltage for ALVC and LVC logic is set at a nominal 1.5V with $V_{DD} = 3.3V$. At $V_{DD} = 2.5V$, the input threshold scales down to about 1.1V. As can be seen in Figure 3, the input threshold will vary relative to V_{DD} with the input hysteresis causing the slight difference between V_{IH} and V_{IL} . The effect of bus-hold will amplify the apparent input hysteresis if the input driving circuit is not low impedance. The data sheet limit for V_{IL} is 0.8V and the limit for V_{IH} is 2.0V when V_{DD} is between 2.7V and 3.6V. At 2.3V these guaranteed values drop to 0.7V for V_{IL} and 1.7V for V_{IH} .

In addition to the above, ALVC and LVC Double Density devices have the advantage of extremely-low input capacitance where typical values range from 4 to 5pF. This makes it possible for a high-impedance source elsewhere on the board to drive many ALVC or LVC Double-Density inputs.

Non Bus-hold Inputs

The ALVC and LVC (no H in the part number) families have no bus-hold on their inputs. In this configuration, the input impedance of the components is very high, limited to the leakage levels only.

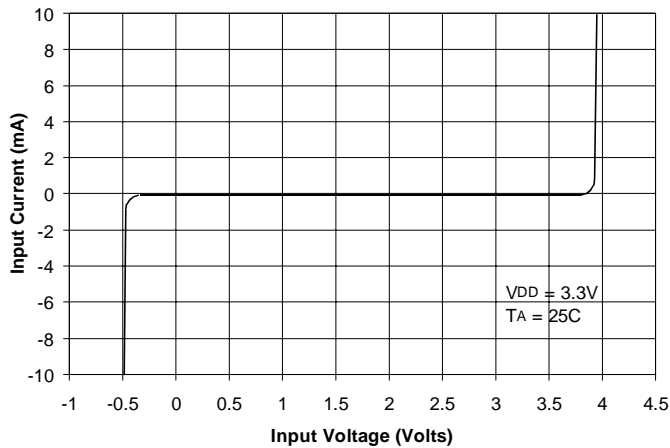


Figure 4, Input Impedance for ALVC

The input impedance of ALVC is shown in Figure 4. As can be seen by the figure, the input has a high impedance except when the input voltage exceeds V_{DD} or drops below ground. At these points the input clamp diodes take effect, allowing high current levels to pass. The maximum input voltage is limited to about 0.5V above V_{DD} regardless of whether V_{DD} is 3.3 or 2.5V.

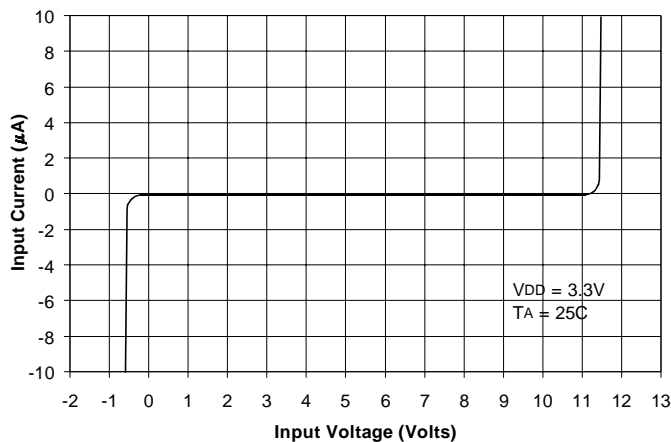


Figure 5, Input Impedance for LVC

The input impedance of LVC is shown in Figure 5. The curve is similar to the ALVC curve of Figure 4, except there is no clamp diode to V_{DD} . As the voltage rises above V_{DD} , the input impedance will remain high until the breakdown level of the component is reached. The breakdown level of LVC components remains constant regardless of V_{DD} , so as V_{DD} drops to 2.5V or lower, the input will remain at a high impedance up to the breakdown voltage. Breakdown typically occurs at some level beyond 10 volts and may cause damage to the component.

Operating a device with the input voltage near or beyond the absolute maximum rating as listed in the data sheet may affect the long term reliability of the component.

Bus-hold Inputs

Components that use bus-hold will automatically drive all 3-state inputs to valid logic states, avoiding floating buses. Figure 6 is a simplified representation of the bus-hold function.

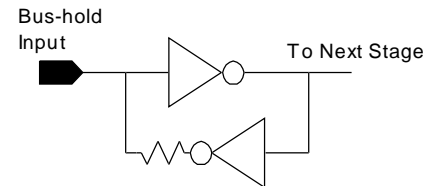


Figure 6, Bus-hold Input Circuit

Inputs with bus-hold will pull themselves and everything else on a bus to a logic HIGH or LOW in a reasonable time period if there is no stronger driver on the bus. Bus-hold inputs should not be used with pull up resistors because the resistor will contend with the bus-hold current, possibly causing a bus to hang at the threshold point. Worst case, pull up resistors with values between 4K and 10K ohm fairly closely match the drive capability of the bus-hold and will contend with a logic LOW bus-hold.

Care should be used when connecting bus-hold inputs with thevenin termination. A typical thevenin termination has a 220 ohm resistor up and a 330 ohm resistor down. This should be strong enough to pull a bus-hold to a logic HIGH, but could very easily hang, especially if there are several bus-hold inputs tied to the bus. When using thevenin termination, the ALVC and LVC families without bus-hold should be used.

Figure 7 shows the input V/I curve for ALVCH device inputs with bus-hold. As the input voltage moves away from the device rail voltages of GND and V_{DD} , the bus-hold circuit will drive current into/out of the input, attempting to bring the voltage back to the rail, avoiding a "floating bus".

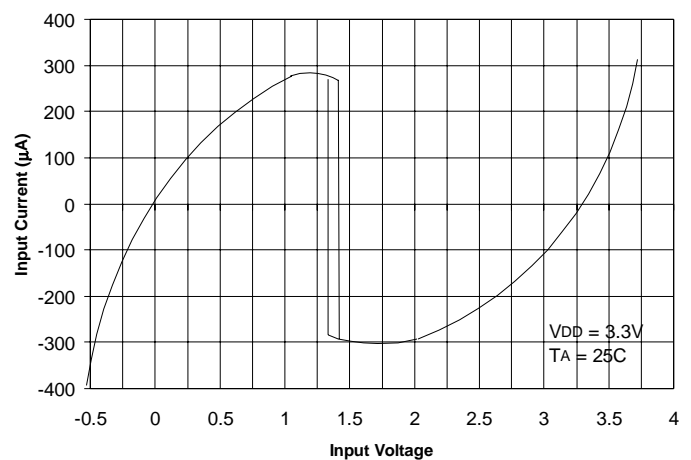


Figure 7, Input VI Curve for ALVCH Bus-hold at $V_{DD} = 3.3V$

Since the ALVCH part is an ALVC part with the addition of the bus-hold circuit, the input clamp diodes still exist and will cause current clamping as the input voltage travels beyond the voltage rails of the component.

From Figure 7 it can be seen that at the logic low threshold of 0.8V, the bus-hold will have a holding current of approximately 250µA. A logic high holding current is about -250µA at the threshold of 2.0V. The maximum external current required to overdrive the input would be about 300µA to transition from a low to a high or -300µA to transition from a high to a low.

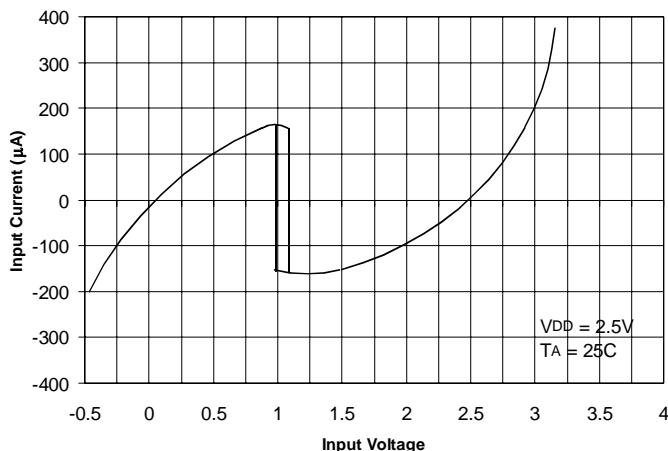


Figure 8, ALVCH Bus-hold at VDD = 2.5V

As VDD drops to 2.5V, the effects of the bus-hold circuitry in the ALVCH family are reduced as can be seen in Figure 8.

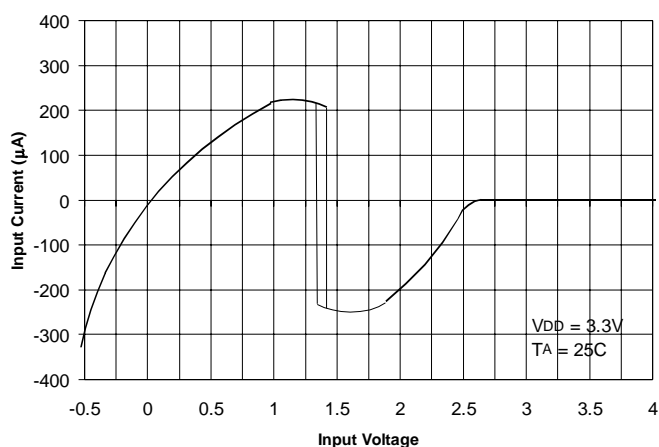


Figure 9, Input VI Curve for LVCH Bus-hold at VDD = 3.3V

The input V/I curve for LVCH is shown in Figure 9. The curve is similar to the ALVCH curve, except there is no clamp diode to VDD limiting the voltage on the input above VDD. LVCH parts with bus-hold have the hot-insertion capability the same as LVC parts.

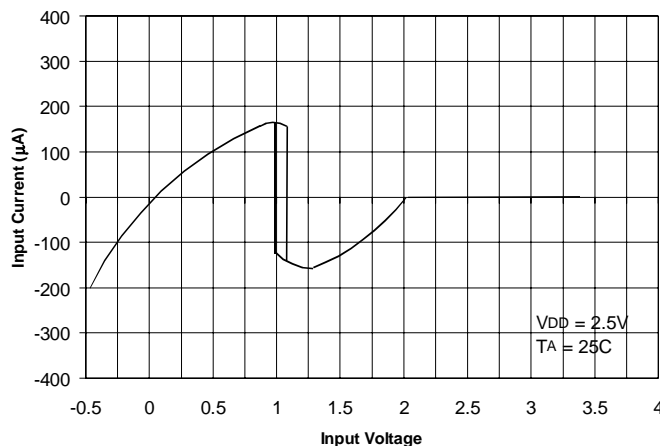


Figure 10, Input VI Curve for LVCH Bus-hold at VDD = 2.5V

As VDD drops to 2.5V on LVCH parts, the drive capability of the bus-hold circuit is reduced as shown in Figure 10.

Bus-hold does not have sufficient drive capability to affect the output toggle rate of a device or affect propagation delays. Bus-hold with its very weak drivers can not contend with the low impedance of a standard output, and therefore will always yield to a stronger driver. While bus-hold is strong enough to pull an input away from the threshold voltage, it cannot be relied upon to “latch” a state in a noisy environment. Bus-hold drivers can easily be overdriven by a transient noise spike that causes the device to toggle.

In a limited number of applications, the performance of bus-hold can be enhanced by tying resistors from the device output back to its bus-hold input. In this case, the device output feeds back current to the input through the resistor to help hold the input. Small value resistors can have a very strong holding effect while large resistors will add very little bus-holding capability. For more information on bus-hold characteristics see APPLICATION NOTE #AN143.

Unused and Floating Inputs

Unused and Floating inputs with bus-hold need no other connection. If it is desired that a bus-hold input (not I/O port) be confined to a state, it can be tied directly to VDD or GND. Unused I/O ports should not be connected directly to VDD or GND because of the possibility the port could act as an output. If an I/O port with bus-hold must be confined to a logic state, it can be pulled high or low with a resistor to VDD or GND. The resistor value should be low enough to overcome any bus-hold currents seen in Figures 7 through 10.

Because of the high input impedance of CMOS components, an input without bus-hold will not drive itself to a valid logic state. Inputs left floating may float near the logic threshold and cause power dissipation as shown in Figure 54. In addition, if the input is picking up a low level, high frequency noise, the input stage may toggle causing the component to oscillate. If the oscillating frequency becomes extreme, the power dissipation of the component may reach high levels, eventually causing device failure.

Special problems may occur with inverting components that have floating inputs. As a floating input toggles the device, the reverse direction of the output switching on an inverter may cause a temporary shifting of the ground reference (ground bounce). A change in ground reference may change the input toggle voltage, causing it to pass back through the floating input voltage. As this back and forth ground shifting continues, the device may go into a high frequency oscillation.

Input hysteresis is present on all IDT logic, and should mitigate many of the oscillation effects caused by noise on a floating input, slowly rising/falling input signals, and bounce. However, a typical 100mV hysteresis level is not sufficient to fully overcome these effects.

Inputs or I/O ports that do not have bus-hold should not be left floating. Unused non bus-hold inputs should be tied directly to V_{DD} or GND to achieve very low input power dissipation. All non bus-hold I/O ports that are not being driven should have a pull up or pull down resistor attached. The resistor value on non bus-hold I/O ports can be anywhere from 500 ohms to 100K. The exact value depends upon the trade offs between a quick recovery, after a driving unconnected I/O port shuts off, and low power dissipation if the I/O port should drive.

Rising and falling input levels of greater than 5 to 10ns should be avoided to insure clean transitions. Slowly rising edges (as may be seen with a large pull up/down resistor) may not produce clean output waveforms, but will cause no component damage

Output Characteristics

Both ALVC and LVC have two options for output characteristics. Both are available in a 16xxx version and a 162xxx version. The output drive characteristics are the distinguishing difference between 16xxx and 162xxx.

The ALVC and LVC 16xxx families are suitable for driving moderate to heavy loads. Applications include all transmission lines, busses, backplanes, distributed loads and general use. These parts have a $\pm 24\text{mA}$ guaranteed drive capability.

The ALVC and LVC 162xxx families have less current drive capability and are more suited for applications that are noise sensitive, or suffer from transmission line noise. While the drivers in these families should drive light loads as quickly as the 16xxx families, the propagation delays will slow down as loads increase. Unless heavy loads are being driven, or maximum speed is required, the 162xxx families will give superior low noise performance with fewer routing and termination constraints.

Because ALVC and LVC use CMOS drivers, the V/I characteristics are linear in the region near zero for V_{OL} . The V_{OH} characteristics are

also linear near V_{DD} . This allows the designer to fairly precisely select termination schemes. Non-CMOS components such as BiCMOS have non-linearities in their drive levels and make termination schemes less precise and more difficult. Because of the nonlinearities of the BiCMOS V/I curve near zero (BiCMOS can not pull to GND), BiCMOS becomes less suitable for use with V_{DD} levels lower than 3.3V. BiCMOS is inadequate for V_{DD} levels of 2.5V and lower.

ALVC16xxx Output Structure

The output structure for the ALVC16xxx family is shown in Figure 11. The approximate impedance values shown include the impedance of the associated FET in saturation. As seen in the figure, the ALVC family has clamp diodes to V_{DD} on all device outputs.

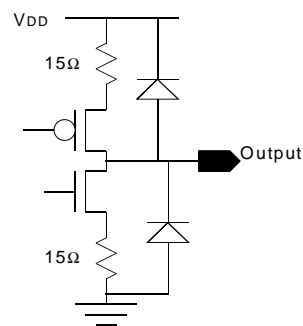


Figure 11, ALVC16xxx Output Structure

The V/I curve shown in Figure 12 represents the pull down characteristics of the ALVC16xxx family. As can be seen by the curve, the typical pull down impedance of the family is approximately 15 ohms with a saturation current of about 180 mA. The guaranteed test point is 24mA at 0.55V with $V_{DD} = 3.0\text{V}$.

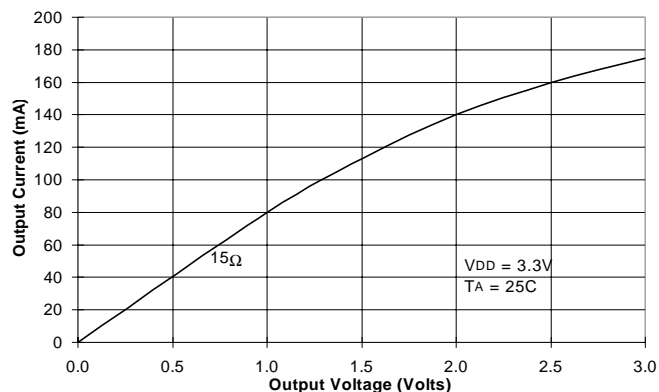


Figure 12, Vol Characteristics of ALVC16xxx at $V_{DD} = 3.3\text{V}$

The pull up characteristics for the family are shown in Figure 13. As can be seen by the curve, the pull up impedance of the ALVC16xxx family is typically about 15 ohms. The guaranteed test point is -24mA at 2.0V with $V_{DD} = 3.0\text{V}$.

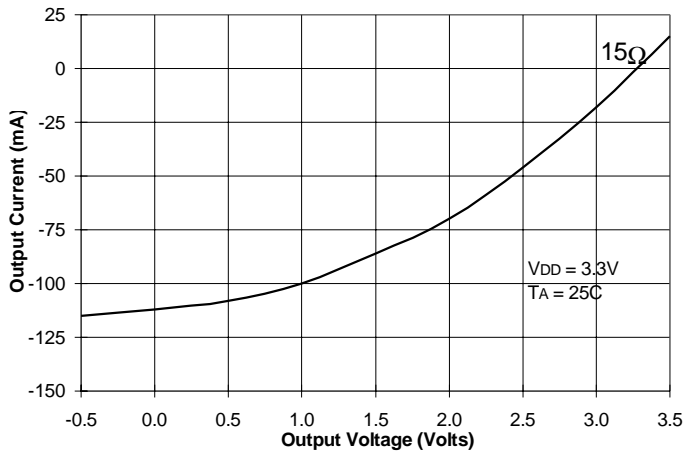


Figure 13, VOH Characteristics of ALVC16xxx at 3.3V

As the level of VDD drops to 2.5V, the output impedance of the ALVC16xxx family remains moderately stable at 15 ohms. The VOL curve operating at 2.5V is shown in Figure 14. The guaranteed test point is 12mA at 0.7V with VDD = 2.3.

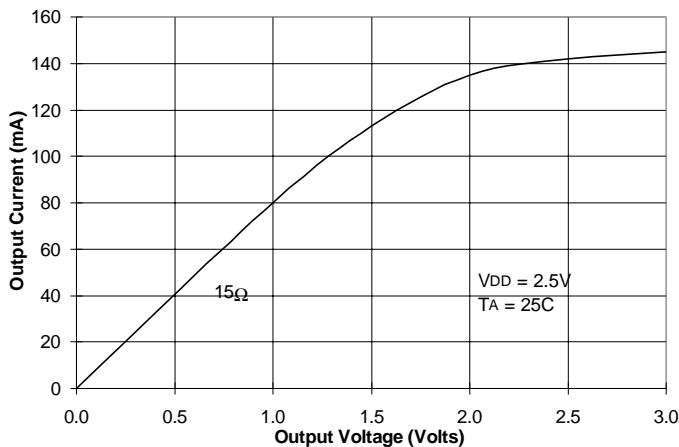


Figure 14, VOL Characteristics of ALVC16xxx at VDD = 2.5V

The pull up impedance for the ALVC16xxx family will increase as shown in Figure 15. As can be seen by the curve, the pull up impedance of the ALVCH16xxx family at 2.5V is typically about 20 ohms. The guaranteed test point is -12mA at 1.7V.

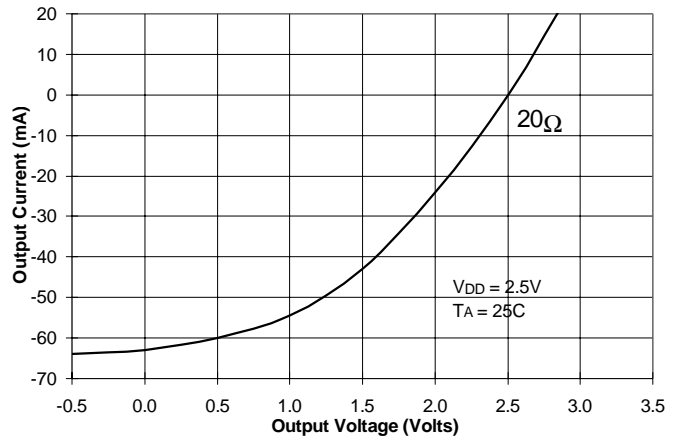


Figure 15, VOH Characteristics of ALVC16xxx at VDD = 2.5V

At voltages other than 3.3V and 2.5V, the output characteristics can be approximated by shifting the curves as needed. Worst case limits and test points can be found in the data sheets for the individual components.

ALVC162xxx Output Structure

The output structure for the ALVC162xxx family is shown in Figure 16. The approximate impedance values shown include the impedance of the associated FET in saturation. The ALVC162xxx family has clamp diodes to VDD on all device outputs, the same as the ALVC16xxx family. Note that some transceivers in this family have a ±12mA driver on one port and a ±24mA driver on the other (the same as ALVC16xxx). See the individual data sheets.

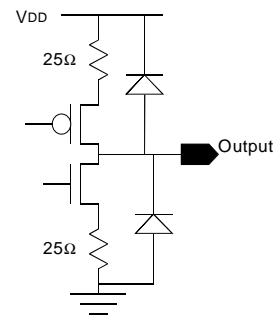


Figure 16, ALVC162xxx Output Structure

The V/I curve shown in Figure 17 represents the pull down characteristics of the ALVC162xxx family. As can be seen by the curve, the typical pull down impedance of the family is approximately 25 ohms with a saturation current of about 95 mA. The guaranteed test point is 12mA at 0.8V with VDD = 3.0V.

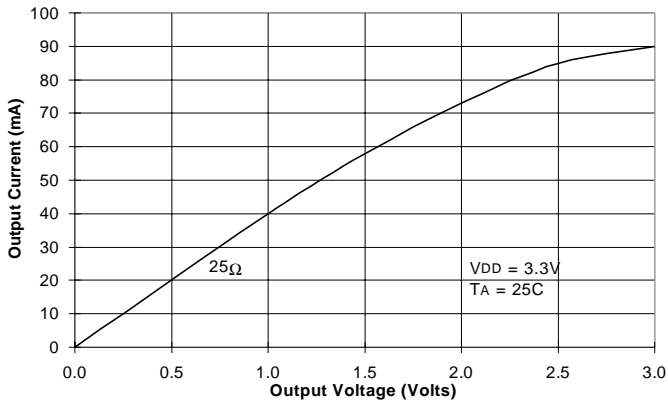


Figure 17, VoL Characteristics of ALVC162xxx at VDD = 3.3V

The pull up characteristics for the family are shown in Figure 18. As can be seen by the curve, the pull up impedance of the ALVC162xxx family is typically about 25 ohms. The guaranteed test point is -12mA at 2.0V with VDD = 3.0V.

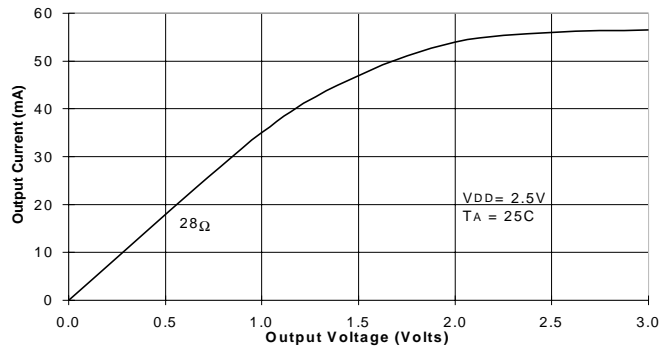


Figure 19, VoL Characteristics of ALVC162xxx at VDD = 2.5V

The pull up impedance for the ALVC162xxx family will also increase as shown in Figure 20. As can be seen by the curve, the pull up impedance of the ALVC162xxx family at 2.5V is typically about 28 ohms. The guaranteed test point is -6mA at 1.7V with VDD = 2.3V.

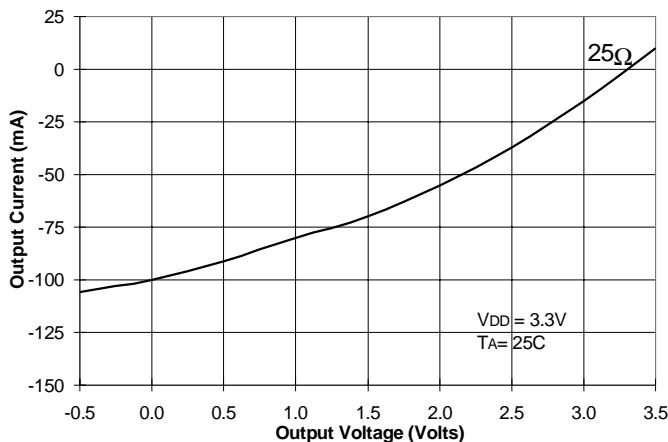


Figure 18, VoH Characteristics of ALVC162xxx at VDD = 3.3V

As the level of VDD drops to 2.5V, the output impedance of the ALVC162xxx family increases. The VoL curve for the ALVC162xxx family operating at 2.5V is shown in Figure 19 where it can be seen that the impedance has increased to 28 ohms. The guaranteed test point is 6mA at 0.55V with VDD = 2.3V.

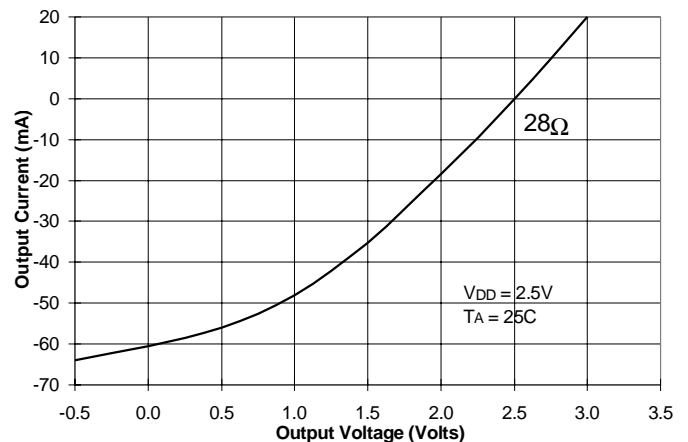


Figure 20, VoH Characteristics of ALVC162xxx at VDD = 2.5V

At voltages other than 3.3V and 2.5V, the output characteristics can be approximated by shifting the curves as needed. Worst case limits and test points can be found in the data sheets for the individual components.

LVC16xxx Output Structure

The output structure for the LVC16xxx family is shown in Figure 21. The approximate impedance values shown include the impedance of the associated FET in saturation. As seen in the figure, there are no clamp diodes to VDD in the LVC family on any device outputs. In addition there is a blocking diode to VDD that prevents current flowing from the output to VDD if the output is externally driven to voltages higher than VDD. The diode allows the LVC16xxx family to be used for hot insertion or voltage translation.

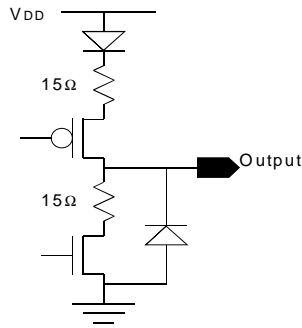


Figure 21, LVC16xxx Output Structure

The V/I curve shown in Figure 22 represents the pull down characteristics of the LVC16xxx family. As can be seen by the curve, the typical pull down impedance of the family is approximately 15 ohms with a saturation current of about 150 mA. The guaranteed test point is 24mA at 0.55V with $V_{DD} = 3.0V$.

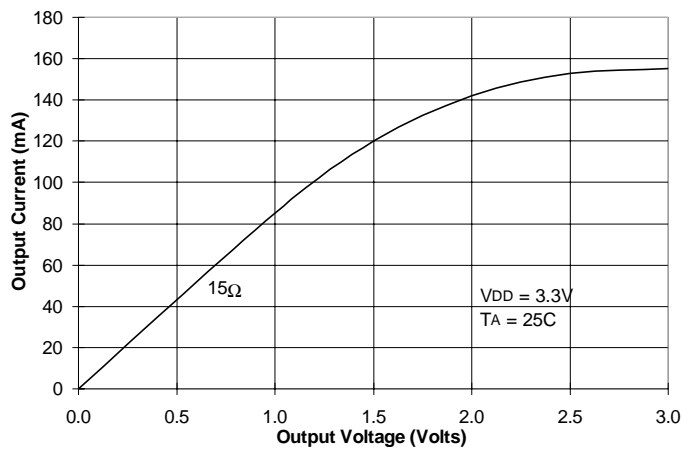


Figure 22, V_{OL} Characteristics of LVCH16xxx at $V_{DD} = 3.3V$

The pull up characteristics for the family are shown in Figure 23. As can be seen by the curve, the pull up impedance of the LVCH16xxx family is typically about 15 ohms. The guaranteed test point is -24mA at 2.0V.

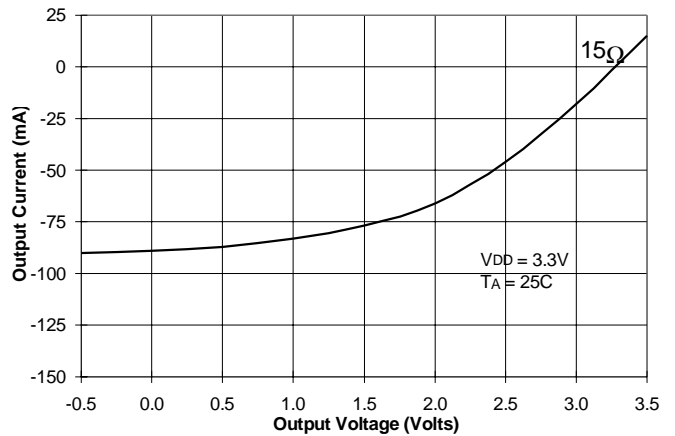


Figure 23, V_{OH} Characteristics of LVC16xxx at $V_{DD} = 3.3V$

As the level of V_{DD} drops to 2.5V, the output impedance of the LVC family remains moderately stable at about 15 ohms. The V_{OL} curve for the LVC16xxx family operating at 2.5V is shown in Figure 24. The guaranteed test point is 12mA at 0.7V with $V_{DD} = 2.3V$.

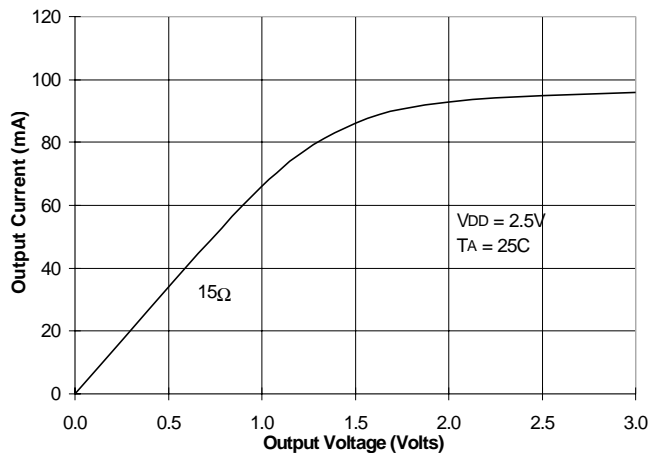


Figure 24, V_{OL} Characteristics of LVC16xxx at $V_{DD} = 2.5V$

The pull up impedance for the LVC16xxx family will increase as V_{DD} is lowered as shown in Figure 25. As can be seen by the curve, the pull up impedance of the LVC16xxx family at 2.5V is typically about 28 ohms. The guaranteed test point is -12mA at 1.7V.

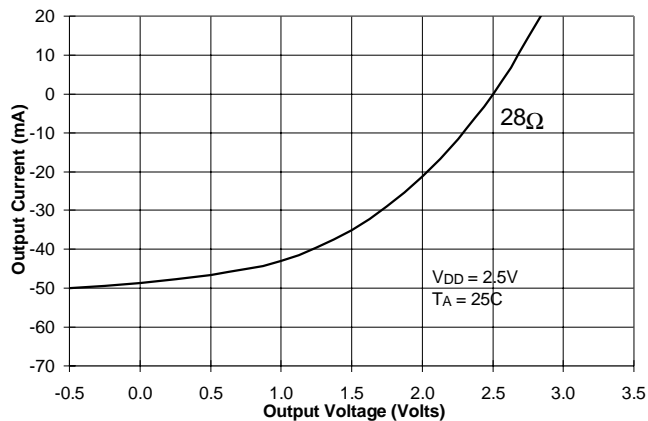


Figure 25, V_{OH} Characteristics of LVC16xxx at V_{DD} = 2.5V

At voltages other than 3.3V and 2.5V, the output characteristics can be approximated by shifting the curves as needed. Worst case limits and test points can be found in the data sheets for the individual components.

LVC162xxx Output Structure

The output structure for the LVC162xxx family is shown in Figure 26. The approximate impedance values shown include the impedance of the associated FET in saturation. The LVC162xxx family has no clamp diodes to V_{DD} on any device outputs, the same as the LVC16xxx family. The LVC162xxx family also has the blocking diode, the same as with LVC16xxx. Note that some transceivers in this family have a ±12mA driver on one port and a ±24 mA (LVC16xxx) driver on the other. See the individual data sheets.

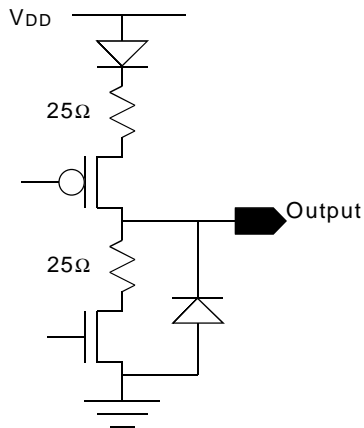


Figure 26, LVC162xxx Output Structure

The V/I curve shown in Figure 27 represents the pull down characteristics of the LVC162xxx family. As can be seen by the curve, the typical pull down impedance of the family is approximately 25 ohms with a saturation current of about 55mA. The guaranteed test point is 12mA

at 0.8V with V_{DD} = 3.0V.

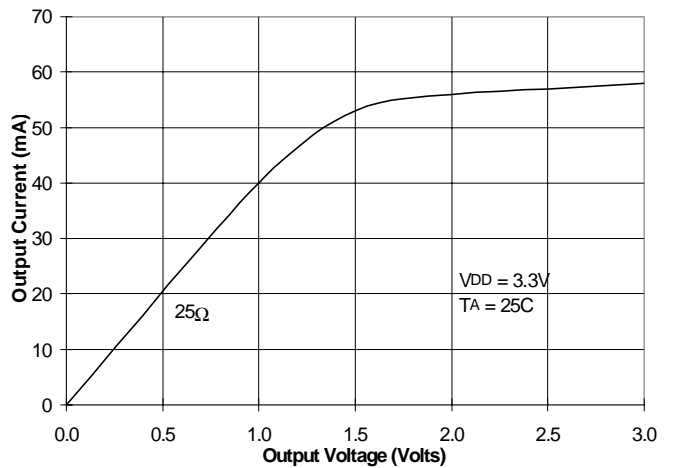


Figure 27, V_{OL} characteristics of LVC162xxx at V_{DD} = 3.3V

The pull up characteristics for the family are shown in Figure 28. As can be seen by the curve, the pull up impedance of the LVC162xxx family is typically about 25 ohms. The guaranteed test point is -12mA at 2.0V with V_{DD} = 3.0V.

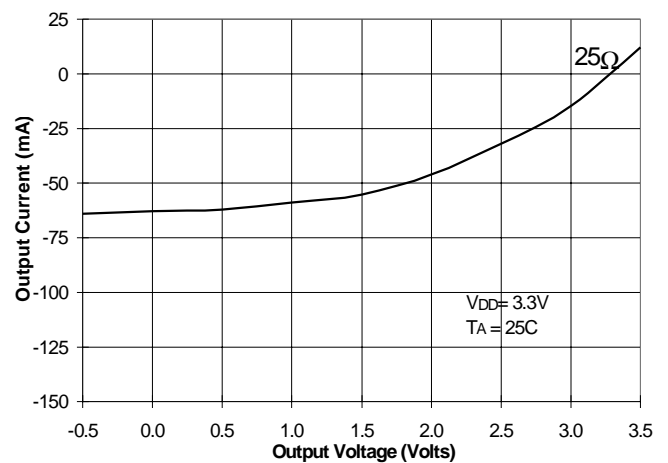


Figure 28, V_{OH} Characteristics of LVC162xxx at V_{DD} = 3.3V

As the level of V_{DD} drops to 2.5V, the output impedance of the LVC162xxx family increases to about 35 ohms. The V_{OL} curve for the LVCH162xxx family operating at 2.5V is shown in Figure 29. The guaranteed test point is 6mA at 0.55V with V_{DD} = 2.3V.

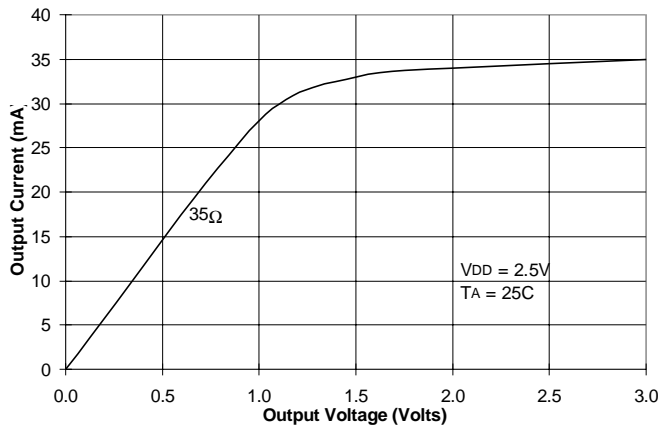


Figure 29, VoL characteristics of LVC162xxx at VDD = 2.5V

The pull up impedance for the LVC162xxx family will also increase as shown in Figure 30. As can be seen by the curve, the pull up impedance of the LVCH162xxx family at 2.5V is typically about 35 ohms. The guaranteed test point is -6mA at 1.7V with VDD = 2.3V.

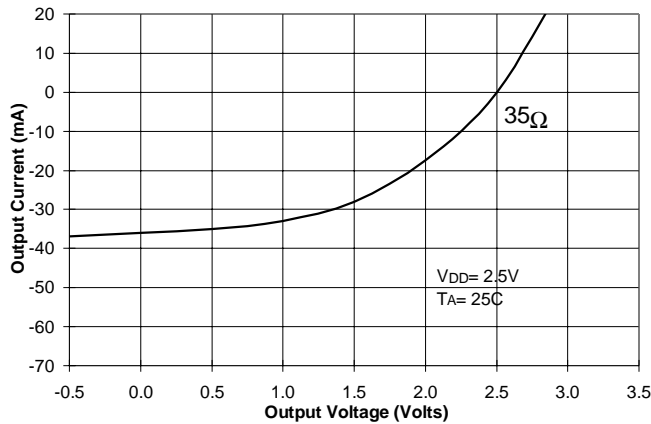


Figure 30, VoH Characteristics of LVC162xxx at VDD = 2.5V

At voltages other than 3.3V and 2.5V, the output characteristics can be approximated shifting the curves as needed. Worst case limits and test points can be found in the data sheets for the individual components.

Temperature Effects and DC Drive

Temperature affects the gain of integrated circuits and will therefore have an effect on the drive level of all CMOS devices. Figure 31 shows how the VoL of a Double Density ALVC or LVC component will change with temperature while delivering 24mA of current. In the graph the

LVC16xxx and ALVC16xxx are represented by the two lower lines (lower impedance) and the LVC162xxx and ALVC162xxx are represented by the upper two lines (higher impedance).

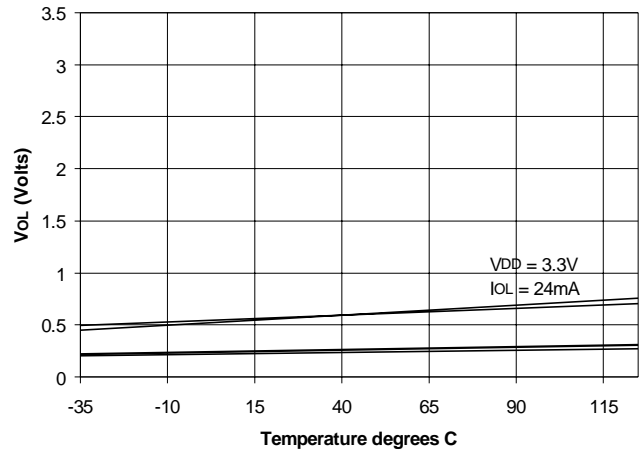


Figure 31, Variation in VoL with Temperature

VoH is also affected by temperature. The effect of temperature under a -24mA load is shown in Figure 32. The LVC16xxx and ALVC16xxx families are represented by the upper two lines and the components with higher output impedance, LVC162xxx and ALVC162xxx are represented by the lower lines.

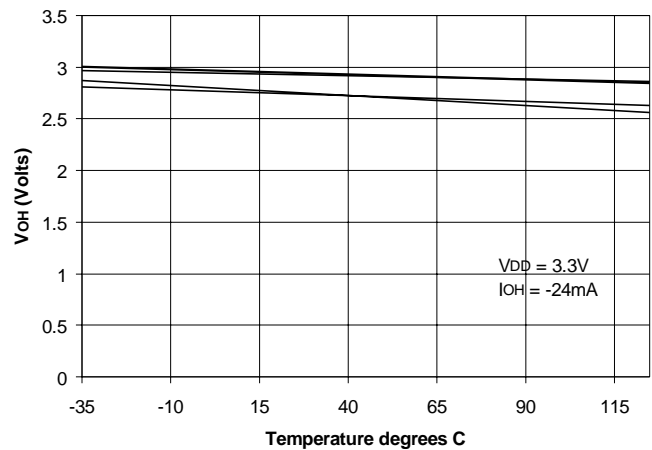


Figure 32, Variation in VoH with Temperature

As seen by the graphs, components with higher output impedance are more affected by variations in temperature than lower impedance components in absolute terms, but proportionally the effect is about the same.

I/O Port Characteristics

I/O Ports are simple combinations of input and output structures on the same pin. When acting as an output driver, an I/O port will have identical characteristics to a standard unidirectional output port from the same family. When the output driver is 3-stated (High Z) the port will be acting as an input port and have identical characteristics to a standard unidirectional input port of the same family. When acting as an input port, ALVCH I/O ports will exhibit the bus-hold characteristics of the ALVCH family and LVCH I/O ports will exhibit the bus-hold characteristics of the LVCH family. These characteristics were described earlier under the topic of bus-hold.

Connecting Outputs Together

Occasionally in an application where a very strong drive is needed, it is possible to connect two outputs together to double the drive capability of the device as shown in Figure 33. When connecting outputs together certain rules must be followed to prevent potentially damaging the component output structure.

1. The two outputs must be from the same component.
2. The two outputs should be adjacent pins and shorted with a trace between the two pins.
3. The two inputs should be shorted with a trace between the two pins.
4. The two outputs must always have the same state (for instance a counter may toggle state and destroy itself).

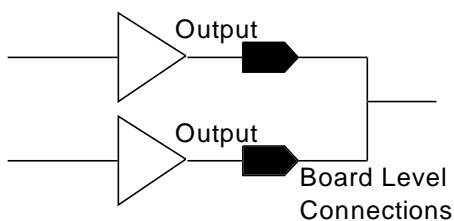


Figure 33, Connecting Outputs Together

When connecting outputs together to achieve higher current levels, care must be taken to not exceed the maximum current level of the component V_{DD} or GND as shown in the ABSOLUTE MAXIMUM RATINGS table of the data sheet.

Bus Contention

ALVC and LVC logic cannot be used to perform any type of wire 'OR' or 'AND' dot functions except when using open drain outputs. ALVC and LVC are designed for high performance and have drive levels that are sufficiently strong to cause damage either to the component or other devices on the bus in the case of sustained bus contention or wire 'OR' operations.

A common system design error is attempting to identify possible bus contention situations by calculating bus timings using "worst case" propagation delays on some components combined with "best case" propagation delays on others. Worst case is found under hot, low V_{DD} conditions while best case is found under cold, high V_{DD} conditions. These two conditions are not usually combined in a system, meaning that it is not practical to attempt to calculate system timings using best and worst case conditions within the same timing calculations.

Output disable times are shorter than output enable times in ALVC and LVC devices, avoiding bus contention when switching with common control signals. The data book times for enable/disable tend to be somewhat lengthy compared to typical delays seen in the components. The passive test method used to measure output disable times (a pull up resistor) tends to extend the disable time measurement well beyond the time the component has released the output.

Brief periods of bus contention, not exceeding 1 to 2ns during switching, should not cause device damage in most cases. During contention the power dissipation will rise to very high levels, possibly causing overheating if the contention is frequent or a significant portion of the duty cycle. Lengthy bus contention of several nsec that may develop from two simultaneously active devices may cause device damage.

Problems with bus contention tend to occur in several scenarios. The most obvious is when there is a "collision" on the bus when two devices simultaneously access an active bus and cause excessive, lengthy currents to flow. Another scenario is during power up when the bus is not yet "under control", and lengthy damaging currents are allowed to flow as two components drive the bus in opposition. The last scenario is when a component with lengthy propagation delays is removing itself from a bus at the same time a "high speed" component is accessing the bus and lengthy high currents are allowed to pass.

Careful system design can avoid these issues, but it isn't necessary to go to extreme sacrifices to avoid contention. It should be possible to both exit a bus with one component and enter the bus with another during the same clock cycle without experiencing damaging levels of bus contention in the exchange if consideration is given to the timing of the transition.

AC ELECTRICAL CHARACTERISTICS

The AC specifications for each component are available in the SWITCHING CHARACTERISTICS OVER OPERATING RANGE table in the data sheet for each component.

The AC limits of the ALVC and LVC families are specified at the worst case temperature condition of $T_A = 85^\circ\text{C}$. The guaranteed temperature range is from $T_A = -40^\circ\text{C}$ to $T_A = 85^\circ\text{C}$ with better performance expected at the cooler temperatures.

ALVC and LVC AC performance levels are guaranteed over three voltage ranges, namely the normal 3.3V range of 3.0V to 3.6V, the extended range of 2.7V to 3.6V, and the nominal 2.5V range of 2.3V to 2.7V. These components should function well in either 3.3V or 2.5V applications.

All AC parameters are measured using the industry standard test load as shown in Figure 34. Propagation delay measurements are taken with the switch open. Enable and disable measurements are taken with the switch connected to 6V or GND depending upon the test.

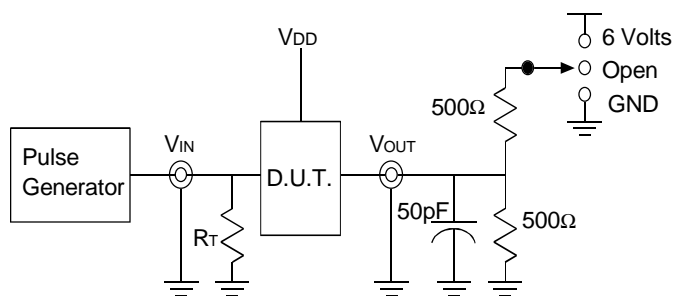


Figure 34, Standard Test Circuit

Standard AC tests are done with a single bit switching. Timings may need to be derated for the worst case of 16/18/20-bits switching simultaneously. When using Double Density logic with 8 GNDs and 4 V_{DD} pins, the effect of multiple bits switching is not significant; but, the designer may wish to add a couple of hundred pico seconds to the stated propagation delays for all bits switching as padding. In most cases the effect will disappear in tester margins and the user will experience no performance degradation over stated data book values.

Testing for 2.5V AC performance levels is done using the 2.5V standard test load of 30pF rather than the 50pF of the 3.3V world.

Delay as a Function of Supply Voltage

Component propagation delay is sensitive to changes in V_{DD} . Typically higher V_{DD} levels will increase component speed and reduce propagation delays. The following figures show propagation delays using the standard 3.3V test load of 50pF and 500 ohms. While the voltages shown extend to well below 2.5V, the values do not directly correlate with 2.5V performance numbers measured with a 30pF 500 ohm load.

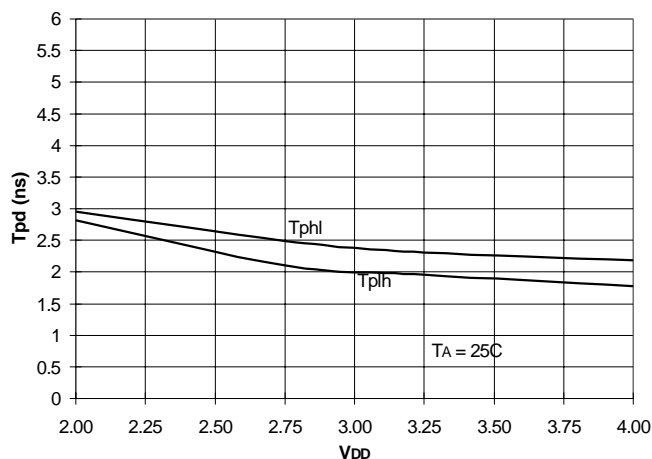


Figure 35, Propagation Delay vs. V_{DD} for ALVC16xxx

Figure 35 shows the propagation delay effects due to changes in V_{DD} on the ALVC16xxx family. Of the families described in this application note, ALVC16xxx has the least amount of variation due to changes in V_{DD} .

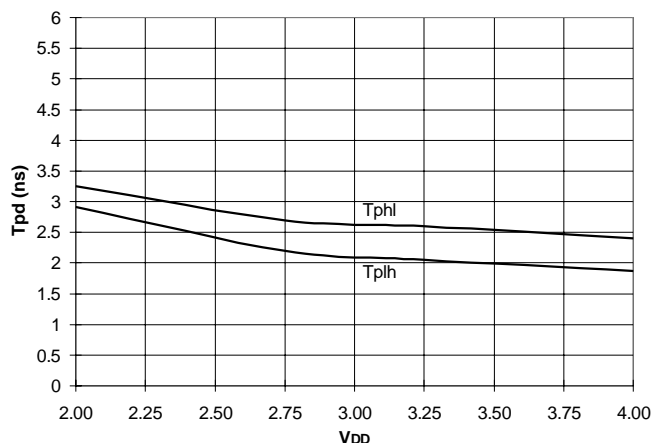


Figure 36, Propagation Delay vs. V_{DD} for ALVC162xxx

Figure 36 shows the effect of V_{DD} on the propagation delay of an ALVC162xxx component. Because of the higher impedance of the ALVC162xxx component, the V_{DD} level has a more significant effect than on the ALVC16xxx component.

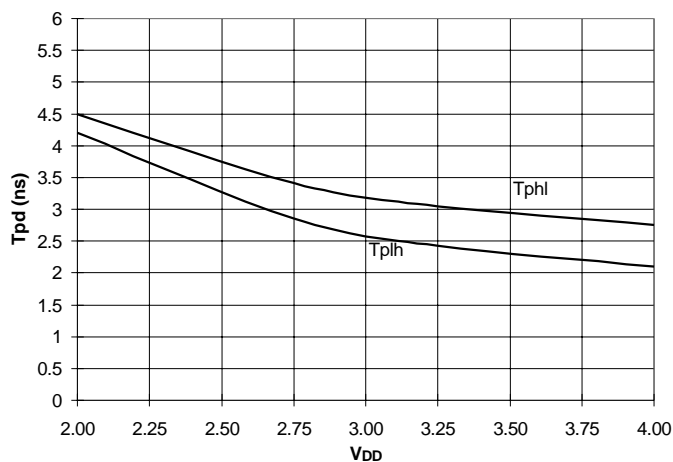


Figure 37, Propagation Delay vs. VDD for LVC16xxx

The LVC16xxx component of Figure 37 shows excellent stability in the propagation delay relative to changes in VDD. The effect of VDD is slightly more pronounced on the LVC family than ALVC because of the additional circuitry in the LVC family to provide the overvoltage tolerance on the device inputs and outputs.

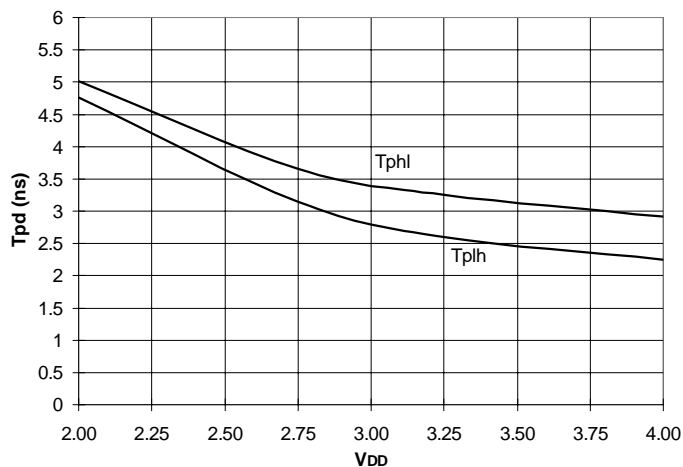


Figure 38, Propagation Delay vs VDD for LVC162xxx

The LVC162xxx family shown in Figure 38 is slightly more affected by VDD than any of the other families shown, but still demonstrates excellent performance over a wide variety of VDD levels, despite having a higher output impedance than the 16xxx families.

Performance Under Temperature

Propagation delay will vary with changes in temperature. Typically these variations are small compared to variations in VDD, but they are present and do have an effect. As the temperature rises, the propagation delay will increase. As the temperature lowers, the component will

demonstrate improved speed performance. The data book specifications are guaranteed between -40°C and 85°C for all ALVC and LVC components with the maximum propagation delay measured at 85°C and the minimum at -40°C. The data book limits have been set for testing purposes only and do not imply a failure to operate outside of these ranges. These components will operate easily below -40°C without damage, but may exhibit performance levels faster than the data sheet limits. The components will also operate at temperatures above 85°C, but may exhibit performance levels slower than indicated in the data sheet. The maximum temperature of the component die should be limited to 150°C including heat generated by internal power dissipation, beyond which component degradation may occur (metal migration). The die temperature can be calculated using the thermal data in section 4 of the IDT Logic Data Book and the POWER SUPPLY CHARACTERISTICS table in each data sheet.

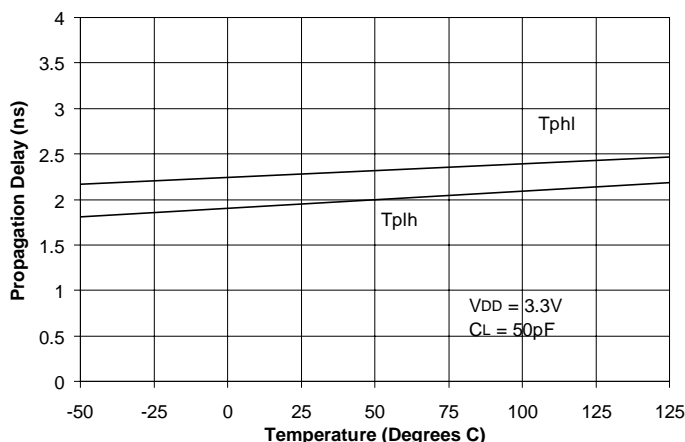


Figure 39, Delay vs. Temperature in an ALVC16244

Figure 39 shows how the propagation delay will vary with temperature for both t_{plh} and t_{pl} for an ALVC16244. As can be seen by the curve, the speed degradation due to temperature is about 150ps per 100°C.

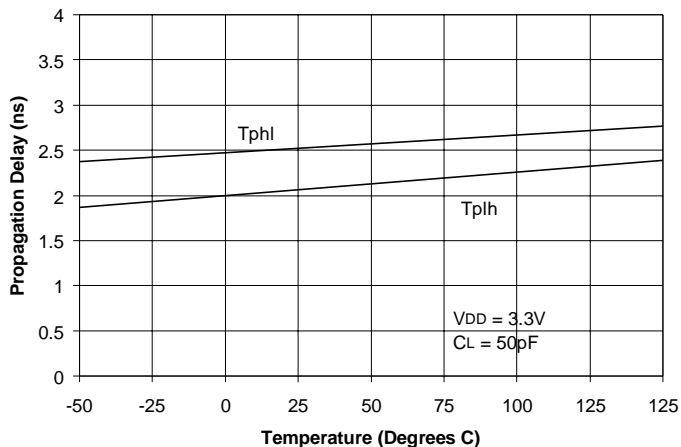


Figure 40, Delay vs. Temperature in an ALVC162244

Figure 40 shows how the propagation delay will vary with temperature for both t_{phl} and t_{plh} for an ALVC162244. As can be seen by the curve, the speed degradation due to temperature is about 200ps per 100°C.

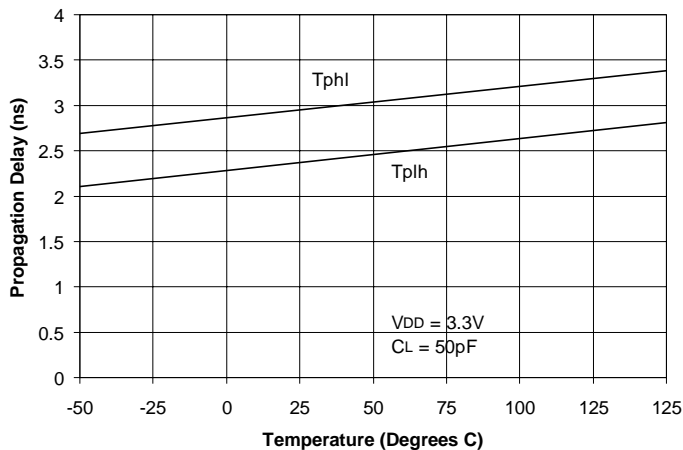


Figure 41, Delay vs. Temperature in an LVC16244

Figure 41 shows how the propagation delay will vary with temperature for both t_{phl} and t_{plh} for an LVC16244. As can be seen by the curve, the speed degradation due to temperature is about 300ps per 100°C.

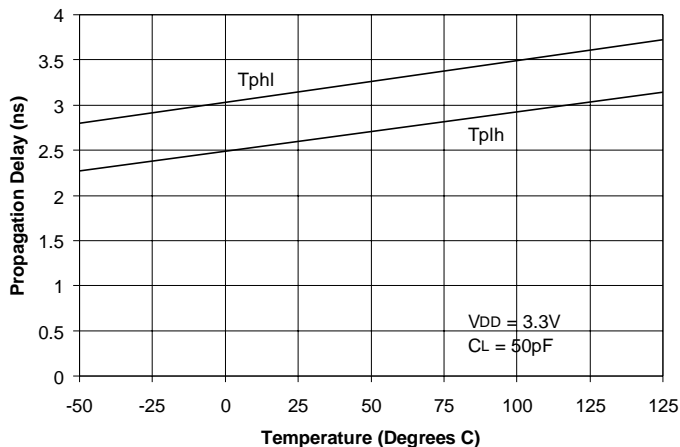


Figure 42, Delay vs. Temperature in an LVC162244

Figure 42 shows how the propagation delay will vary with temperature for both t_{phl} and t_{plh} for an LVC162244. As can be seen by the curve, the speed degradation due to temperature is about 400ps per 100°C.

Rise and Fall Times

When calculating transmission line effects, it is necessary to know the rise and fall times of the drivers under the intended load. All IDT logic has output edge rate control, but in order to achieve a very fast throughput (short propagation delays), the amount of edge rate control must be limited. As the load increases, the rise/fall times will naturally increase (slowing the edge), reducing the need for line termination. Wherever possible, ALVC162xxx or LVC162xxx should be used over the 16xxx families to avoid the faster edge rates. The following rise and fall times are measured from the time a transitioning signal passes from 10% of its final level to 90% of its final state. While an edge rate has an influence on propagation delays, a signal can quickly pass from its initial state to the threshold point (1.5V for 3.3V operation) to measure propagation delay and then slowly transition to its final state. The slower the signal makes the final transition, the fewer line noise problems it will develop.

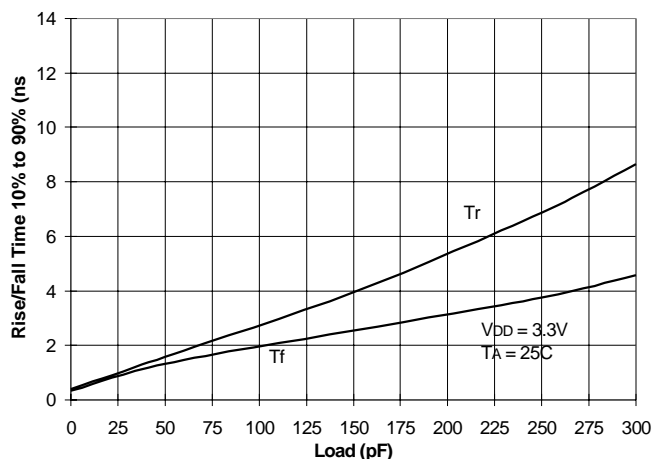


Figure 43, Rise/Fall Time, ALVC16xxx

The rise and fall times for an ALVC16xxx component are shown in Figure 43. While theoretically the device will approach infinite slew rate as the load approaches zero, the loading of the component output structure and mounting will prevent reaching zero. As can be seen by the curve, the increase in rise and fall time for ALVC16xxx is approximately 2.0ns per 100pF of load.

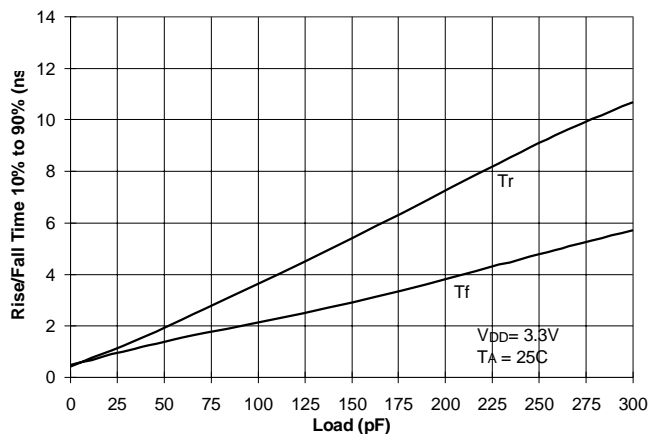


Figure 44, Rise/Fall Time, ALVC162xxx

Figure 44 shows the rise/fall time for an ALVC162xxx component. The effect of the additional internal series impedance in the component output structure can be seen as the falling edge is slower under load than for ALVC16xxx. As can be seen by the curve, the increase in rise and fall time for ALVC162xxx is approximately 3.0ns per 100pF of load.

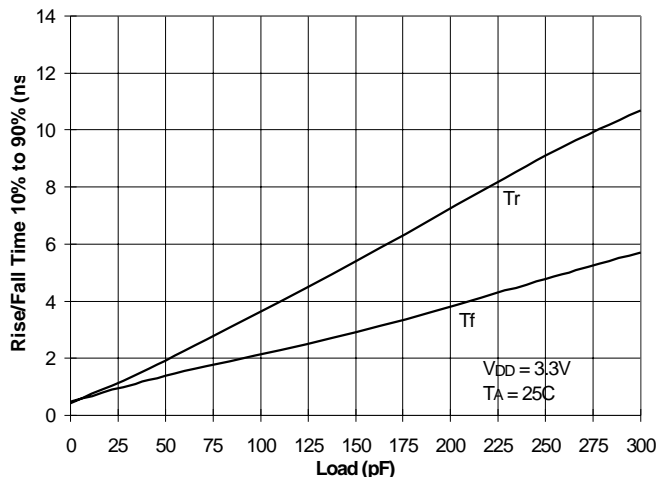


Figure 45, Rise/Fall Time, LVC16xxx

Figure 45 shows rise and fall times for an LVC16xxx component. LVC is naturally slower than ALVC and exhibits slower edge rates than the faster family. These slower edge rates simplify issues with line termination, board routing and EMI. LVC is an excellent choice for a general purpose family where the speed of ALVC is not needed. As can be seen by the curve, the increase in rise and fall time for LVC16xxx is approximately 2.5ns per 100pF of load.

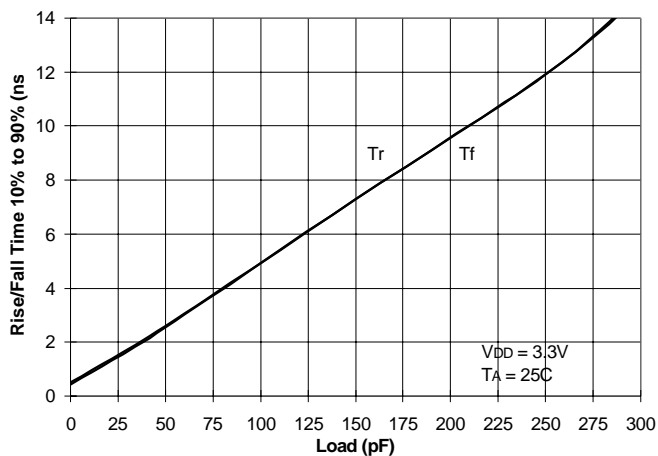


Figure 46, Rise/Fall Time, LVC162xxx

Figure 46 shows the rise/fall time for an LVC162xxx component. These components have the slowest edge rates of the four families described and will give quieter performance than any of the other families. These components are ideal where low noise is needed on lightly loaded interfaces or in applications where external series resistors would otherwise be used to control edge rates with a stronger device. In applications where the load is less than 100pF and achieving first incident wave switching in a distributed load is not important, LVC162xxx in most applications will give significantly superior low noise perfor-

mance than any of the other 3.3V families described. No additional line termination is usually needed with the LVC162xxx family. The increase in rise and fall time for LVC162xxx is approximately 4.5ns per 100pF of load.

Delay as a Function of Load

Data sheet performance specifications are based on an industry standard load of 50pF and 500 ohm for 3.3V or 30pF, and 500 ohm for 2.5V unless otherwise noted. Realistic loads are typically capacitive only (unless DC terminated) and in most cases will be something other than these values.

As the load on an output increases, the effective delay through the component will increase. This is primarily because of the increase in the rise and fall time of the device output delaying the time the signal will cross the logic threshold. Also, the increased load may exceed the current supplying capacity of the component temporarily, adding additional delay while the load charges.

Figures 47 through 49 show the change in propagation delay as a function of external load. These characteristics are essentially linear and can be extrapolated for heavier loads. Loads above 400pF may draw significant current levels when switching at high frequencies and the designer must be careful not to exceed the maximum power dissipation specifications.

The following examples are for a typical 16x244 type component. Other components respond similarly except there may be an additional propagation delay due to the normal internal delay of the component. The internal delay is not affected by load; therefore, the slope of the line in Figure 47, Figure 48, Figure 49, and Figure 50 will remain constant for all parts of the same drive type, but the Tpd intersect point will shift higher or lower according to part type.

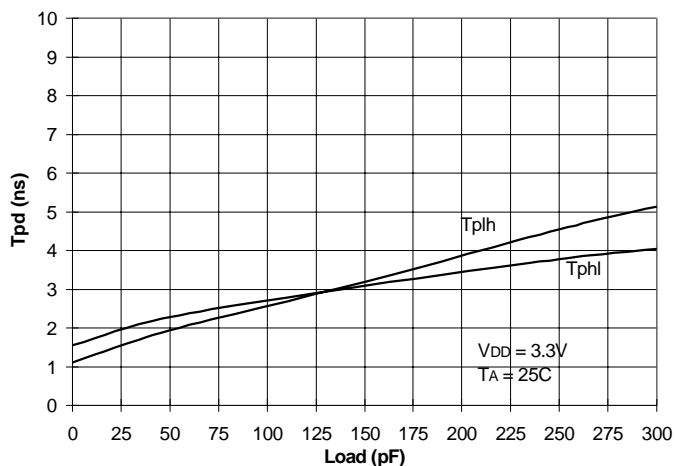


Figure 47, Delay vs. Load for ALVC16244

Figure 47 shows how the effective propagation delay of an ALVC16xxx component will increase with an increase in load. These components have a lower output impedance than ALVC162xxx components and therefore will be less affected by loading. The propagation delay derating for ALVC16xxx is approximately 1.2ns per 100pF of additional loading.

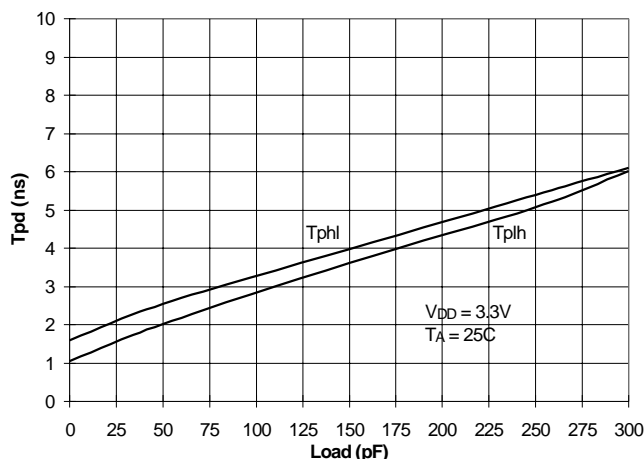


Figure 48, Delay vs. Load for ALVC162244

The ALVC162xxx delay as shown in Figure 48 will be more affected by load than 16xxx. The increased output impedance of ALVC162xxx causes a larger RC time constant and hence a longer overall propagation delay. Because of the longer delay under heavy loads, ALVC162xxx is less suited to driving heavy loads than ALVC16xxx. The derating on ALVC162xxx is approximately 1.7ns per 100pF of additional loading.

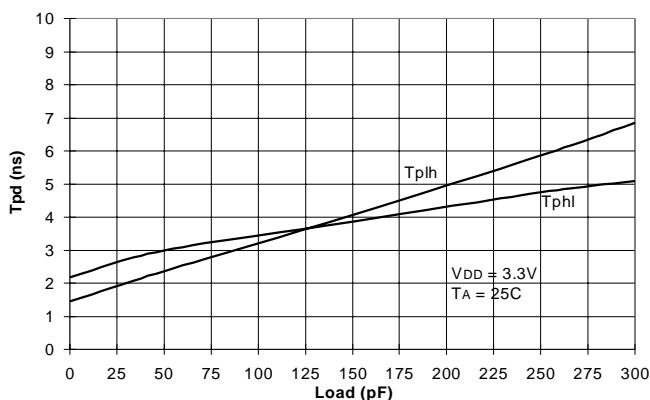


Figure 49, Delay vs. Load for LVC16244

LVC16xxx has more drive capability than any of the 162xxx families. This makes the family better suited to driving backplanes and heavy interfaces than some of the other families. As shown in Figure 49 LVC16xxx is less affected by capacitive loading of its outputs than 162xxx. The derating of the propagation delay of LVC16xxx is approximately 1.3ns per 100pF.

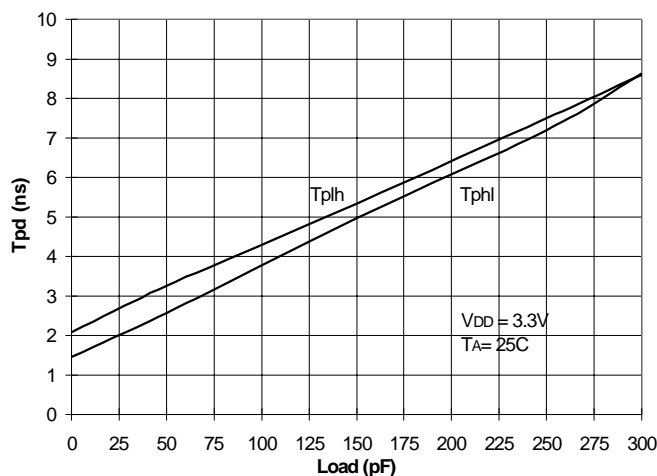


Figure 50, Delay vs. Load for LVC162244

Figure 50 shows the effective propagation delay of an LVC162xxx component under various loads. The LVC162xxx family has a higher output impedance than 16xxx families and will generate longer delays under increasing loads than their counterparts with stronger drive. The LVC162xxx family has the slowest propagation delay of all of families described in this application note. As a result, it will provide the quietest performance in point to point or lightly loaded applications of all the families. The propagation delay derating for LVC162xxx is approximately 2.3ns per 100pF of additional loading.

Number of Outputs Switching

The number of outputs switching can affect the propagation delay of a component due to the switching currents in the package ground and V_{DD} leads. Components with lower drive levels will be less affected by this phenomena than higher drive level components. This phenomena primarily affects octal components due to the use of only one GND and one V_{DD} pin on the package. The net result of all bits switching in an octal component may be up to a few hundred pico seconds additional propagation delay. Double Density components with eight GNDs and four V_{DD} pins have multiple routes for current, plus a higher ratio of GND to output pins. The switching speed of double density components will not be significantly affected by multiple outputs switching, especially if the component is an ALVC162xxx or LVC162xxx device.

Output Enables

Figure 51 shows an example of how the enable times of the four families will vary with V_{DD} . The components shown are 16x244 type devices. The top line in the graph is LVC162244, followed by LVC16244, then ALVC162244, with ALVC16244 the lowest line. Disable times will be similarly affected. The graph again demonstrates that faster components with lower output impedances are less affected by V_{DD} than slower components with higher output impedances. Components other

than 16x244 will exhibit similar scaling with V_{DD} , but the curves will be higher or lower depending upon the inherent propagation delay of the selected component type.

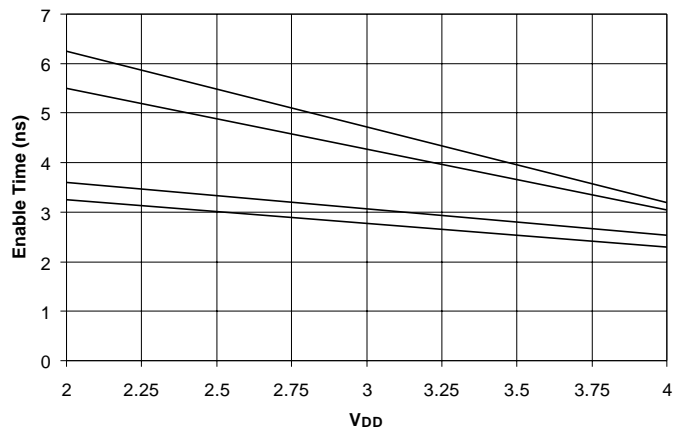
Figure 51, Enable Time vs. V_{DD}

Figure 52 shows a similar comparison between enable times and temperature of the four families. Again the components shown are 16x244 type devices with the top line in the graph being an LVC162244, followed by an LVC16244, then ALVC162244, with ALVC16244 the lowest line. Disable times will be similarly affected. Faster components with lower output impedances are less affected by temperature than slower components with higher output impedances. Components other than 16x244 can also be scaled depending upon the inherent propagation delay of the selected component type.

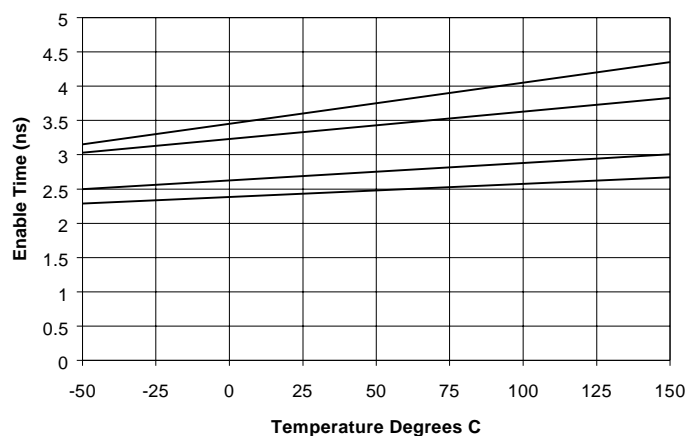


Figure 52, Enable Time vs. Temperature

Setup and Hold Times

In clocked components there is a point at which the data must be stable prior to the clock edge to guarantee that the data is clocked into the register on the clock edge. There is then an input hold time after the clock to guarantee that the clocking is complete and the changing input data will not be clocked into the register.

For most IDT ALVC and LVC registered and latched components, the toggle point where changing input data will be clocked into the register/latch is with the data preceding the clock by about 0.1ns ($T_{SU}=0.1ns$ and $T_H = -0.1ns$). The toggle point is device specific and will be affected (minimally) by V_{DD} , temperature and process variations, but in almost all cases will be within 0.3ns of the clock. Generally the data book specifications allow a conservative testing window around the toggle point of about 2.5ns (e.g. $T_{SU} = 1.9ns$, $T_H = 0.5ns$ for an ALVC16374). The primary reason for the large window is to guarantee specification compatibility with second source vendors of these components.

Skew

Skew reflects the worst case propagation delay difference between the different outputs. Skew results from design (routing/placement), process and packaging specific to the device.

Because of a lack of legitimate skew specifications, there is a tendency among designers to compute the difference between the maximum and minimum propagation delay specifications and use this number as the worst case skew. This is not a realistic measure of skew because the maximum (worst case) and minimum (best case) delays occur under mutually exclusive conditions of temperature, power supply voltage and process. In order to provide the user with the skew information, ALVC and LVC Double-Density devices have an output skew specification of 0.5ns maximum between outputs on the same device switching in the same direction. Part to part skew is not guaranteed on any devices except clock drivers, but if the user wishes to maintain low skew between parts, using components from the same date code and lot should guarantee low part to part skew. If operating under identical V_{DD} , temperature conditions, and loading, the user should be safe in assuming that two parts from the same lot will have a part to part skew of less than 1ns.

Metastability

Metastability is a state that may occur in clocked registers when the input data is transitioning through the input toggle point simultaneously with the clocking of the device. Theoretically, the indeterminate state is clocked into the device. Through the device, indeterminate states are reached and an indeterminate (middle voltage) state is driven to the output. This middle voltage state is held until the device can resolve whether it is going to drive HIGH or LOW. While theoretically it is possible for any component whether it is bipolar, BiCMOS or CMOS to exhibit metastability, the characteristic is pronounced only in very slow, low gain devices.

Because of the very high gain and high speed found in ALVC and LVC components, the high gain of the input translator will quickly resolve level issues prior to or during clocking. Internally the hysteresis circuit should drive any marginal state to a determinate condition. While theoretically, metastability can present itself in any clocked circuit, such characteristics should not be exhibited in the ALVC and LVC families.

Designers who are not familiar with the characteristics of metastability often confuse other conditions with the term metastability. Metastability is a highly transient effect that can rarely be caught on an oscilloscope except under tightly controlled conditions and long periods of sampling. If an output appears to be routinely/occasionally hanging at a mid state, the situation is not metastable. Other conditions that may exhibit an effect of this type include bus contention, a disconnected GND, a disconnected V_{DD} , an invalid GND reference in the test equipment, or the output is simply disabled.

Undershoot and Overshoot

Undershoot and overshoot on inputs or outputs can cause false switching, register upset, and device damage if the overshoot/undershoot is excessive. In addition, buses that interface memory devices will likely cause memory upset and data loss if undershoot is excessive.

When viewing undershoot and overshoot with an oscilloscope, be aware that adding a scope probe to a device output that is switching may cause an observable undershoot, due to the inductive kick of the device bond wire interacting with the capacitive load of the scope probe. Observations of undershoot and overshoot should be made using a high impedance scope probe.

The maximum limitation for undershoot and overshoot is the Absolute Maximum Rating specification for DC Output Current of -60 to 60 mA, given in all ALVC/LVC data sheets. As the voltage drops below the clamp diode voltage of about 0.7V, the current level will increase exponentially. The lead inductance of the component reacting with the pad capacitance will limit the current for very brief periods, allowing undershoot beyond the clamp voltage. The best way to determine whether an undershoot level or duration is damaging to a component is to use the package parameters found in the SPICE model, and modeling the undershoot to determine the current seen at the die.

As a very crude guideline under transient conditions, LVC and ALVC are expected to withstand an overshoot of $V_{DD} + 3.0V$ or an undershoot of -3V for 10ns regardless of clamp diodes. The LVC family should be able to tolerate an overshoot of up to 7 volts. While the parts should not sustain damage from these overshoots and undershoots, false switching may occur if there are device inputs sitting at marginal voltage levels or if other marginal conditions exist. In order to guarantee correct switching, undershoots and overshoots should be cleaned up as much as possible. Usually good line termination or selection of components with lighter drive levels (162xxx) will correct most problems.

EMI/RFI Problems

EMI and RFI problems are characteristic of very high speed components with fast edge rates that are driving long buses or transmission lines. When developing systems that must maintain low levels of EMI and RFI, reducing the drive level of the high speed components will reduce the noise radiation. In applications where radiated noise may be a problem, devices from the ALVC162xxx and LVC162xxx families will radiate less energy and cause less radiated noise than similar families with stronger output drivers. Some families that use BiCMOS drivers have output impedances as low as 2 ohm that may cause significant radiated noise.

POWER DISSIPATION

ALVC and LVC are true CMOS components that will dissipate no power if they are not toggling, the inputs are sitting at GND or V_{DD}, and no current is being pulled from the outputs.

If the ALVC or LVC components are toggling, the power dissipation can be calculated by using data in the POWER SUPPLY CHARACTERISTICS table of the respective data sheet. The equation for calculating power is found in Note 6 below the table in every data sheet.

The limiting factor in power dissipation is the component die temperature which should be held to less than 150°C to avoid metal migration and component damage. This temperature should be considered as a marginal condition with long term reliability requiring lower temperatures. While the devices can operate beyond 150°C the failure rate increases exponentially with increasing temperature (some manufacturers have selected 170°C as the cutoff).

Section 4 of the Logic Data Book contains thermal data for all logic packages used. Using the calculated power dissipation, the ambient temperature, and the thermal impedance from the data book, the operating die temperature can be calculated. Normally the impedance from junction to ambient is used to calculate die temperature under the intended power conditions. If a heat sink or airflow is used, the thermal impedance is significantly reduced, allowing a higher power dissipation level for a given temperature. The data book also includes specifications for the thermal impedance from the junction to the case. If an excellent cooling of the case is accomplished, the lower thermal resistance can be used in the calculation.

Figure 53 gives an example of what the maximum power dissipation would be in selected packages at 25°C and 70°C with no air flow and no heat sink.

Package	Description	θ_{ja}	θ_{jc}	PT	
				T _A = 25	T _A = 70
SSOP (PV)					
SO48-1	48-Pin SSOP	110	55	1.56W	1.00W
SO56-1	56-Pin SSOP	100	55	1.79W	1.14W
TSSOP (PA)					
SO48-2	48-Pin TSSOP	93	50	1.34W	0.86W
SO56-2	56-Pin TSSOP	84	50	1.49W	0.95W

Figure 53, Calculated Power for Selected Packages to Bring the Die Temperature to 150°C at 25°C and 70°C Ambient Temperatures

The power dissipation in high speed logic is broken into three separate identifiable sections. The first is component leakage current (I_{DD}) which is present whenever the component is powered. The second section is leakage current due to floating inputs (ΔI_{DD}). The third section is switching current which is obtained by multiplying the charge that is passed each time the device toggles (Q_d) by the frequency of switching (f). Note that Q_d is often incorrectly referred to as I_{ccd} in data sheets. In addition to these three, there is also power dissipation due to output loading which must be calculated by the system designer.

Power dissipation in an unloaded device is

$$PD(\text{unloaded}) = V_{DD} \times I_D$$

where I_D = Total power supply current

$$I_D = I_{DD} + \Delta I_{DD} \cdot D_H \cdot N_T + Q_d \times N_o \times f$$

where N_T = Number of TTL level inputs

D_H = Duty cycle of TTL level input

N_O = Number of switching bits

f = Switching Frequency

(1) I_{DD} - Static or quiescent power supply current, specified at V_{IN} = GND or V_{DD}.

(2) ΔI_{DD} - Power supply current through input translator for TTL level logic high inputs, specified at V_{IN} = V_{DD} - 0.6V.

(3) Q_d - Dynamic power supply current due to switching of internal circuitry and outputs. (Q_d = C_{pd} * V_{DD})

The total power supply current for unloaded conditions is the sum of these three components.

Leakage Currents (I_{DD})

IDT Logic has the lowest leakage currents in the industry with typical leakage levels lower than 1μA. This makes these components ideal for battery operation and other very low power applications.

Input Leakage (ΔI_{DD})

Looking at Figure 1, the input structure consists of a P-Channel and an N-Channel FET stacked on top of each other. When device inputs are held at levels other than V_{DD} or GND, both FETs will partially turn on allowing a leakage directly from V_{DD} to GND (crossover current). The amount of leakage for a typical device input is shown in Figure 54. In order to maintain low power dissipation, device inputs should always be held either HIGH or LOW at levels away from the areas of high leakage.

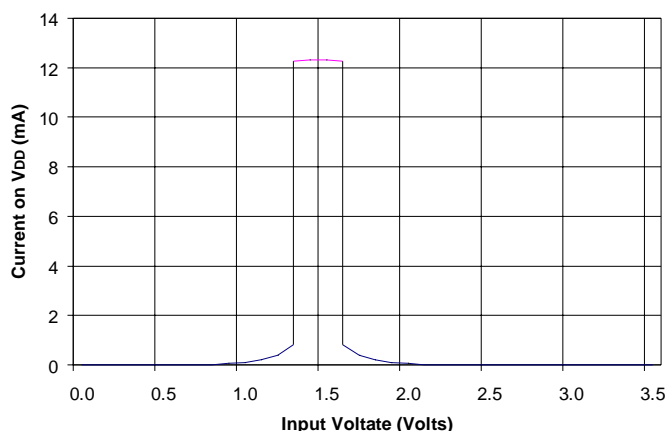


Figure 54, ΔI_{DD} vs. Input Voltage

Data sheets describe ΔI_{DD} as the current associated with TTL level inputs and specify ΔI_{DD} in mA per input. When calculating power dissipation, this parameter is multiplied by the duty cycle high and the number of inputs at a logic high to arrive at an average current over time that this parameter adds to the total current.

During switching, the input will pass through the threshold causing higher input crossover currents than at steady state, but these currents are part of the dynamic switching currents ($Q_d \times f$) and should not be added a second time as input leakage.

Dynamic Switching Current ($Q_d \times f$)

The last component is $Q_d \times f$, or the dynamic switching current (charge per cycle times the toggle frequency). This component of current represents the charging and discharging of the internal gate capacitance, crossover currents, and the charging and discharging of the device output drivers with no load. Q_d , which is specified in terms of $\mu A / MHz/bit$, is dependent upon the switching frequency and the number of bits switching.

For ALVC and LVC components, the Q_d is listed in the data sheet as C_{PD} . The conversion between C_{PD} and Q_d is as follows:

$$Q_d \text{ (in } \mu A / MHz/bit) = C_{PD} * V_{DD}$$

Many manufacturers do not specify switching current in any form, making accurate power calculations impossible with their components.

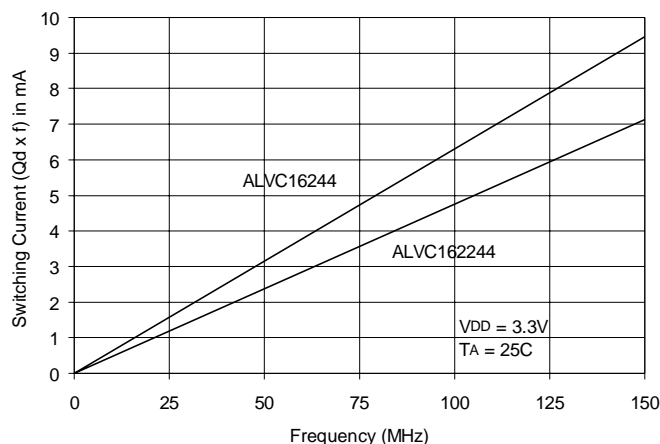


Figure 55, Switching Current vs. Frequency for ALVC

Figure 55 shows how switching frequency affects the current consumed by ALVC devices. The slope of the curve is Q_d . The currents shown are under unloaded conditions with one bit switching. The output drivers of a device are responsible for a large portion of the dynamic power dissipation. If a device is being switched with the output drivers disabled (3-state), Q_d will be significantly reduced.

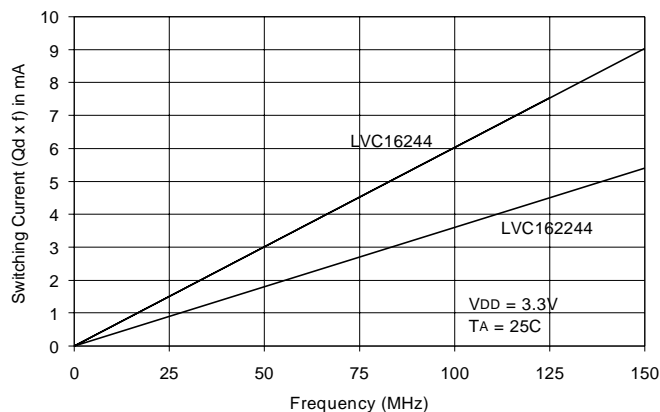


Figure 56, Switching Current vs. Frequency for LVC

Figure 56 is the equivalent of Figure 55 for LVC devices. The standard method of measuring switching current is by measuring I_d (current entering the V_{DD} pins) while toggling one input and one output only. To avoid driving a board pad capacitance or radiating energy from a loose pin, the switching output pin is cut off. All other inputs are tied to V_{DD} or GND.

Current Due to Loading

Adding loading to the output of a component will increase the current flowing into the power pin of the device. Most of this current will flow directly from the output into the load, causing power dissipation in the load. Any voltage drop between V_{DD} and V_{OH} or GND and V_{OL} will cause additional power dissipation within the component. This power dissipation is dependent upon the characteristics of the load.

If the load is strictly capacitive, the calculations are simplified. The current driven into a capacitive load can be calculated by the equation:

$$I = fC_LV$$

$$\text{Load Current} = \text{Frequency} * \text{Load Capacitance} * \text{Voltage}$$

To convert this to power, it can be multiplied times the toggle voltage ($= V_{DD}$ for CMOS rail swing) to obtain the power dissipation. This makes the equation:

$$PD = fC_LV^2$$

When calculating the dynamic power dissipation in a loaded device, the power dissipation capacitance C_{pd} and the load capacitance C_L can be added together. If the I_{DD} and the ΔI_{DD} are included in the equation, the total power dissipated in the device can be calculated as follows:

$$PD = V_{DD}(I_{DD} + \Delta I_{DD} * D_H * N_T + f * N_o * (C_{PD} + C_L) * V_{DD})$$

Figure 57 gives an example of how the current through the V_{DD} of the device will increase over frequency under a 50pF load with one pin switching. The power from the increased current will be dissipated partially in the driving component and partially in the load.

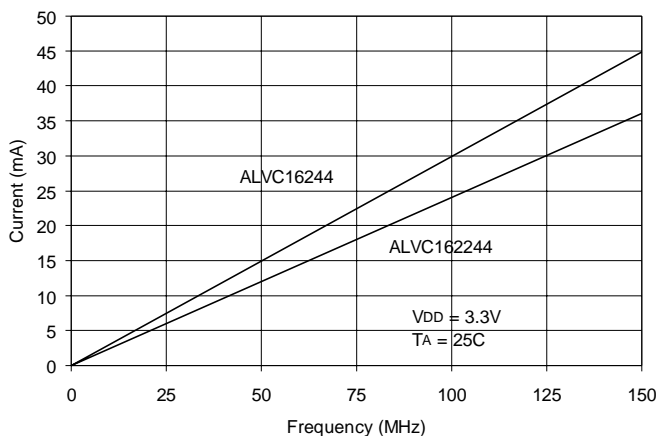


Figure 57, Supply Current under 50pF Load for ALVC

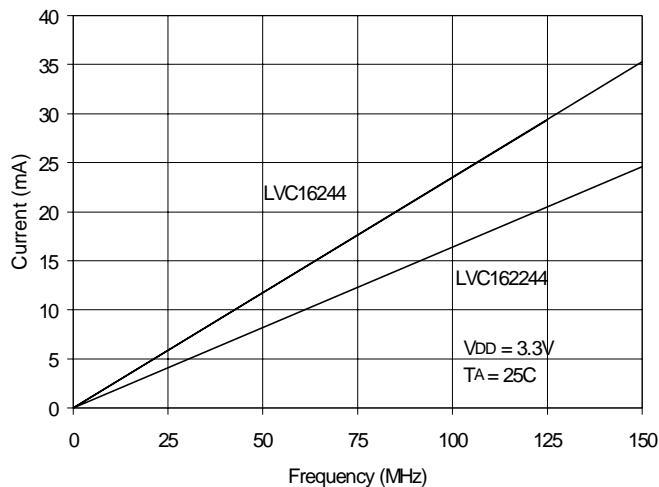


Figure 58, Supply Current under 50pF Load for LVC

Figure 58 is the equivalent of Figure 57 for the LVC family.

CONCLUSIONS

The ALVC and LVC logic families provide versatility and performance unequaled in the industry today. With choices of drive levels, bus-hold, overvoltage tolerance, high speed, and the ability to use the parts in 3.3V, 2.5V, or interfacing 5V systems, a component can be found to meet almost any need. The variety of output options allows these devices to be used in all applications from noise sensitive interfaces to loaded backplanes.

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01 Jan 2024)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.