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M16C/28, 29 Group

16-Bit PWM Output with SR Waveform Output Mode of Timer S

1. Abstract

This application note shows the PWM output of variable period and duty by using the waveform generation function of Timer S.

2. Introduction

This application note is applied to the following microcomputers:
MCU: M16C/28 Group
M16C/29 Group

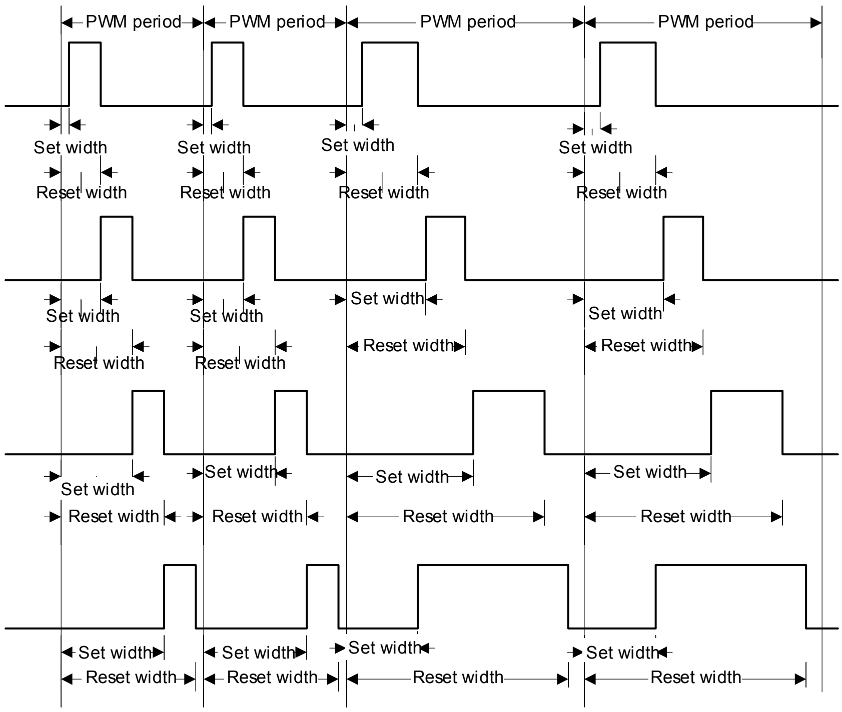
3. Detailed description

Timer S has one 16-bit base timer for free-run operation and eight 16-bit registers (channel 0 to 7) for the time measurement function and the waveform generation function.

In the SR waveform output mode, PWM period is set in the base timer reset register (G1BTRR register), the set width is set in the channel j (j=0,2,4,6), and the reset width is set in the channel k (k=1,3,5,7). PWM waveform is output from OUTC1j for the channel j.

PWM period and duty can change and the starting point of duty (set width) and the ending point (reset width) can be set as requested.

PWM Output Waveform



(1) PWM Period

The base timer is reset by matching the base timer reset register (G1BTRR Register) with the base timer. The formula of the PWM period is shown below.

$$\frac{1}{f_{BT1}} \times (n+2)$$

Where

fBT_1 is the count source frequency of the base timer.
'n' is a setting value for the base timer reset register.

(2) Set/Reset Width

The channel j is used in the SR waveform output mode. Set/reset width can be calculated by the following formula.

Set width: $\frac{1}{f_{BT1}} \times m$ Reset width: $\frac{1}{f_{BT1}} \times n$

Where

"m" is a setting value for the G1P0j register.
"n" is a setting value for the G1P0k register.

(3) PWM Period and Set/Reset Width Modification

The PWM period and set/reset width can be modified by rewriting the setting value in the G1BTRR, G1P0j and G1POk registers during the base timer interrupt process.

3.1 How to Set Up

This section shows setting procedures and setting values to execute “3.Detailed Description”. Refer to the hardware manual (M16C/28 Group or M16C/29 Group) for details of each register.

(1) Inhibiting an Interrupt
Set I flag=“0”. Or set interrupt priority level=“000₂” in interrupt control register that received interrupt requests issued by the timer S to be used.

(2) G1DV Register

b7 | 8 bits | b0

Set f_1/f_2 or dividing ratio of two-phase pulse input.

(3) G1BCR0 Register

b7							b0
0	0	0	0	0	1	1	1

- BCK1 to BCK0 Count source select bits
  f_1 or f_2
- RST4 Base timer reset cause select bit 4
  Base timer is reset by matching the G1BTRR register with the base timer.
- \- Not used. Must be set to “000_2”.
- CH7INSEL Channel 7 input select bit
  $P2_7$ to $INPC1_7$
- IT Base timer interrupt select bit
  Overflow of bit 15

(4) G1BCR1 Register

b7							b0
0	0	0	0	0	0	0	0

- \- Not used. Must be set to “0_2”.
- RST1 Base timer reset cause select bit 1
  Base timer is not reset by matching the G1PO0 register with the base timer.
- RST2 Base timer reset cause select bit 2
  Base time is not reset by input “L” to $\overline{INT1}$ pin.
- \- Not used. Must be set to “0_2”.
- BTS Base timer start bit
  Base timer reset
- UD1 to UD0 Up/down control bits
  Up-count mode
- \- Not used. Must be set to “0_2”.

(5) G1BTRR Register

b15 b0
16 bits

PWM period can be set.
When a setting value is n, the PWM period can be obtained from:

$$\frac{1}{f_{BT1}} \times (n+2)$$

(6) G1POCR0 to G1POCR7 Register

b7 b0
0 0 0 0 0 0 0 1

MOD1 to MOD0 Operation mode select bits
SR waveform output mode

\- Not used. Must be set to "00_2".

IVL Output initial value select bit
Output "0" as an initial value

RLD G1POCRj register value reload timing select bit
Reloaded when writing.

\- Not used. Must be set to "0_2".

INV Invert output function select bit
Output is not inverted

(7) G1PO0 to G1PO7 Register

b15 b0
16 bits

Set/reset width can be set.
"L" width time is defined by the following formula, where
"m" is a setting values.

$$\frac{1}{f_{BT1}} \times m$$

(8) G1FS Register

b7 b0
* * * * * * * *

FSC7 to FSC0 Channel 7 to 0 time measurement / Waveform Generation function select bits
Select waveform generation function.
(Note) It does not matter either "0" or "1" is set to other channels.

(9) G1IE0 Register

b7 b0
0 0 0 0 0 0 0 0

G1IE7 to G1IE0 Set the channels of the unused interrupt to "0".

(10) G1IR Register

b7							b0
0	0	0	0	0	0	0	0

G1IR7 to G1IR0 Interrupt request register is initialized.

(11) BTIC Register

b7							b0
0	0	0	0	0	*	*	*

ILVL2 to ILVL0 Interrupt priority level select bits
Interrupt priority level can be selected.

IR Interrupt request bit
Set to “no interrupt request” .

- Not used. Must be set to “0000$_2$”.

(12) G1FE Register

b7							b0
*	*	*	*	*	*	*	*

IFE7 to IFE0 Channel 7 to 0 function enable bits
Set the using channel bit to “1” (channel function enable)
(Note) Set to “0” if channel is not used.

3.2 Precaution on Interrupt

In the process of Timer S interrupt, the description varies depending on the interrupt routine by the base timer or by each channel.
In the case of the base timer interrupt, interrupt request bit is “0” when the request is accepted. (It is not necessary to set to “0” by the program.)

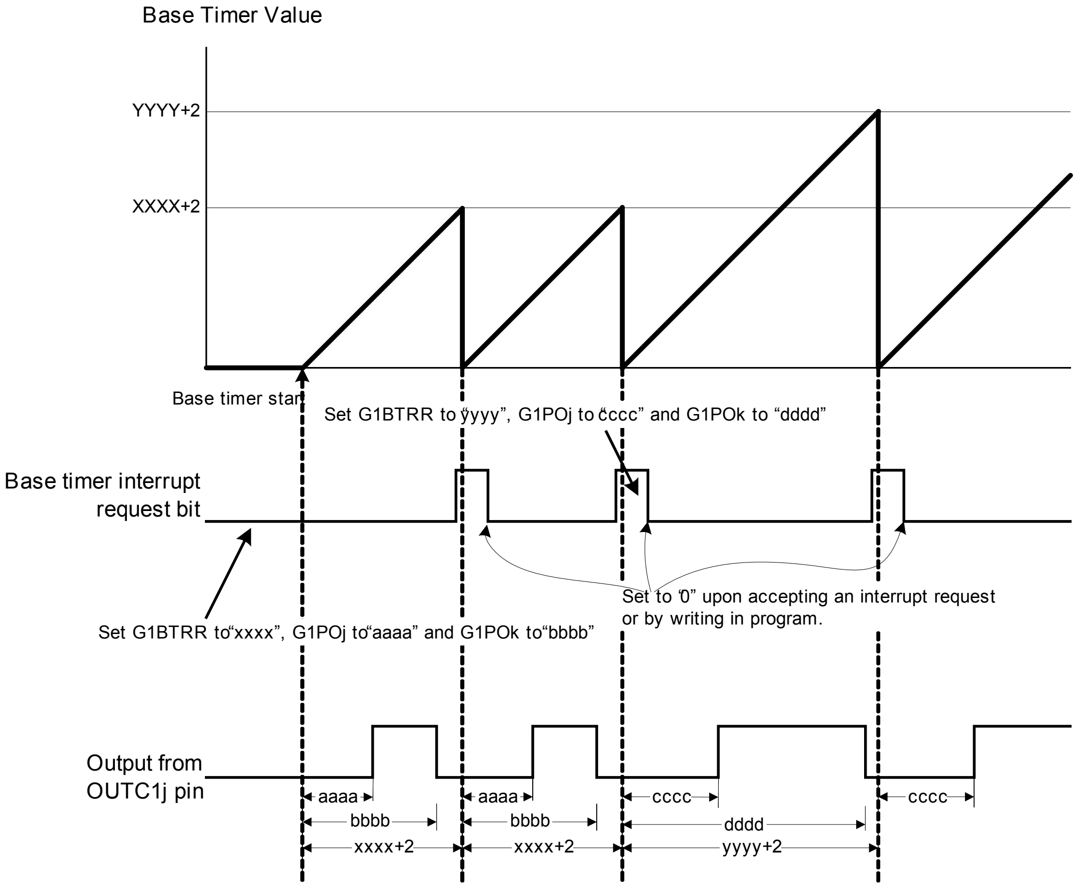
In the case of interrupt by each channel, interrupt requests for each channel are set in the interrupt request register (G1IR Register). When an interrupt request in the channel i occurs, the bit i in the G1IR Register is set to “1”.
If the bit i in the interrupt enable register 0 (G1IE0 Register) is “1”, the interrupt request bit in the IC/OC0 interrupt control register (ICOC0IC Register) is set to “1”.
If the bit i in the G1IE1 register is “1”, the interrupt request bit in the IC/OC1 interrupt control register (ICOC1IC Register) is set to “1”.

Interrupt request bits in the IC/OC0 and IC/OC1 interrupt control register are set to “0” automatically when they receive the interrupt request. However the interrupt request bits of each channel in the G1IR register are not set to “0” automatically, so set to “0” (no interrupt request) by the program.

Use the following instructions when writing “0” to each bit in the G1IR register.
AND, BCLR

3.3 Timing Diagram

The following diagram shows PMW output according to the section “3.1” and “3.2”.



4. Sample Program

```
/****************************************************************
 *                                                              *
 *   FILE NAME :                                                *
 *   Version   : 1.10                                           *
 *   Function  : 16-bit PWM by S-R Waveform output mode         *
 *                                                              *
 *   Copyright (C)2004, Renesas Technology Corp.                *
 *   Copyright (C)2004, Renesas Solutions Corp.                 *
 *                                                              *
 ****************************************************************/
/****************************
 *   include file          *
 ****************************/
#include "sfr28.h"

/****************************
 *   Function Definition    *
 ****************************/
void    bt_int(void);
#pragma INTERRUPT bt_int

void    port_init(void);
void    icoc_init(void);
/****************************
 *   main                  *
 ****************************/
void main(void) {

        port_init();
        icoc_init();

        bts_g1bcr1 = 1;             /* Base Timer Start */
        asm (" fset I");
        while (1) {
        }
}

void port_init() {
        p0 = 0;
        p1 = 0;
        p2 = 0;
        p3 = 0;

        p7 = 0;
        p8 = 0;
        p9 = 0;
        p10 = 0;

        pd0 = 0xff;
        pd1 = 0xff;
        pd2 = 0x00;
        pd3 = 0xff;

        pd7 = 0xff;
        pd8 = 0xff;
        prcr = 4;
        pd9 = 0xff;
        pd10 = 0xff;

        ifsr2a = 1;
}

void icoc_init() {

        g1dv = 20-1;                /* fBT is 1MHz */
        g1bcr0 = 0x07;
        g1bcr1 = 0x00;              /* The base timer is reset by matching the G1PO0 regiser */
```

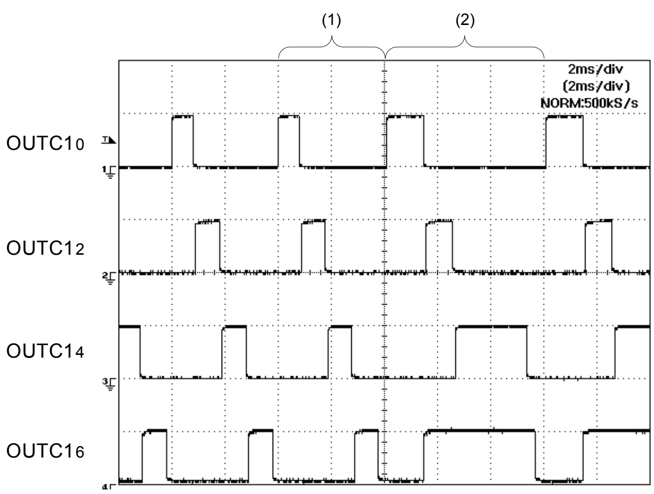
```
        g1btrr = 4000-2;

        g1pocr0 = 0x01;            /* ch-0 Set/Reset waveform output mode */
        g1pocr2 = 0x01;            /* ch-2 Set/Reset waveform output mode */
        g1pocr4 = 0x01;            /* ch-4 Set/Reset waveform output mode */
        g1pocr6 = 0x01;            /* ch-6 Set/Reset waveform output mode */
        g1po0 = 100;
        g1po1 = 900;
        g1po2 = 1000;
        g1po3 = 1900;
        g1po4 = 2000;
        g1po5 = 2900;
        g1po6 = 3000;
        g1po7 = 3900;

        g1fs = 0x00;               /* ch-0 to ch-7 Waveform generation function select */

        g1ie0 = 0x00;              /* Interrupt enable register 0 set */

        g1ir = 0;                  /* Interrupt request register initialize */

        btic = 0x04;               /* IC/OC 0 Interrupt control register set */

        g1fe = 0xFF;               /* ch-0 to ch-7 function enable */
}

void    bt_int() {

        p1++;
        if (p1==5) {
                g1btrr = 6000-2;
                g1po0 = 200;
                g1po1 = 1600;
                g1po2 = 1700;
                g1po3 = 2700;
                g1po4 = 2800;
                g1po5 = 5500;
                g1po6 = 1600;
                g1po7 = 5800;
                p10_7 = 1;
        }
        if (p1==10) {
                g1btrr = 4000-2;
                g1po0 = 100;
                g1po1 = 900;
                g1po2 = 1000;
                g1po3 = 1900;
                g1po4 = 2000;
                g1po5 = 2900;
                g1po6 = 3000;
                g1po7 = 3900;
                p1=0;
                p10_7 = 0;
        }
}
```

5. Example of PWM Output

The following shows examples of the PWM output from OUTC1$_0$(P2$_0$), OUTC1$_2$(P2$_2$), OUTC1$_4$(P2$_4$) and OUTC1$_6$(P2$_6$) when the Timer S is used.

Conditions: Supply voltage = 5V
Main clock = 20MHz
Base timer operation clock (f_{BT1}) = 1MHz

Item	Register	(1) in the following figure	(2) in the following figure
PWM period	G1BTRR	Setting value n = 3998 1 µs x (3998+2) = 4.00ms	Setting value n = 5998 1 µs x (5998+2) = 6.00ms
Set width of OUTC1$_0$ (P2$_0$) output	G1P00	Setting value m = 100 1 µs x 100 = 0.10ms	Setting value m = 200 1 µs x 200 = 0.20ms
Reset width of OUTC1$_0$ (P2$_0$) output	G1P01	Setting value m = 900 1 µs x 900 = 0.90ms	Setting value m = 1600 1 µs x 1600 = 1.60ms
Set width of OUTC1$_2$ (P2$_2$) output	G1P02	Setting value m = 1000 1 µs x 1000 = 1.00ms	Setting value m = 1700 1 µs x 1700 = 1.70ms
Reset width of OUTC1$_2$ (P2$_2$) output	G1P03	Setting value m = 1900 1 µs x 1900 = 1.90ms	Setting value m = 2700 1 µs x 2700 = 2.70ms
Set width of OUTC1$_4$ (P2$_4$) output	G1P04	Setting value m = 2000 1 µs x 2000 = 2.00ms	Setting value m = 2800 1 µs x 2800 = 2.80ms
Reset width of OUTC1$_4$ (P2$_4$) output	G1P05	Setting value m = 2900 1 µs x 2900 = 2.90ms	Setting value m = 5500 1 µs x 5500 = 5.50ms
Set width of OUTC1$_6$ (P2$_6$) output	G1P06	Setting value m = 3000 1 µs x 3000 = 3.00ms	Setting value m = 1600 1 µs x 1600 =1.60ms
Reset width of OUTC1$_6$ (P2$_6$) output	G1P07	Setting value m = 3900 1 µs x 3900 = 3.90ms	Setting value m = 5800 1 µs x 5800 = 5.80ms



6. Reference

Hardware Manual

M16C/28 Group Hardware Manual

M16C/29 Group Hardware Manual

(The latest version is available on the website: http://www.renesas.com)

7. Website and Contact for Support

Renesas Website

http://www.renesas.com/

For technical information related to M16C family

E-mail: support_apl@renesas.com

REVISION HISTORY

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1.00	2004.09.23	-	First edition issued
1.00	2004.11.30	3, 4, 6, 7	How to set up revised

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