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M16C/28, 29 Group

16-Bit PWM Output with the Single-phase Waveform Output Mode of Timer S

1. Abstract

This application note shows the PWM output of variable period and duty by using the waveform generation function of Timer S.

2. Introduction

This application note is applied to the following microcomputers:

MCU: M16C/28 Group

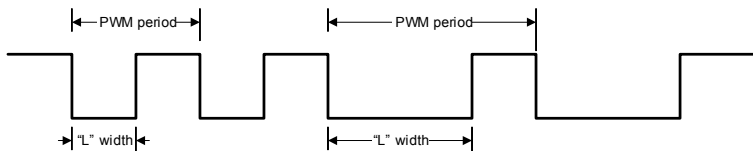
M16C/29 Group

3. Detailed description

Timer S has one 16-bit base timer for free-run operation and eight 16-bit registers (channel 0 to 7) for the time measurement function and the waveform generation function.

In this example, PWM period is set in the base timer reset register, and "L" width is set in the channel j (j=0 to 7). And PWM waveform is output from the OUTC1j pin for channel j.

PWM Output Waveform



(1) PWM Period

The base timer is reset by matching the base timer reset register (G1BTRR Register) with the base timer. The formula of the PWM period is shown below.

$$\text{PWM period: } \frac{1}{f_{BT1}} \times (n+2)$$

Where

f_{BT1} is the count source frequency of the base timer.

'n' is a setting value for the G1BTRR register.

(2) "L" Width

The channel j is used in the single-phase waveform output mode of the waveform generation function. "L" width can be calculated by the following formula.

$$\text{"L" width: } \frac{1}{f_{BT1}} \times m$$

Where

"m" is a setting value for the G1P0j register.

INV bit in the G1P0CRj register is "0" (output is not inverted).

(3) PWM Period and "L" Width Modification

The PWM period and "L" width can be modified by rewriting the G1BTRR and G1P0j registers during the base timer interrupt process.

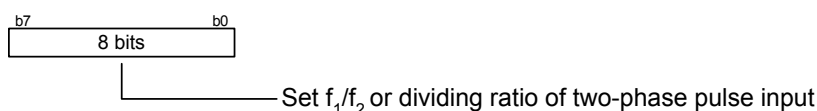
3.1 How to Set Up

This section shows setting procedures and values to execute "3.Detailed Description". Refer to the hardware manual (M16C/28 Group or M16C/29 Group) for details of each register.

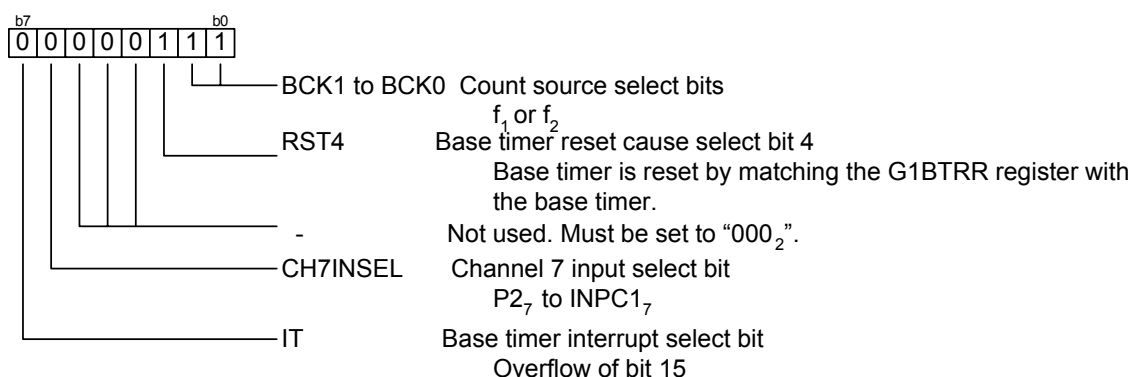
(1) Inhibiting an Interrupt

Set I flag="0". Or set interrupt priority level="0002" in interrupt control register that received interrupt requests issued by the timer S to be used.

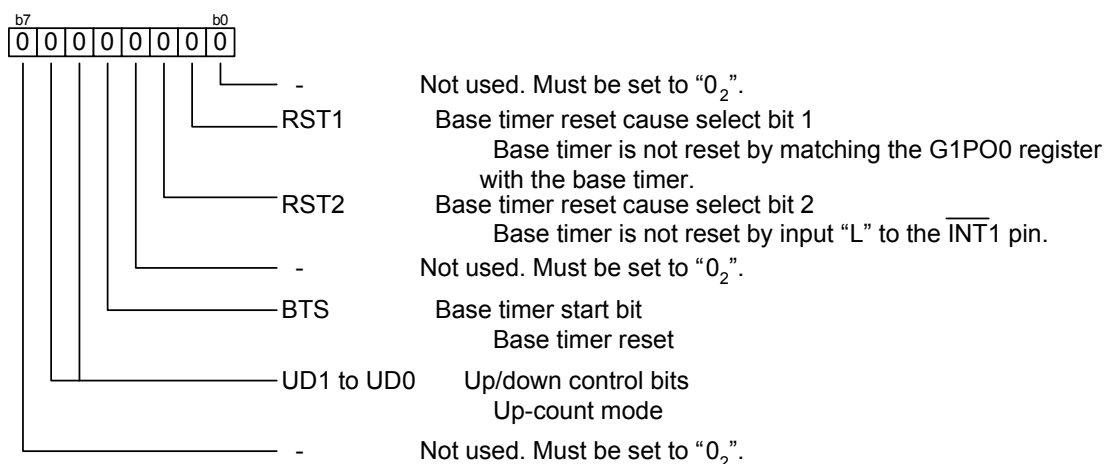
(2) G1DV register



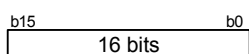
(3) G1BCR0 register



(4) G1BCR1 register



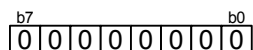
(5) G1BTRR register



PWM period can be set.
When a setting value is n , the PWM period can be obtained from

$$\frac{1}{f_{BT1}} \times (n+2)$$

(6) G1POCR0 to G1POCR7 register



MOD1 to MOD0 Operation mode select bits
Single-phase waveform output mode

- Not used. Must be set to "00₂".

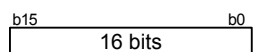
IVL Output initial value select bit
Output "0" as an initial value

RLD Register reload timing select bit
Reloaded when writing

- Not used. Must be set to "0₂".

INV Invert output function select bit
Output is not inverted

(7) G1PO0 to G1PO7 register



"L" width can be set.
"L" width time is defined by the following formula, where
"m" is a setting value of G1PO register.

$$\frac{1}{f_{BT1}} \times m$$

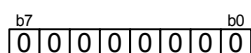
(8) G1FS register



FSC7 to FSC0 Channel 7 to 0 time measurement/ waveform generation function select bits

Select waveform generation function
(Note) It does not matter either "0" or "1" is set to other channels.

(9) G1IE0 register

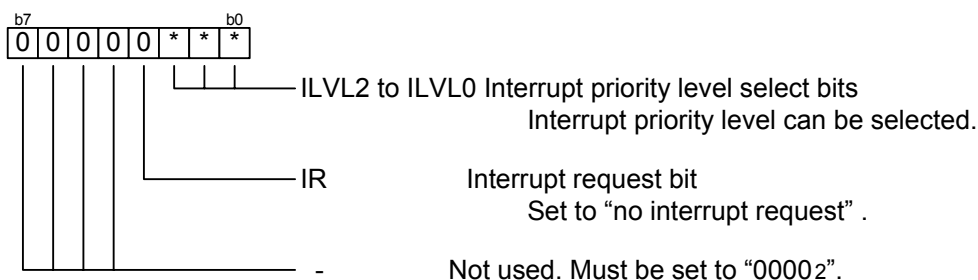


G1IE7 to G1IE0 Set the channels of unused interrupt to "0".

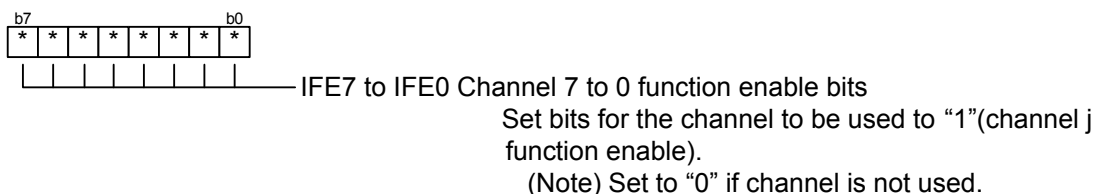
(10) G1IR register



(11) BTIC register



(12) G1FE register



3.2 Precaution on Interrupt

In the process of Timer S interrupt, the description varies depending on the interrupt routine by the base timer or by each channel.

In the case of the base timer interrupt, interrupt request bit is "0" when the request is accepted. (It is not necessary to set to "0" by the program.)

In the case of interrupt by each channel, interrupt requests for each channel are set in the interrupt request register (G1IR Register). When an interrupt request in the channel i occurs, the bit i in the G1IR Register is set to "1".

If the bit i in the interrupt enable register 0 (G1IE0 Register) is "1", the interrupt request bit in the IC/OC0 interrupt control register (ICOC0IC Register) is set to "1".

If the bit i in the G1IE1 register is "1", the interrupt request bit in the IC/OC1 interrupt control register (ICOC1IC Register) is set to "1".

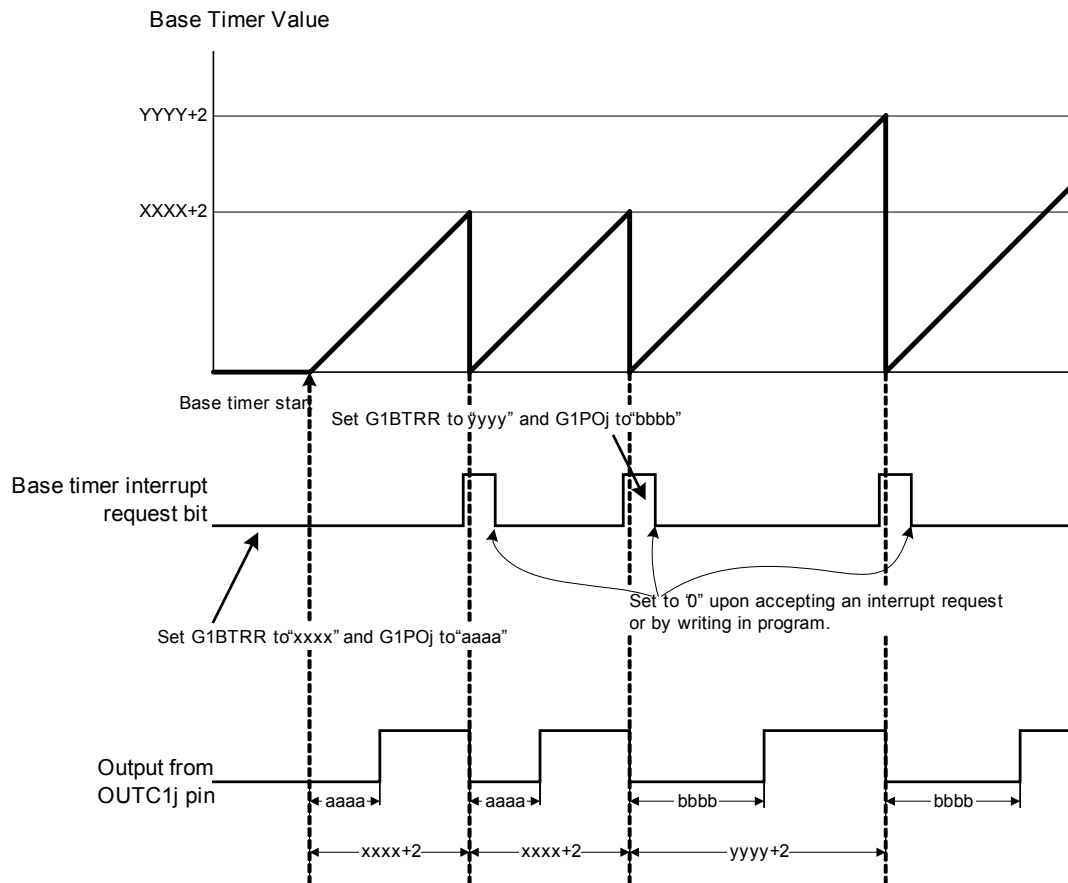
Interrupt request bits in the IC/OC0 and IC/OC1 interrupt control register are set to "0" automatically when they receive the interrupt request. However the interrupt request bits of each channel in the G1IR register are not set to "0" automatically, so set to "0" (no interrupt request) by the program.

Use the following instructions when writing "0" to each bit in the G1IR register.

AND, BCLR

3.3 Timing Diagram

The following diagram shows PMW output according to the section “3.1” and “3.2”.



4. Sample Program

```

/*****
 *
 * FILE NAME :
 * Version : 1.10
 * Function : 16-bit PWM
 *
 * Copyright (C)2004, Renesas Technology Corp.
 * Copyright (C)2004, Renesas Solutions Corp.
 *
 *****/
/*****
 * include file
 *****/
#include "sfr28.h"

/*****
 * Function Definition
 *****/
void bt_int(void);
#pragma INTERRUPT bt_int

void port_init(void);
void icoc_init(void);
/*****
 * main
 *****/
void main(void) {

    port_init();
    icoc_init();

    bts_glbcr1 = 1;          /* Base Timer Start */
    asm ("fset I");
    while (1) {
    }

void port_init() {
    p0 = 0;
    p1 = 0;
    p2 = 0;
    p3 = 0;

    p7 = 0;
    p8 = 0;
    p9 = 0;
    p10 = 0;

    pd0 = 0xff;
    pd1 = 0xff;
    pd2 = 0x00;
    pd3 = 0xff;

    pd7 = 0xff;
    pd8 = 0xff;
    prcr = 4;
    pd9 = 0xff;
    pd10 = 0xff;

    ifsr2a = 1;
}

void icoc_init() {

    glbv = 20-1;          /* fBT is 1MHz */
    glbcr0 = 0x07;

```

```

    glbcr1 = 0x00;          /* The base timer is reset by matching the G1P00 regiser */

    glbtrr = 4000-2;

    glpocr0 = 0x00;        /* ch-0 Single waveform output mode */
    glpo0 = 3500;

    glpocr1 = 0x00;        /* ch-1 Single waveform output mode */
    glpo1 = 500;

    glpocr4 = 0x00;        /* ch-4 Single waveform output mode */
    glpo4 = 2000;

    glpocr5 = 0x00;        /* ch-5 Single waveform output mode */
    glpo5 = 3000;

    glfs = 0x00;          /* ch-0,7 Waveform generation function select */

    glie0 = 0x00;          /* Interrupt enable register 0 set */

    glir = 0;              /* Interrupt request register initialize */

    btic = 0x04;           /* IC/OC 0 Interrupt control register set */

    glfe = 0x33;           /* ch-0,ch-4 function enable */
}

void bt_int() {
    p1++;
    if (p1==5) {
        glbtrr = 6000-2;
        glpo0 = 4000;
        glpo1 = 1000;
        glpo4 = 4000;
        glpo5 = 5500;
        p10_7 = 1;
    }
    if (p1==10) {
        glbtrr = 4000-2;
        glpo0 = 3500;
        glpo1 = 500;
        glpo4 = 2000;
        glpo5 = 3000;
        p1=0;
        p10_7 = 0;
    }
}

```

5. Example of PWM Output

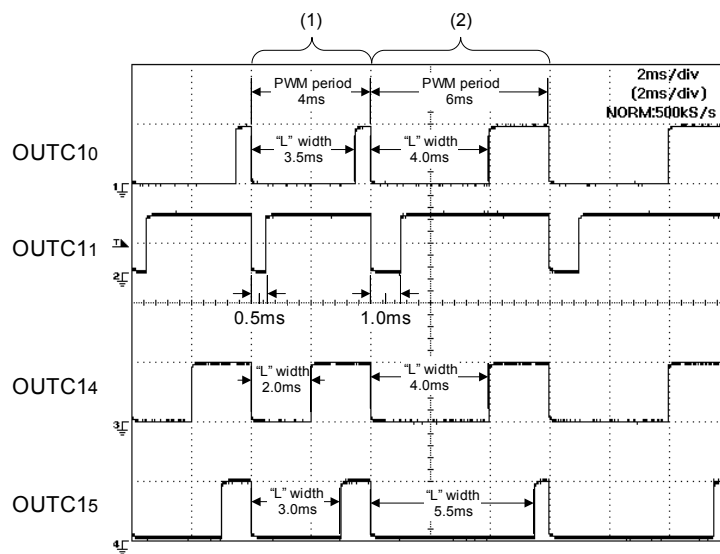
The following shows examples of the PWM output from OUTC1₀(P2₀), OUTC1₁(P2₁), OUTC1₄(P2₄) and OUTC1₅(P2₅) when the Timer S is used.

Conditions: Supply voltage = 5V

Main clock = 20MHz

Base timer operation clock (f_{BT1}) = 1MHz

Item	Register	(1) in the following figure	(2) in the following figure
PWM period	G1BTRR	Setting value n = 3998 $1\mu s \times (3998+2) = 4.00ms$	Setting value n = 5998 $1\mu s \times (5998+2) = 6.00ms$
"L" width of OUTC1 ₀ (P2 ₀) output	G1P00	Setting value m = 3500 $1\mu s \times 3500 = 3.50ms$	Setting value m = 4000 $1\mu s \times 4000 = 4.00ms$
"L" width of OUTC1 ₁ (P2 ₁) output	G1P01	Setting value m = 500 $1\mu s \times 500 = 0.50ms$	Setting value m = 1000 $1\mu s \times 1000 = 1.00ms$
"L" width of OUTC1 ₄ (P2 ₄) output	G1P04	Setting value m = 2000 $1\mu s \times 2000 = 2.00ms$	Setting value m = 4000 $1\mu s \times 4000 = 4.00ms$
"L" width of OUTC1 ₅ (P2 ₅) output	G1P05	Setting value m = 3000 $1\mu s \times 3000 = 3.00ms$	Setting value m = 5500 $1\mu s \times 5500 = 5.50ms$



6. Reference

Hardware Manual

M16C/28 Group Hardware Manual

M16C/29 Group Hardware Manual

(The latest version is available on the website: <http://www.renesas.com>)

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For technical information related to M16C family

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REVISION HISTORY

Rev.	Date	Description	
		Page	Summary
1.00	2004.09.23	-	First edition issued
1.10	2004.11.30	3,4,6,7	How to set up revised

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