Renesas RA Family

16-Bit A/D Converter Performance for RA2A1

Introduction

This application note describes the performance and calibration functions of the 16-bit A/D converter integrated into the RA2A1.

Target Device

RA2A1 MCU Group

Conditions

Unless otherwise specified, typical data are based on VCC = AVCC0 = AVCC1 = VREFH0 = 3.3 V, VSS = AVSS0 = AVSS1 = VREFL0 = 0 V, Ta = 25 °C

Contents

1. Overview

A 16-bit A/D converter with digital calibration function is built into the RA2A1 MCU Group. The input mode can be selected as differential input mode or single-ended input mode. Digital calibration allows high-precision A/D conversion by calculating the offset error correction value and gain error correction value under the conditions of use.

This application note explains the 16-bit A/D converter timing parameters, linear characteristics, dynamic characteristics, A/D conversion current consumption, and how to perform calibration.

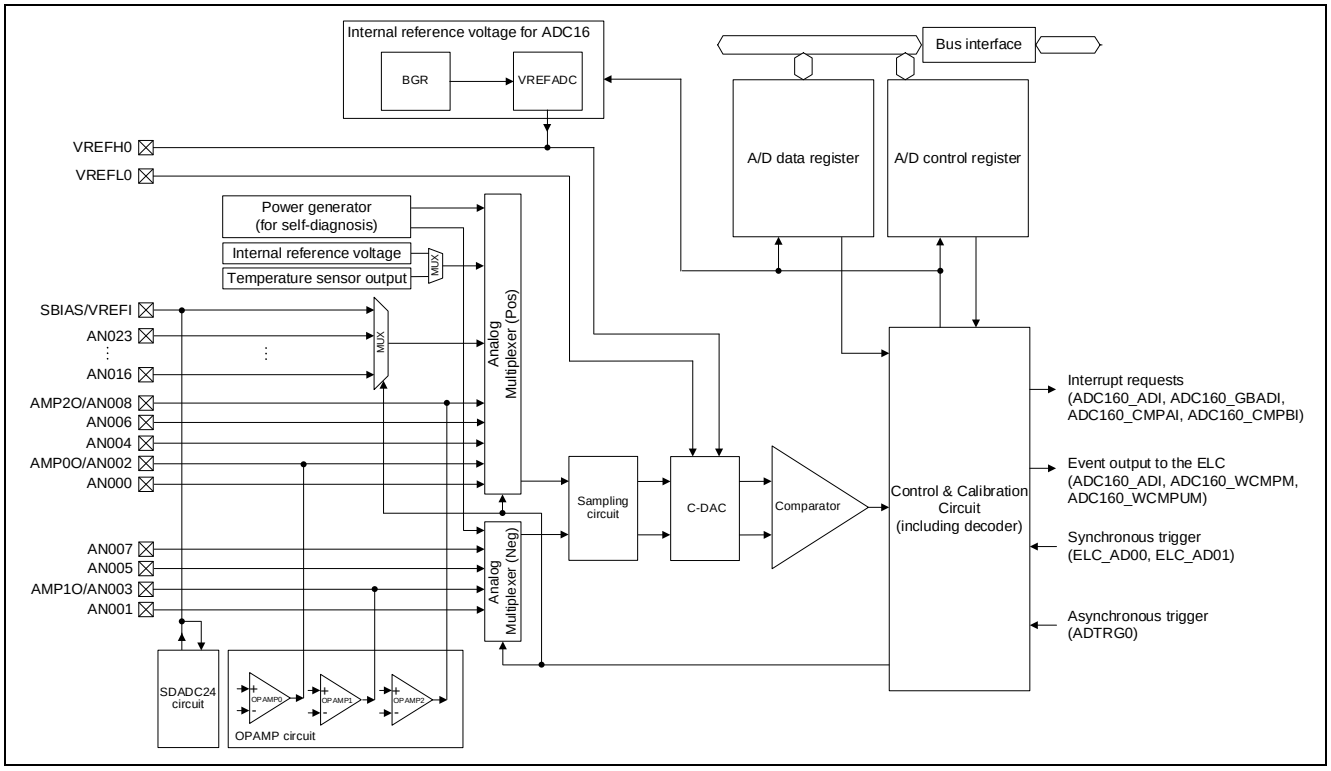

Figure 1. ADC16 Block Diagram

Table 1 ADC16 I/O Pins

Pin name	I/O	Function
AVCC0	Input	Analog block power supply pin
AVSS0	Input	Analog block power supply ground pin
VREFH0	Input*1	Reference power supply pin
	Output*2	VREFADC output voltage
VREFL0	Input	Reference power supply ground pin
AN000 to AN008, AN016 to AN023	Input	Analog input pins 00 to 08, 16 to 23
ADTRG0	Input	External trigger input pin for starting A/D conversion
SBIAS/VREFI	I/O	Power supply pin for sensor or external VREF input pin for the SDADC24

Notes:

1. When VREFH0 is used to supply the high potential reference voltage.
2. When VREFADC is used to supply the high potential reference voltage.

2. Utilizing Data Sheet Parametric Values

This section describes the electrical characteristics of the 16-bit A/D converter.

2.1 Analog Input Parameters

The 16-bit A/D converter has the following features:

- Analog input voltage is up to VREFH0 at VREFH0 ≤ 5.5 V.
- Analog input common voltage range (Acm) in differential input mode is from VREFL0 to VREFH0.

Examples of input analog signal are shown in Figure 2.

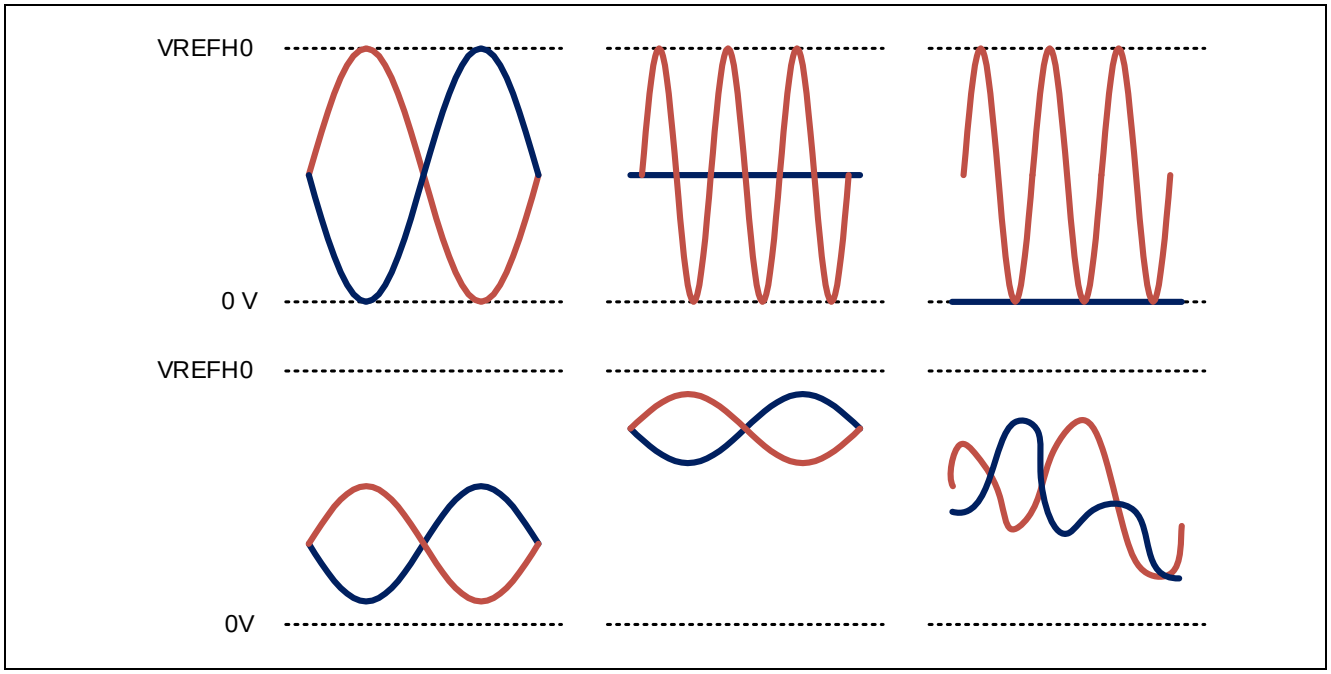

Figure 2. Examples of Input Analog Signal in Differential Input Mode

2.2 Timing Parameters

Table 2 shows the timing parameters of the 16-bit A/D converter.

Table 2. 16-bit A/D Conversion, Timing Parameters

Conditions: VCC = AVCC0 = AVCC1 = 1.7 to 5.5 V, VREFH0 = 1.7 to 5.5 V, VSS = AVSS0 = AVSS1 = VREFL0 = 0 V, Reference voltage range applied to the VREFH0 and VREFL0.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Frequency	ADCLK*2	1	-	32	MHz	3.0 V ≤ AVCC0 ≤ 5.5 V, 3.0 V ≤ VREFH0
		1	-	24		2.7 V ≤ AVCC0 ≤ 5.5 V, 2.7 V ≤ VREFH0
		1	-	16		2.4 ≤ AVCC0 ≤ 5.5 V, 1.5 V ≤ VREFH0
		1	-	8		1.8 V ≤ AVCC0 ≤ 5.5 V, 1.5 V ≤ VREFH0
		1	-	4		1.7 V ≤ AVCC0 ≤ 5.5 V, 1.5 V ≤ VREFH0
Conversion rate	Fs	-	-	$1/(t_{SPL}+18/ADCLK)$	S/s	-
Sampling time*1	t_{SPL}	0.25	-	-	µs	High-precision channel, 2.7 V ≤ AVCC0 ≤ 5.5 V

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
		3	-	-		High-precision channel, 1.7 V ≤ AVCC0 < 2.7 V
		3	-	-		Normal-precision channel, 2.7 V ≤ AVCC0 ≤ 5.5 V
		10	-	-		Normal-precision channel, 1.7 V ≤ AVCC0 < 2.7 V
Settling time	t_{START}	-	-	1	µs	2.7 V ≤ AVCC0 ≤ 5.5 V
		-	-	3.2		1.8 V ≤ AVCC0 < 2.7 V
		-	-	8.9		1.7 V ≤ AVCC0 < 1.8 V

Notes: 1. Permissible signal source impedance Max = 0.5 kΩ.
2. The ADCLK clock is identical to the PCLKD clock. It must not exceed 32 MHz for the proper operation of ADC16. Since ICLK (CPU Clock) and PCLKD share the same clock source, getting the maximum ADC16 conversion rate requires that the CPU also runs at 32 MHz. Additionally, in this scenario, the UCLK (the USB clock) does not meet the required 48 MHz and so this interface cannot be used. If the users require running the CPU at its maximum clock rate or utilizing the USB interface, then the PCLKD must be set to 24 MHz, affecting the ADC16 conversion time accordingly.

The conversion rate (Fs) consists of input sampling time (t_{SPL}) and time for conversion by successive approximation (t_{SAM}). The A/D conversion processing time (output rate of the conversion result) is the sum of the conversion rate and the gain correction time. However, because gain correction occurs concurrently with sampling, the gain correction time affects the A/D conversion processing time only in the first cycle of single scan, continuous scan, and group scan. Gain correction time (t_{GAIN}) does not affect the second and later cycles. The t_{SPL} is used to charge sample-and-hold circuits in the A/D converter. Minimum t_{SPL} is defined only at signal source impedance 0.5 kΩ in Table 2.

If the sampling time is not sufficient due to the high impedance of an analog input signal source, the sampling time can be increased by adjusting the ADSSTRn register. Similarly, if the A/D conversion clock (ADCLK) is slow, sampling time can be adjusted by decreasing value in the ADSSTRn register.

The t_{SAM} is 18 ADCLK states and the t_{GAIN} is 10 ADCLK states.

Settling time is the wait time required from the time of releasing the module-stop state until A/D conversion is started. If you want to wait for settling time by hardware, set the value obtained by adding the sampling time and settling time to the ADSSTR register.

Figure 3 shows an example of operation of the A/D converter when AN004 to AN006 are selected in single scan mode.

1. Wait for settling time to start A/D conversion after release from the module-stop state. If you want to wait for settling time by hardware, set the value obtained by adding the sampling time and settling time to the ADSSTR register.
2. When the ADST bit in ADCSR register is set to 1 (A/D conversion start) by a software trigger, a synchronous trigger input (ELC), or an asynchronous trigger input, A/D conversion is performed on the ANn channels selected in the ADANSA0 and ADANSA1 registers, starting from the channel with the smallest number n.
3. The A/D converter samples the analog input for the time set by ADSSTRn register, and conversion by successive approximation. Then, gain correction is performed.
4. Each time A/D conversion and the gain correction is complete, the A/D conversion result is stored in the associated A/D Data Register y (ADDRy). The same storing operation is also performed in continuous scan mode and group scan mode. Gain correction occurs concurrently with sampling, and the gain correction time affects the A/D conversion processing time only in the first cycle of single scan, continuous scan, and group scan. Gain correction time (t_{GAIN}) does not affect the second and later cycles.
5. When A/D conversion and the gain correction of all the selected channels completes, an ADC160_ADI interrupt request is generated.
6. The ADST bit remains 1 (A/D conversion start) during A/D conversion, and is automatically set to 0 when A/D conversion and the gain correction of all the selected channels completes. The ADC16 then enters a wait state.

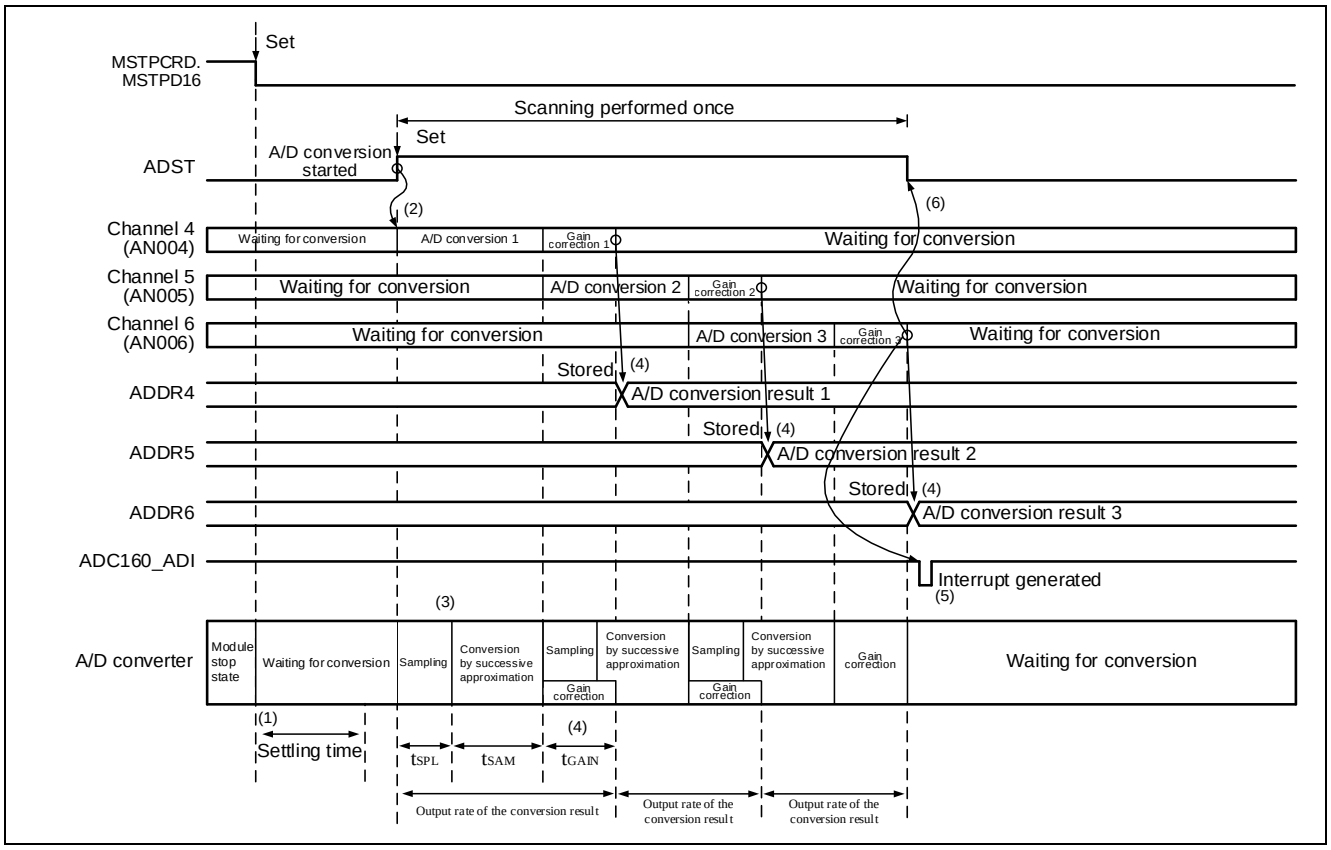

Figure 3. A/D Converter Operation Example When AN004 to AN006 are Selected in Single Scan Mode

2.3 Linearity Parameters

INL, DNL, offset error, and gain error are used as representative indicators for accuracy and error of the A/D converter.

INL: Integral non-linearity (LSB)
The maximum deviation between the ideal line and the actual output code when the measured offset and full-scale errors are zeroed.

DNL: Differential nonlinearity (LSB)
The difference between 1 LSB width based on the ideal A/D conversion characteristics and the width of the actual output code.

Offset error (LSB)
The difference between the transition point of the ideal 0x0000h output code and the actual 0x0000h output code.

Gain error (LSB)
The difference between the transition point of the ideal 0x7FFFh (or 0x8000h) output code and the actual 0x7FFFh (or 0x8000h) output code.

The definitions of an LSB are shown in Equation 1 and 2, and the output range of A/D conversion result is shown in Table 3.

Single-ended Input Mode

$$\text{Equation 1:}\quad 1\text{LSB} = \frac{(\text{VREFH0} - \text{VREFHL0})}{2^{15}}$$

Differential Input Mode

$$\text{Equation 2:}\quad 1\text{LSB} = \frac{2 \times (\text{VREFH0} - \text{VREFHL0})}{2^{16}}$$

For example, 1 LSB is 100.7 μV at VREFH0 = 3.3 V and VREFL0 = 0 V in differential input mode.

Table 3. A/D Conversion Result Output Ranges

Input Mode	A/D conversion	ADCER.ADINV (Data Inversion)	Output Range
Single-end Input Mode	Temperature sensor	x	0 to $2^{15} - 1$
	Internal reference voltage		
	AN008, AN016 to AN023, SBIAS/VREFI		
	AN000, AN002, AN004, AN006	1	
	AN001, AN003, AN005, AN007	0	-2^{15} to 0
Differential Input Mode	AN000, AN001, AN002, AN003, AN004, AN005, AN006, AN007	x	-2^{15} to $2^{15} - 1$
-	Self-diagnosis	x	-2^{15} to $2^{15} - 1$

x: Don't care

Note: A/D conversion result of odd channels AN000 to AN007 in single-ended mode can be inverted according to the ADCER.ADINV bit setting value. Therefore, the A/D conversion results can be stored in the A/D data registers in the same output range as even channels AN000 to AN008 or AN016 to AN023.

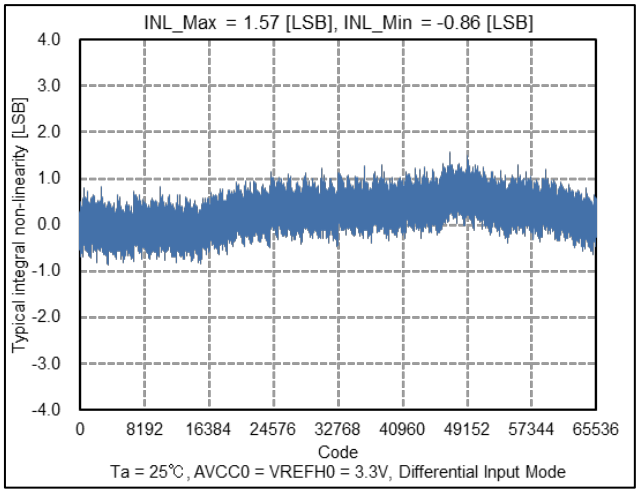

Figure 4. INL versus Code

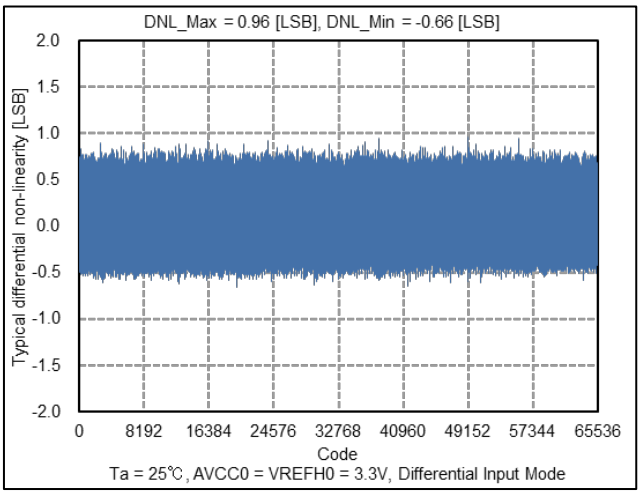

Figure 5. DNL versus Code

2.4 Dynamic Parameters

SINAD or ENOB is very important in many applications because it describes the smallest input signal that the converter can resolve. In closed loop systems, detecting small changes in input signals allows better control loop performance.

SINAD: Signal-to-noise and distortion (dB)

RMS level of input signal/sum RMS value of all noise and distortion excluding DC

ENOB: Effective number of bits

ENOB = (SINAD – 1.76 dB) / 6.02 dB

THD: Total Harmonic Distortion (dB)

Root-sum-square (RMS) value of the harmonics produced by the A/D converter relative to the RMS level of a sinusoidal input signal near full-scale.

THD is calculated up to 5th order harmonic distortion. THD = HD2 + HD3 + HD4 + HD5.

2.4.1 Improving Accuracy by Averaging A/D Conversion Result

The 16-Bit A/D Converter has a function for averaging the results of A/D conversion. A/D conversion is performed multiple times consecutively, and the result is averaged. This can suppress the influence of sudden noise and improve the accuracy of the conversion result.

Table 4. SINAD and ENOB Characteristics Evaluation Results of 16-Bit A/D Converter

Conditions: VCC = AVCC0 = AVCC1 = VREFH0 = 3.3 V or 5.0 V, VSS = AVSS0 = AVSS1 = VREFL0 = 0 V,
Fin = 1 kHz, External clock input used.

Parameter	Symbol	Typ		Unit	Test Conditions
		AVCC0 = 3.3 V	AVCC0 = 5.0 V		
Signal-to-noise and distortion	SINAD	83.4	85.3	dB	Differential input, No averaging
		86.1	87.8		Differential input, 2 times average
		88.5	90.0		Differential input, 4 times average
		90.8	91.8		Differential input, 8 times average
		92.9	92.9		Differential input, 16 times average
		77.4	80.0		Single input, No averaging
Effective number of bits	ENOB	13.6	13.9	bit	Differential input, No averaging
		14.0	14.3		Differential input, 2 times average
		14.4	14.7		Differential input, 4 times average
		14.8	15.0		Differential input, 8 times average
		15.1	15.1		Differential input, 16 times average
		12.6	13.0		Single input, No averaging

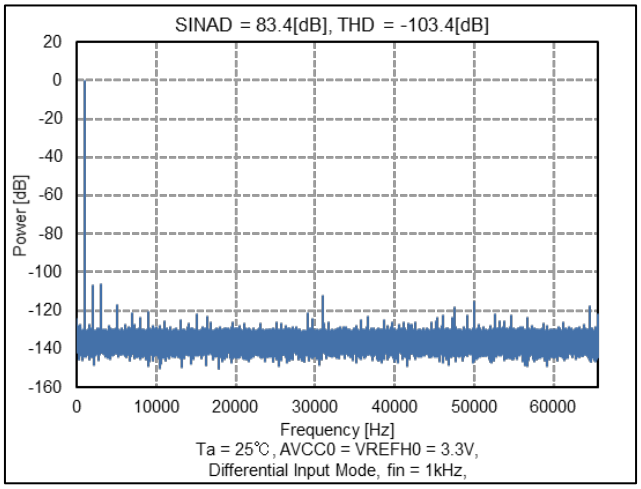

Figure 6. FFT of 8x Decimated ADC Output

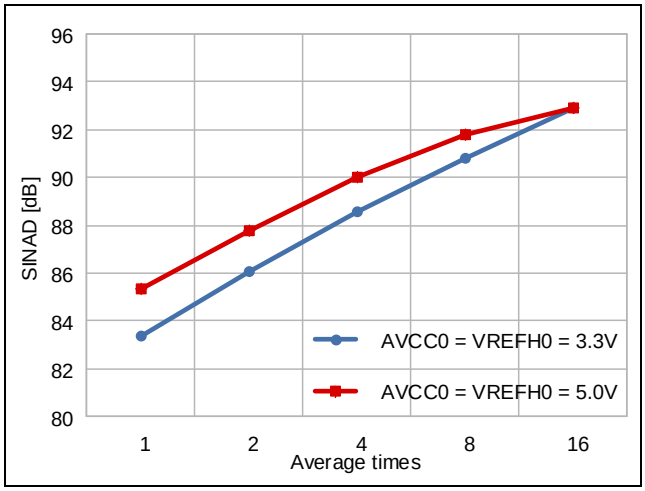

Figure 7. SINAD versus Average Times

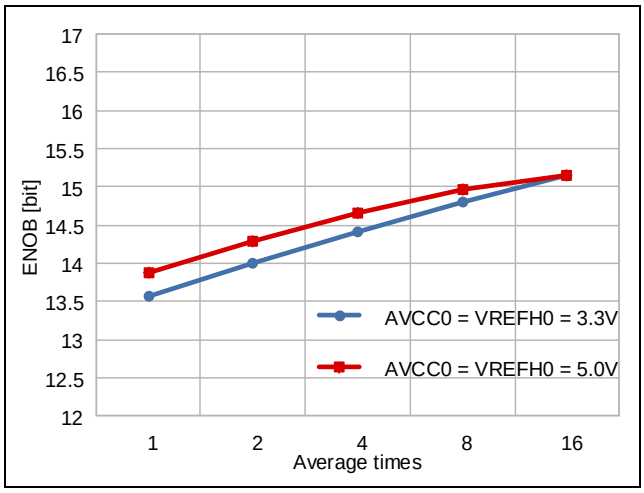

Figure 8. ENOB versus Average Times

2.5 Operating and Standby Current

Table 5 to Table 6 show operating current evaluation results of the A/D converter module stop state, A/D conversion wait state, and A/D conversion state.

Table 5. Operating Current Evaluation Result in A/D Conversion Wait State

Conditions: VCC = AVCC0 = AVCC1 = VREFH0 = 3.3 V, VSS = AVSS0 = AVSS1 = VREFL0 = 0 V,
HOCO clock oscillation frequency = 32 MHz, PCLKD = 32 MHz, MSTPCRD.MSTPD16 = 0b,
ADCSR.ADST = 0b

Parameter	Symbol	Typ	Unit	Test Conditions
Analog power supply current	I_{AVCC0}	598	µA	-
Reference power supply current	I_{VREFH0}	17.2	µA	-

Table 6. Operating Current Evaluation Result in A/D Conversion State

Conditions: VCC = AVCC0 = AVCC1 = VREFH0 = 3.3 V, VSS = AVSS0 = AVSS1 = VREFL0 = 0 V,
HOCO clock oscillation frequency = 32 MHz, PCLKD = 32 MHz, MSTPCRD.MSTPD16 = 0b,
ADCSR.ADST = 1b

Parameter	Symbol	Typ	Max	Unit	Test Conditions
Analog power supply current	I_{AVCC0}	989	1204	µA	-
Reference power supply current	I_{VREFH0}	37.5	67.3	µA	-

3. Calibration Function

Calibration allows high-precision A/D conversion by obtaining the capacitor array D/A converter (C-DAC) linearity error correction coefficient and gain (offset) error correction coefficient from the internally generated analog input under usage conditions.

All correction coefficients are derived using special ultra-high-precision equipment for 16-bit A/D converter only and are stored in the microcontroller's flash memory at the time of factory shipment. ADC16 characteristics described in the *MCU User's Manual* are realized by automatically loading the correction coefficient at microcontroller startup.

There are two additional ways to improve the characteristic:

1. Correct offset error and gain error.
2. Re-derive all correction coefficients.

When temperature and supply voltage change, it is possible to correct offset error and full-scale error by using 3 level self-diagnostic A/D conversion results. The offset is obtained by ADRST.DUAGST=10 and the gain error by ADRST.DUAGST= 01 or 11. The linearity errors of the C-DAC are not dependent on temperature and voltage. Since one-time self-diagnostic conversion results fluctuate, average the conversion results of several tens or more values to obtain the accurate offset error and full-scale error.

In order to re-derive all correction coefficients, the ADCALEXE.CALEXE bit is set to 1 and calibration starts. Calibration time is a little longer, about 24 ms at ADCLK = 32 MHz. When using the calibration function, be sure to perform in an environment where the analog block power supply, reference power supply, and ADCLK are stable. If calibration is performed in an unstable environment, A/D conversion accuracy might deteriorate more than at the time of shipment.

3.1 Calibration Flow

Figure 9 shows the calibration operation.

1. When the ADCSR.ADST bit becomes 1 (A/D conversion start) by writing 1 to ADCALEXE.CALEXE bit with software, the correction values for C-DAC linearity error and GAIN error are calculated.
2. When calculation of all correction values completes and the ADICR.ADIC[1:0] bits are set to 11b (ADC16_ADI interrupt due to calibration end enabled), an ADC16_ADI interrupt request is generated.
3. The ADCSR.ADST bit remains 1 (A/D conversion start) during calibration and is automatically cleared to 0 when calculation of all correction values completes and the A/D converter enters the standby state.

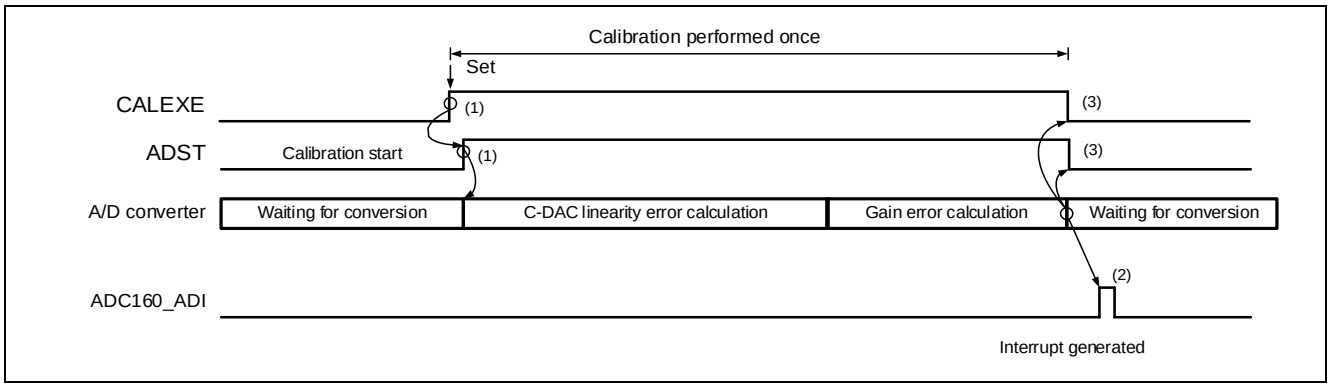

Figure 9. Calibration Operation (C-DAC Linearity Error Calculation and Gain Error Calculation) Example

Figure 10 shows the software flow and an operation example.

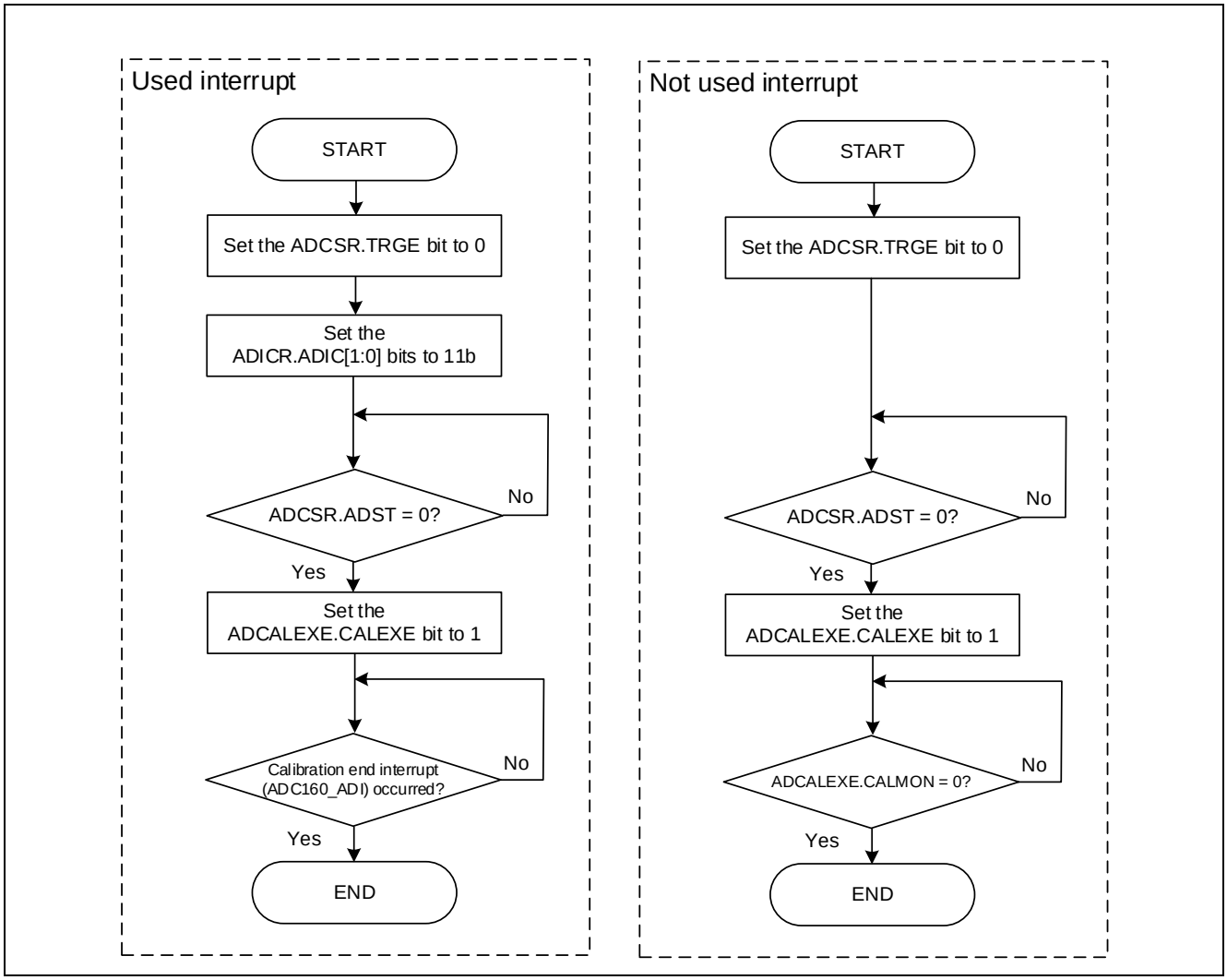

Figure 10. Software Flow and Calibration Operation Example

Website and Support

Visit the following vanity URLs to learn about key elements of the RA family, download components and related documentation, and get support.

RA Product Information	www.renesas.com/ra
RA Product Support Forum	www.renesas.com/ra/forum
RA Flexible Software Package	www.renesas.com/FSP
Renesas Support	www.renesas.com/support

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Dec.19.19	—	Initial release

Notice

1. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation or any other use of the circuits, software, and information in the design of your product or system. Renesas Electronics disclaims any and all liability for any losses and damages incurred by you or third parties arising from the use of these circuits, software, or information.
2. Renesas Electronics hereby expressly disclaims any warranties against and liability for infringement or any other claims involving patents, copyrights, or other intellectual property rights of third parties, by or arising from the use of Renesas Electronics products or technical information described in this document, including but not limited to, the product data, drawings, charts, programs, algorithms, and application examples.
3. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
4. You shall not alter, modify, copy, or reverse engineer any Renesas Electronics product, whether in whole or in part. Renesas Electronics disclaims any and all liability for any losses or damages incurred by you or third parties arising from such alteration, modification, copying or reverse engineering.
5. Renesas Electronics products are classified according to the following two quality grades: “Standard” and “High Quality”. The intended applications for each Renesas Electronics product depends on the product’s quality grade, as indicated below.
   "Standard": Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; industrial robots; etc.
   "High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control (traffic lights); large-scale communication equipment; key financial terminal systems; safety control equipment; etc.

   Unless expressly designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not intended or authorized for use in products or systems that may pose a direct threat to human life or bodily injury (artificial life support devices or systems; surgical implantations; etc.), or may cause serious property damage (space system; undersea repeaters; nuclear power control systems; aircraft control systems; key plant systems; military equipment; etc.). Renesas Electronics disclaims any and all liability for any damages or losses incurred by you or any third parties arising from the use of any Renesas Electronics product that is inconsistent with any Renesas Electronics data sheet, user’s manual or other Renesas Electronics document.
6. When using Renesas Electronics products, refer to the latest product information (data sheets, user’s manuals, application notes, “General Notes for Handling and Using Semiconductor Devices” in the reliability handbook, etc.), and ensure that usage conditions are within the ranges specified by Renesas Electronics with respect to maximum ratings, operating power supply voltage range, heat dissipation characteristics, installation, etc. Renesas Electronics disclaims any and all liability for any malfunctions, failure or accident arising out of the use of Renesas Electronics products outside of such specified ranges.
7. Although Renesas Electronics endeavors to improve the quality and reliability of Renesas Electronics products, semiconductor products have specific characteristics, such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Unless designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not subject to radiation resistance design. You are responsible for implementing safety measures to guard against the possibility of bodily injury, injury or damage caused by fire, and/or danger to the public in the event of a failure or malfunction of Renesas Electronics products, such as safety design for hardware and software, including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult and impractical, you are responsible for evaluating the safety of the final products or systems manufactured by you.
8. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. You are responsible for carefully and sufficiently investigating applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive, and using Renesas Electronics products in compliance with all these applicable laws and regulations. Renesas Electronics disclaims any and all liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
9. Renesas Electronics products and technologies shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations. You shall comply with any applicable export control laws and regulations promulgated and administered by the governments of any countries asserting jurisdiction over the parties or transactions.
10. It is the responsibility of the buyer or distributor of Renesas Electronics products, or any other party who distributes, disposes of, or otherwise sells or transfers the product to a third party, to notify such third party in advance of the contents and conditions set forth in this document.
11. This document shall not be reprinted, reproduced or duplicated in any form, in whole or in part, without prior written consent of Renesas Electronics.
12. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products.

(Note1) “Renesas Electronics” as used in this document means Renesas Electronics Corporation and also includes its directly or indirectly controlled subsidiaries.

(Note2) “Renesas Electronics product(s)” means any product developed or manufactured by or for Renesas Electronics.

(Rev.4.0-1 November 2017)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

Contact information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
www.renesas.com/contact/.