DESIGNING FOR HOT INSERTION AND MULTIPLE POWER SUPPLY SYSTEMS

APPLICATION NOTE AN-158

By Stanley Hronik

INTRODUCTION

There are many applications where components on one side of an interface are powered while components on the opposite side of the interface are either unpowered or powered at a different voltage level. Special care must be taken when designing these interfaces to prevent situations that would cause damage to the system.

The common characteristic in these situations is the applying of a voltage to an interface pin of a component that is either powered off or has a Vcc that is lower than the driving voltage. Hot insertion situations compound the problems by including partial connection scenarios in the list of potential interface conditions.

This application note addresses the problems found in hot insertion and multiple power supply system applications. Recommendations on component selection and design techniques to complete a successful interface are given.

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APPLICATIONS

Applications that require the use of multiple power supplies and hot insertion include:

1) **Fault tolerant systems** that allow the changing of circuit boards during active operation.
2) **Power conserving systems** where portions of the system are shut down during idle times.
3) **5V to 3.3V interfaces** where the 5V power supply is higher than the 3.3V supply, or one supply can be turned off while the other is active.
4) **Large systems** with multiple independent power supplies or independently powered sections. This could include systems in which the power does not rise and fall uniformly across the system due to loading, disconnects, or poor regulation.
5) **Cables or other external interfaces** that may become connected or disconnected during powered operation. Cables also are used to connect systems with independent power supplies.

Many components have been designed for use in these applications. "Power-off Disable" is the name used to describe the capability of components to interface to an active bus while unpowered.

PROBLEMS THAT DEVELOP

In the applications listed, there are two areas of concern. These are:

1) Applying power to the interface pins of unpowered or partially powered devices.
2) Properly sequencing powered connections to an unpowered component.

When designing the interface and the method for hot insertion or power down, care must be taken to avoid forward biasing clamp diodes within the interface components. If a clamp diode should become forward biased, excessive current levels and potential destruction of either the component with the clamp or the driver may occur. Examples of how these problems can develop are shown in the following figures.

TheVcc Clamp Diode

Many components are designed with clamp diodes between the device outputs and Vcc. This clamp diode is inherent in P-Channel FETs which are frequently used in 3.3V components and CMOS rail swing devices to pull the output voltage to the Vcc rail. Many manufacturers also add clamp diodes to their components for added ESD protection.

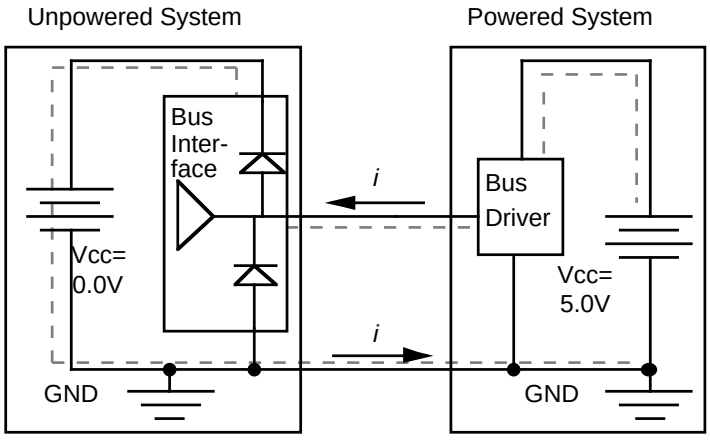

Figure 1, Forward Biased Clamp Diode

Figure 1 shows how a component with a clamp diode to Vcc can cause system failures if connected to an active bus when unpowered. In the figure the Bus Driver attempts to pull the output HIGH, but instead finds a low impedance path (as

shown by the dotted line) through the device clamp diode and into the off power supply. Excessive current can easily develop, causing failure of the Bus Interface component or the Bus Driver.

Disconnecting the unpowered supply or putting a blocking diode in the unpowered supply does not solve the problem. In this case the current flowing through the clamp diode will attempt to raise the Vcc level on the entire unpowered system. The potential to damage either the bus interface component or the bus driver still remains.

The Ground Disconnect

When performing hot insertion or other power off disable functions, the ground connections must be made first and maintained until all other connections are released. This prevents unexpected return current paths from developing through sensitive components.

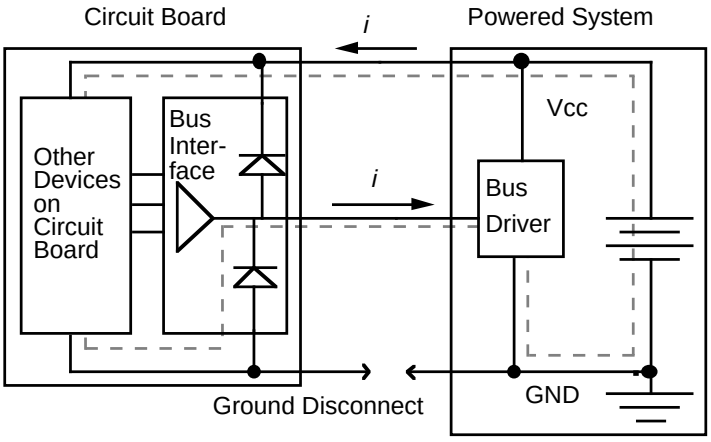

Figure 2, Ground Disconnect

Figure 2 shows how a disconnected ground can cause device failure by routing all current for powering the board through the clamp diode on the bus interface and bus driver components. The dotted line shows the low impedance current path.

COMPONENT CHARACTERISTICS

Components that have a power-off disable capability will have a high impedance on their interface pins when the component is powered off. The high impedance allows the component to be connected to active busses and active interfaces while in the off (powered down) state. The high impedance component will not drive or pull down the bus.

Figure 3 shows an example of the possible locations of clamp diodes on a device output. If the voltage on the output pin drops below GND or rises above Vcc, it is possible to forward bias one of the clamp diodes.

On inputs, Vcc clamp diodes are not present unless the port is an I/O port with an output clamp that affects the input. I/O ports simply combine an input and an output structure on the same pin. Because all inputs have no clamp diode to Vcc, whether the I/O port has power-off disable is determined exclusively by the output structure.

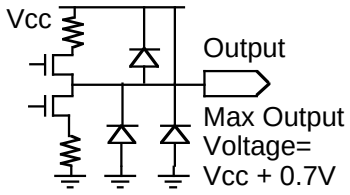

Figure 3, An Output Structure Clamped to Vcc

Almost all logic components have clamp diodes to GND on both the inputs and outputs.

A component needs to have power-off disable only on the interface that connects to the active bus while the component is powered off. For instance an FCT163244 function with no Vcc clamp on its input can be connected to an active bus with its input side, but not output side.

		Input Clamp		Output Clamp	
Double Density		Vcc	GND	Vcc	GND
High Drive	FCT16xxxT		X		X
Balanced Drive	FCT162xxxT		X	X	X
BD-Lite	FCT166xxxT		X	X	X
3 Volt FCT	FCT163xxx		X	X	X
3 Volt FCX (5V tol)	FCX16xxx		X		X
3 Volt FCX (5V tol)	FCX162xxx		X	X	X
High Speed 3 Volt	ALVH16xxx		X	X	X
High Speed 3 Volt	ALVH162xxx		X	X	X
Bus Switch	FST16xxx		X		X
Resistored Bus Switch	FST162xxx		X		X

		Input Clamp		Output Clamp	
Octal		Vcc	GND	Vcc	GND
High Drive 1	FCTxxxT		X		X
Balanced Drive	FCT2xxxT		X	X	X
3 Volt FCT	FCT3xxx		X	X	X
CMOS Output	FCTxxx		X	X	X
Bus Switch	FSTxxx		X		X
Resistored Bus Switch	FST2xxx		X		X

Table 1, Clamp Diode Structure of IDT Logic[1]

For IDT logic components, Table 1 lists the clamp diode structures for all of the bus interface components.

Data Sheet Power-Off Specifications

To determine if a component has no Vcc clamp diode, a user should check the data sheet for an Ioff specification. Components with power-off disable capabilities frequently have an Ioff specification in the DC characteristics table or in the OUTPUT DRIVE CHARACTERISTICS table of the data sheet as shown in Table 2.

1. High Drive Octal components manufactured prior to October 1995 had Vcc clamp diodes on selected parts. Check with the factory for the status of particular components. Components with an Ioff specification are guaranteed to have no Vcc clamps regardless of date of manufacture. Double Density High Drive are guaranteed to have no clamp diodes regardless of manufacture date.

Sym	Parameter	Test Conditions	Max	Unit
Ioff	Input/Output Power Off Leakage	Vcc = 0V Vin or Vo ≤4.5V	±1	µA

Table 2, Data Sheet Ioff Specification

Also the ABSOLUTE MAXIMUM RATINGS table should have a specification for input and output voltage that allows the voltage to rise to the absolute maximum voltage for breakdown (typically 7.0 for 5V or 4.6 for 3.3V). If instead, the maximum voltage is described in terms of Vcc, it indicates there is a clamp present. In Table 3 the first line Vterm(1) indicates the described pin has Power-off Disable, while the second line Vterm(2) indicates the described pin has a clamp diode to Vcc and will short circuit an active bus if Vcc = 0 or some voltage less than nominal.

Sym	Parameter	Commercial	Unit
Vterm(1)	Terminal Voltage with Respect to GND	-0.5 to 7.0	V
Vterm(2)	Terminal Voltage with Respect to GND	-0.5 to Vcc + 0.5	V

Table 3, Data Sheet Input/Output Voltage Specification

Most components have a clamp diode to GND. This can be seen in Table 3 where Vterm is limited to -0.5V on the bottom side for both terminals.

DESIGN CONSIDERATIONS

When designing an interface for Power-off Disable many design issues come into play. Whether or not a Vcc clamp diode will cause problems depends upon the configuration. The absence of a Vcc clamp diode does not guarantee proper operation. A few of the design considerations are listed here.

Power Up/Down Impedance

During power up and power down operation when a component is interfacing an active data bus, the component must avoid interfering with the active bus (causing bus contention). Ideally the component will maintain a high impedance throughout the voltage transition and not communicate with the bus until the component is fully operational and the bus acknowledges the new driver.

In IDT logic components, the input threshold level will scale with Vcc. For both 5V and 3.3V components at nominal Vcc the input threshold toggle point is about 1.5V. This will drop proportionately with Vcc.

To guarantee a high impedance output during power up and power down, the /OE input should be held at >50% of Vcc over all voltages. Under this condition, the output will not drive or interfere with active components on the bus. A high /OE can be maintained with a pull up resistor to Vcc, provided the device controlling the /OE does not overdrive the resistor. Possibly a power on reset circuit can be used to control the interface.

Using Vcc Clamped Components

A clamped component may be used to drive across an interface if there are no other components on the bus that that are active at any time when the clamped component has a low Vcc. As an example, a clamped Balanced Drive component could be used on an interface if it can be guaranteed that the bus will never be driven by any device when the Balanced Drive Vcc is lower than the driving voltage.

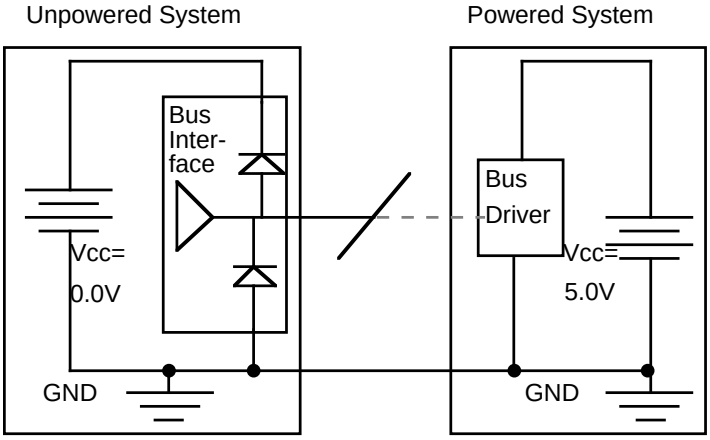

Figure 4, Clamp diode on a 3-state bus

Figure 4 is a re-creation of Figure 1 except all bus drivers on the bus are in a high impedance mode. As long as no driver attaches a voltage to the bus, there is no path for current to flow through the Vcc clamp on the unpowered device.

The Use of backplane Jumpers

Many designs use jumper wires to Vcc or GND at the backplane interconnect. These are frequently used for slot identification, device identification, or presence detect. In all cases, these jumpers should be current limited with a series resistor. In the case of a break in the power connection or power return path to the board, in some cases a jumper directly connected to Vcc or GND may become the primary power source or return path. Any component on the other side of the interface may be damaged in the process.

Using Bus Switch

Bus switch is a FET switch connecting one port to another. In a hot insertion or dual power supply application, the bus switch will protect a sensitive interface against damaging currents or voltages.

In a Power-off Disable application, placing a bus switch on the interface gives the ability to maintain a high impedance on the port regardless of the type of component connected at the interface.

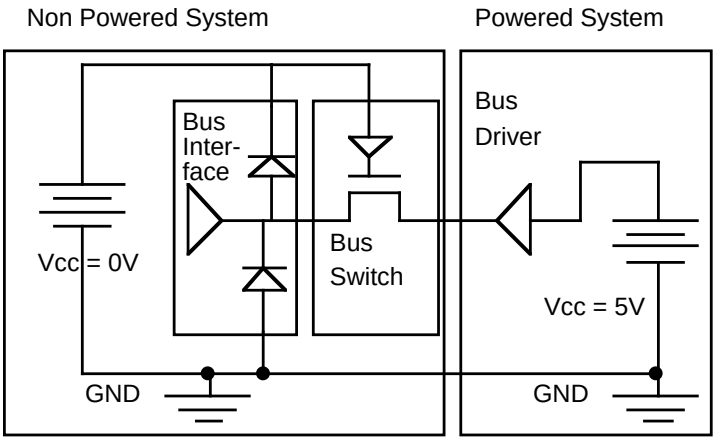

Figure 5, Bus Switch on the Low Power Side

As shown in Figure 5, placing a Bus-Switch on the interface prevents the voltage on the sensitive interface from rising above Vcc, even as Vcc approaches zero. As Vcc is lowered, the bus switch gate will be unable to turn on, keeping the voltage low. In the case of a random or accidental connect/ disconnect this scheme will prevent damage to the interface.

During power ramping, either a power on reset must hold the switch in the off state to prevent interaction with an active bus, or the bus must be in a high impedance idle state.

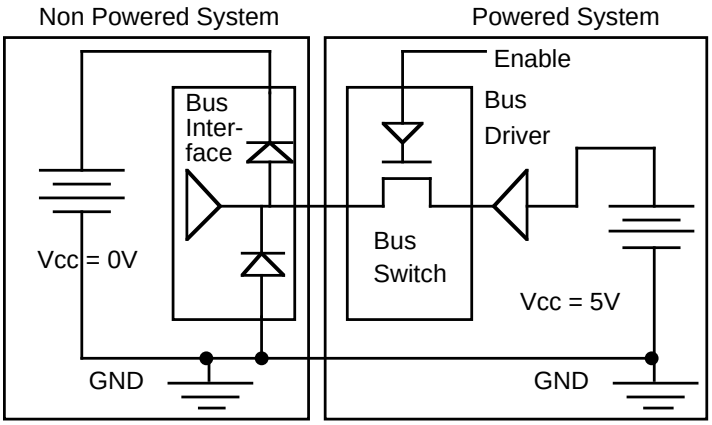

Figure 6, Bus Switch on the High Power Side

Figure 6 shows how a bus switch on the active interface can also be used to protect a clamped or otherwise sensitive connection. In Figure 6, the switch can be disabled (using the enable control), which will shut off any current flow to the connection point. The non powered system can then be disconnected, connected, or undergo power up/down without concerns about damage or interacting with the powered system.

The connection scheme shown in Figure 6 is ideal for applications where a controlled, orderly insertion or removal is required. In the opposite case where the disconnection is a random, unpredicted event such as an accidental cable disconnect, the switch shown in Figure 6 may not be disabled. This may allow damaging currents to cross the interface. In this case the scheme of Figure 5 should be used.

Interfacing 3.3V

3.3V systems tend to use clamp diodes to Vcc on device outputs because of the need to pull the output to the Vcc rail to achieve a logic HIGH. Since most 5V components are capable of pulling voltages higher than the 3.3V power supply, the interface issue between 3.3V and 5V is an extension of the Power-off Disable situation.

When designing with 3.3V components in systems with multiple power supplies, especially 5V supplies, it is necessary to avoid forward biasing a clamp diode. When designing the interface, use components that have no Vcc clamp, or limit the bus to unidirectional operation.

Bus Switch can be used as a 5V, 3.3V translator by placing a diode in series with the 5V Vcc pins on the Bus Switch. This limits the voltage passing from the 5V to 3.3V port, if the power supplies are tightly controlled[2]. During power off and ramping conditions, it would still be necessary to disable the interface through the /OE.

Clock Distribution on Backplanes

Distributing a clock across a backplane is an example of an application that easily adapts to hot insertion and power down modes with no special considerations as shown in Figure 7. Typically one central board in the backplane is used to distribute the clock. Driving the clock with a clock buffer (e.g. FCT807T) allows matching all clock lines and trace lengths across the backplane.

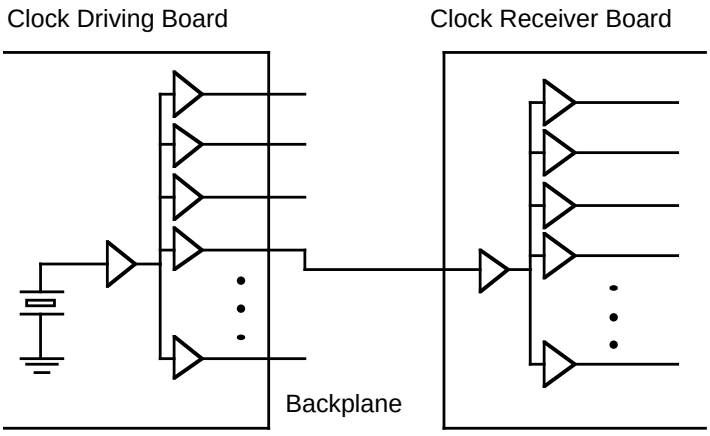

Figure 7, Backplane Clock Distribution

Placing a clock distribution buffer on each receiving card makes a single point receiver for each line. Since clock buffers are unidirectional parts, there is no clamp diode on the input, regardless of whether the part is 3V, 5V TTL or 5V CMOS (check with manufacturer if non IDT parts are used). Since there are no input clamps to Vcc, the clock buffer can interface the backplane when powered, unpowered, or under hot insertion without damage.

2. This is a frequently used method for translating between 5V and clamped 3.3V systems. Despite this, if the 3.3V supply drops towards the minimum voltage (3.0V or less) and the 5V supply approaches the maximum (5.5V), it is possible to damage the 3.3V component by passing excessive current into the clamp diode.

CONCLUSION

When designing an interface for hot insertion or use with multiple power supplies there are both workable and damaging situations that can develop.

Acceptable Interface Conditions

1. Interfacing a component with no Vcc clamp to an active bus.
   a) Component may be powered on or off.
   b) Some components have clamps on selected pins only. Unclamped pins can be attached to an active bus when unpowered.
2. Interfacing a clamped component to a bus while the component is powered off if no other device drives the bus to a logic HIGH. The bus should have no terminators or pull up resistors that pull the bus HIGH.
3. During power up/down, holding /OE in the disable mode to prevent driving the bus.
4. Using a Bus Switch on the interface between the two Vcc levels.
   a) Bus switch on the low Vcc side will limit voltages to acceptable levels.
   b) Bus switch on the high Vcc side can disable the connection.
5. GND connections must be maintained during power up/down and hot insertion.

Potentially Damaging CONDITIONS

1. Ground Breaks
   a) Disconnecting GND between power supplies while other connections are still valid.
   b) Connecting Vcc before GND during hot insertion.
2. Raising an output with a Vcc clamp to a voltage above Vcc.
   a) Powering off a component with a Vcc clamp while it is attached to an active, driven bus.
   b) Connecting a 3.3V clamped output port to a 5V bus.
3. Allowing bus contention during power up/down (or any other time) where the contending voltage is above the Vcc level on a Vcc clamped output.
   4. Hardwiring a signal line to Vcc or GND with no series resistor (an example would be a presence detect pin or device ID tied to Vcc).

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