CLOCK AND SIGNAL DISTRIBUTION USING FCT CLOCK BUFFERS

APPLICATION NOTE AN-150

INTRODUCTION

In synchronous systems where timing and performance of the system are dependent on the clock, integrity of the clock signal is important. Thus information on the characteristics of IDT clock buffers are provided in this application note. IDT has a family of low skew clock distribution chips. This application note discusses both IDT clock buffer characteristics and general clock distribution issues. Information on IDT's phase-lock loop-based clock distribution chips can be found in specific datasheets and a separate application note (AN-155).

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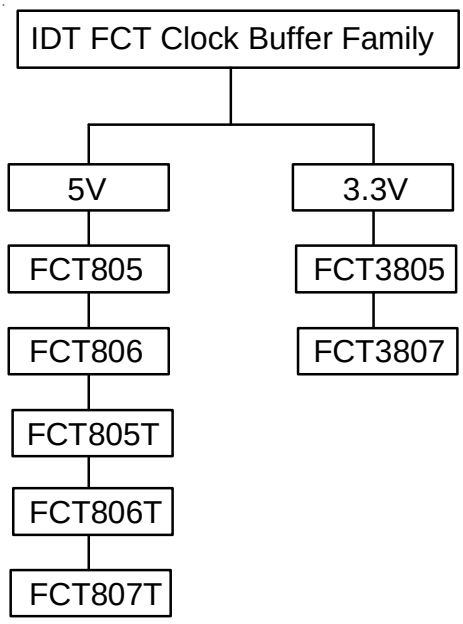
CLOCK BUFFER CHARACTERISTICS

All IDT clock buffers have 150 to 200mV of hysteresis. Their input structure is similar to other FCT/FCT-T devices and is shown in figure 1(next page). 5V FCT-T (TTL outputs) clock buffers have a totem pole output structure consisting of an nchannel pullup transistor and an n-channel pulldown transistor. 5V FCT (CMOS outputs) clock buffers and 3.3V clock buffers, however, have a p-channel pullup instead. Figure 2 (next page) shows the two types of clock buffer output structures.



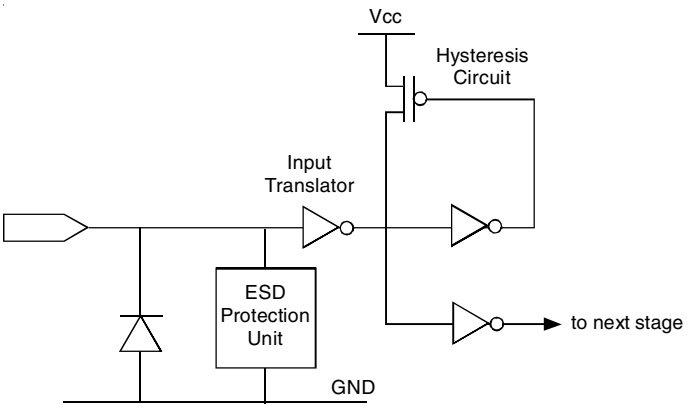
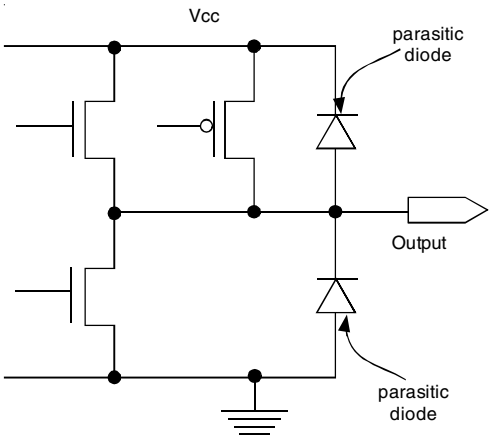


Figure 1: IDT Clock Buffer Input Structure

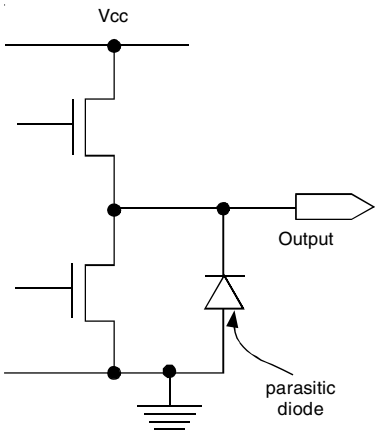
The devices with p-channel pullups have rail-to-rail output voltage swings, while devices with n-channel pullups have TTL output voltage swings. This difference is highlighted in a datasheet by typical V_{OH} specifications as shown in the tables below.

Another difference between the two types of output structures is the parasitic diode clamp to Vcc. 5V FCT-T buffers have no diode clamp to Vcc, while 3.3V devices and 5V FCT buffers have the diode.

Static drive specifications in datasheets are often standard values maintained for compatibility reasons. The output drive characteristics of a device are usually more accurately represented by typical V/I curves. The output V/I graphs for the pullup(logic high) and pulldown(logic low) stages of IDT clock drivers are shown in figures 3, 4, 5 and 6 (next page). The equivalent output impedance of the driver can be obtained from the straightline portion of the output V/I curves. The FCT LOGIC HIGH, FCT-T LOGIC HIGH, and CLOCK BUFFER OUTPUT DRIVE tables present output driver information on various IDT clock buffers. Clock lines are often required to drive long traces and need sufficient drive capability for this. IDT Clock drivers typically have strong output drivers. Transmission line impedances have been superimposed on the output V/I curves in figures 3,4,5 and 6 to give an idea of the impedance the driver is capable of switching. In addition to the 50Ω load the graphs also show the minimum impedance each driver is capable of switching on first incidence. As more aggressive technologies are introduced speeds and edge



CMOS Output: FCT805/806, FCT3805, FCT3807



TTL Output: FCT805T/806T, FCT807T

Figure 2: IDT Clock Buffer Output Structures

FCT LOGIC HIGH

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL} (V_{HC} = V_{CC} - 0.2V), I_{OH} = -15mA	V_{HC}	V_{CC}	–	V

FCT-T LOGIC HIGH

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}, I_{OH} = -15mA	2.4	3.3	–	V

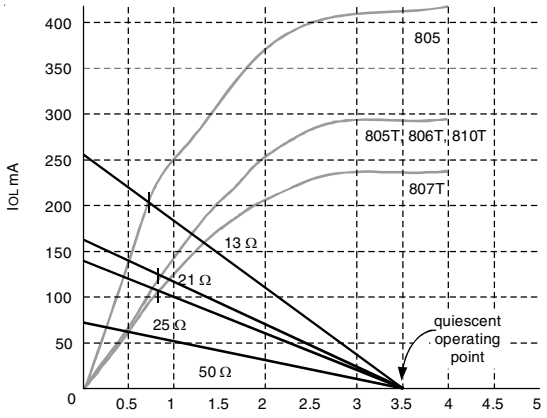


Figure 3: FCT805, FCT805T/ 806T, FCT807T Output LOW

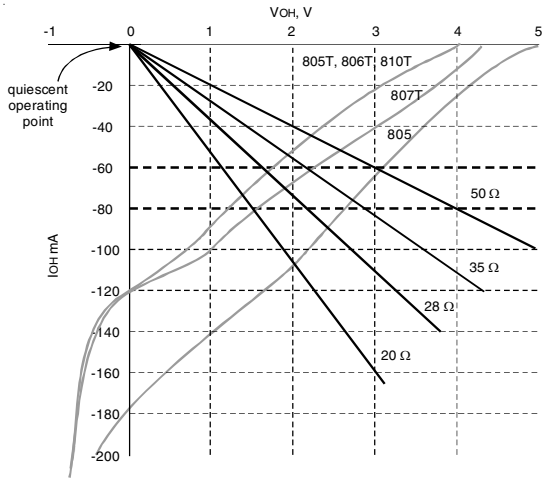


Figure 4: FCT805, FCT805T/ 806T, FCT807T Output HIGH

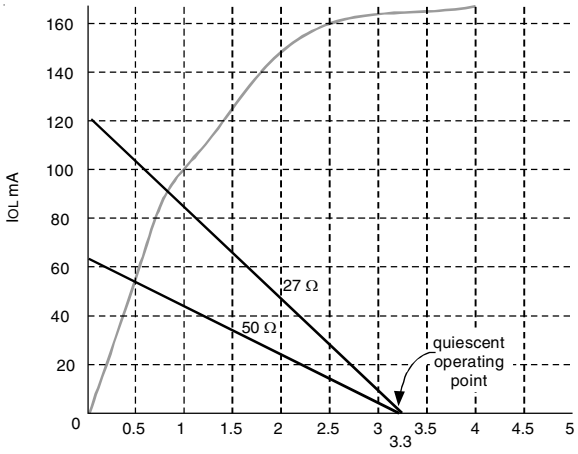


Figure 5: FCT3805/ 3807 Output LOW

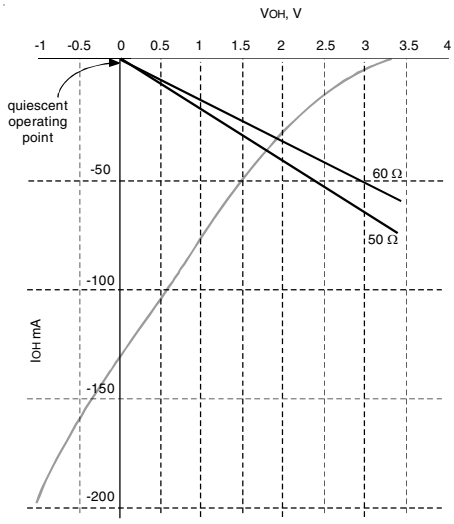


Figure 6: FCT3805/ 3807 Output HIGH

CLOCK BUFFER OUTPUT DRIVE AND IMPEDANCE

Device	Output Voltage Swing	Ron (HIGH)	Ron (LOW)	Dymanic Drive (typ.) I_{ODH}/ I_{OLD}	Static Drive Specs I_{OH}/ I_{OL}
FCT805/806	CMOS	25Ω	4Ω	-120/320mA	-24/64mA
FCT3805T/806T	TTL	25Ω	8Ω	-70/210mA	-15/48mA
FCT807T	TTL	33Ω	8Ω	-80/175mA	-15/48mA
FCT3805	CMOS	12Ω	19Ω	-50/115mA	-8/24mA
FCT3807	CMOS	12Ω	29Ω	-50/135mA	-8/24mA

rates get faster. The CLOCK BUFFER OUTPUT DRIVE table summarizes typical edge rates encountered with IDT clock buffers. These edge rates are measured between 10% and 90% levels into a standard 50pF, 500Ω load. In addition to this rise and fall times between 0.8V and 2.0V are also specified in the datasheet.

AC CHARACTERISTICS

IDT clock buffers are available in a number of different speed grades and key parameters are shown in the 5V CLOCK BUFFER and 3.3V CLOCK BUFFER tables. AC parameters for logic devices are specified with a standard test load of 50pF in parallel with 500Ω. In the case of clock buffers, some devices like the 807 and 3807 are specified with several different load configurations that include pure capacitive loads and transmission line loads. This provides users with a closerapproximation to the real life load. AC performance tends to degrade at higher capacitive loads and this performance penalty can be estimated using derating factors. Typical derating factors for IDT clock buffers are :

Propagation delay load derating	2ns/100pF
Output skew load derating	75ps/10pF

5V CLOCK BUFFER PERFORMANCE

Parameter	805, 806	805A, 806A	805BT, 806BT	805CT, 806CT	807BT	807CT
t_{PD}	6.5	5.8	5	4.5	3.8	3.5
$t_{SK(O)}$	0.7	0.7	0.7	0.5	0.5	0.25
$t_{SK(P)}$	1	1	0.7	0.6	0.5	0.35
$t_{SK(T)}$	1.5	1.5	1.2	1	1	0.75

3.3V CLOCK BUFFER PERFORMANCE

Parameter	3805	3805A	3807	3807A
t_{PD}	5.8	5	4.8	4.3
$t_{SK(O)}$	0.7	0.7	0.5	0.35
$t_{SK(P)}$	1	0.7	0.5	0.35
$t_{SK(T)}$	1.5	1.2	1	0.75

SIGNAL INTEGRITY

Noise on a clock line is harmful because it can result in false switching and data corruption in downstream devices. Taking appropriate steps to reduce noise on the clock line is critical since it can have wide ranging effects on systems ranging from EMI and system malfunction to degradation of performance and reliability. This section provides some guidelines on improving clock signal integrity.

Switching noise

As in the case of all high performance logic, a key contributor to noise on a clock line is simultaneous switching noise or "ground/Vcc bounce". Every device has certain inherent switching noise characteristics which can be compared by means of a ground bounce test. This test requires that the effect of simultaneously switching outputs be measured on a "quiet" or low output. This is not always possible, especially in the case of clock buffers - there may be no "quiet" output available. In such cases, overshoot and undershoot on a switching output can be used as the next best measure of switching noise. Vcc or ground noise is given by,

$V_G = L_G di/dt = L_G (C_L.d^2V/dt^2)$

where

L_G = Vcc or ground lead inductance

C_L = Load capacitance

dV = Output voltage swing

dt = rise/fall time

The equation shows that switching noise is dependent on package inductance, edge rates, output voltage swings and the output load.

a. Package inductance

Packages with reduced lead inductances are to be preferred. Usually smaller packages tend to have lower associated package inductances.

b. Edge rates

Faster edge rates are usually responsible for generating greater ground bounce because Vg is inversely proportional to the square of dt. Edge rates on IDT buffers are given in the CLOCK BUFFER OUTPUT EDGE RATES table.

CLOCK BUFFER OUTPUT EDGE RATES(1)

Device	Rise Time	Fall Time
FCT805/806	3ns	1.7ns
FCT805T/806T	3.5ns	2.6ns
FCT807T	3ns	1.7ns
FCT3805	2.5ns	1.6ns
FCT3807	3.7ns	2.3ns

NOTE:
1. Typical output edge rates between 10% and 90% levels.

CLOCK BUFFER PACKAGE PARASITICS(1)

Package	Inductance L, nH	Capacitance C_{IN}/ C_{OUT}, pF
PDIP-20	8nH	6pF/8pF
PDIP-24	12nH	6pF/8pF
SOIC-20	5nH	6pF/8pF
SOIC-24	6nH	6pF/8pF
SSOP-20	4nH	6pF/8pF
SSOP-24	4nH	6pF/8pF
QSOP-20	3.5nH(1)	6pF/8pF
QSOP-24	3.5nH(1)	6pF/8pF

NOTE:
1. Modeled approximation.

c. Output voltage swings

Wider output voltage swings generate more switching noise(larger dV). Thus TTL outputs (FCT-T devices) are preferred over CMOS outputs (FCT devices) for 5V designs.

d. Output load

The output load effects two factors in the above equation - C_L and dt. V_G is directly proportional to C_L and inversely proportional to dt^2. Increasing the output load causes both C_L and dt to go up. Usually the effect of the increase in dt dominates and the switching noise decreases with increasing load, but this is not a linear variation and the decrease in switching noise tends to flatten out at large loads. The effect of other parasitics in the equation can also cause unpredictable effects with increasing capacitive load.

Transmission Line Reflections

Traces longer than four or five inches appear as transmission lines to an FCT/FCT-T driver. This is because an output edge rate faster than two or three times the transmission line delay requires special consideration over a simpler lumped capacitive load model. Typical microstrip traces have a line impedance of 70Ω which corresponds to a line capacitance of 2pF per inch or a delay of 0.15ns per inch. Typical FCT edge rates lie in the 2ns range. Once it has been determined that the load is in fact a transmission line, the line should be properly terminated in order to reduce line reflections. There are two main questions that arise:

1) Does the driver have sufficient drive capability to achieve first incidence switching at the receiver or the sending end of the line?

This can be verified by drawing a line with slope corresponding to the line impedance from the quiescent point (0V, 0mA for logic low and 3.5V, 0mA for a logic high TTL output) and intersecting the driver's output V/I curve. This is illustrated for the various IDT clock buffers in figures 3,4,5 and 6. In cases where the line has loads distributed along its length, the impedance of the line is driven down further. The loaded line impedance is given by:

$Z_L = Z_O [C_O / (C_O + C_L)]^{1/2}$

where

Z_O - the unloaded line impedance

Z_L - loaded line impedance

C_O - the inherent line capacitance per unit length

C_L - the load capacitance per unit length.

For example, a 10inch long 70Ω line loaded with two distributed loads of 8pF each presents a lowered effective line impedance of ~52Ω. A lower impedance now requires a stronger driver to drive to the same logic voltage threshold.

2) Is the line properly terminated to prevent line reflections and ringing?

The line can be terminated either at the near end or the far end. Series termination is used at the near end and parallel termination, Thevenin termination or ac termination is used at the far end. Near end termination seeks to match the source end impedance (output driver + series resistor) and absorbs relections at the near end. Far end termination seeks to match the termination value to the line impedance preventing any reflections at the far end. The advantages and disadvantages of the different termination schemes are discussed in greater detail in a separate IDT application note.

a. Type of termination

In general, the preferred termination techniques are series or ac termination. For tight timing budgets series termination sometimes poses a problem by adding to the output skew.

b. Termination values

Series termination - Sum total of driver output impedance and series resistor should equal the line impedance. Assuming a loaded line impedance of 50Ω, a termination value of 25Ω to 33Ω usually works.

Parallel termination - Termination value should match the line impedance.

Thevenin termination - Equivalent Thevenin impedance should match the line impedance. Also the voltage at the line termination point should be above the threshold voltage of the receiver. Terminating with 100Ω to Vcc & 100Ω to ground matches a 50Ω line impedance and also maintains a voltage at the line termination point of Vcc/2 which is above the receiver input threshold of 2.4V.

AC Termination - Here the value of the termination resistor should match the line impedance and the terminating capacitor value should be such that RC time constant > 3 times the line delay. Commonly used ac termination values for a 50Ω line are 50Ω and 220pF.

Decoupling

Adequate and proper decoupling is very important. Bypass capacitors provide the required current surge for transient switching. Some guidelines for decoupling high speed clock buffers are given below.

1. Use ceramic capacitors for each Vcc pin. 0.1mF is a good value to use here. One large MLC (multilayer ceramic chip capacitor) should be used per chip for power supply bypassing. These work best for power supply decoupling on account of their low inductance characteristics. A 10mF to 50mF capacitor value is usually suitable here.
2. The bypass capacitor should be placed right at the device Vcc pin where possible and connected to the ground plane on the other side. Capacitor, device and trace inductance which together make up the Vcc-ground loop length must be minimized.
3. Pick the capacitor value based on the device loading. The bypass cap should be able to supply the required amount of switching current at frequency.

As an example consider a case of a clock driver with 10 outputs each driving 70Ω transmission lines.

Total current required = 10 x 5V/ 70Ω = 714mA

So, I = CdV/dt = 714mA

Assuming an allowable Vcc droop of 30mV and an output edge rate of 2ns, minimum required bypass capacitor value

= 0.714 x 2ns / 30mV

= 0.047mF

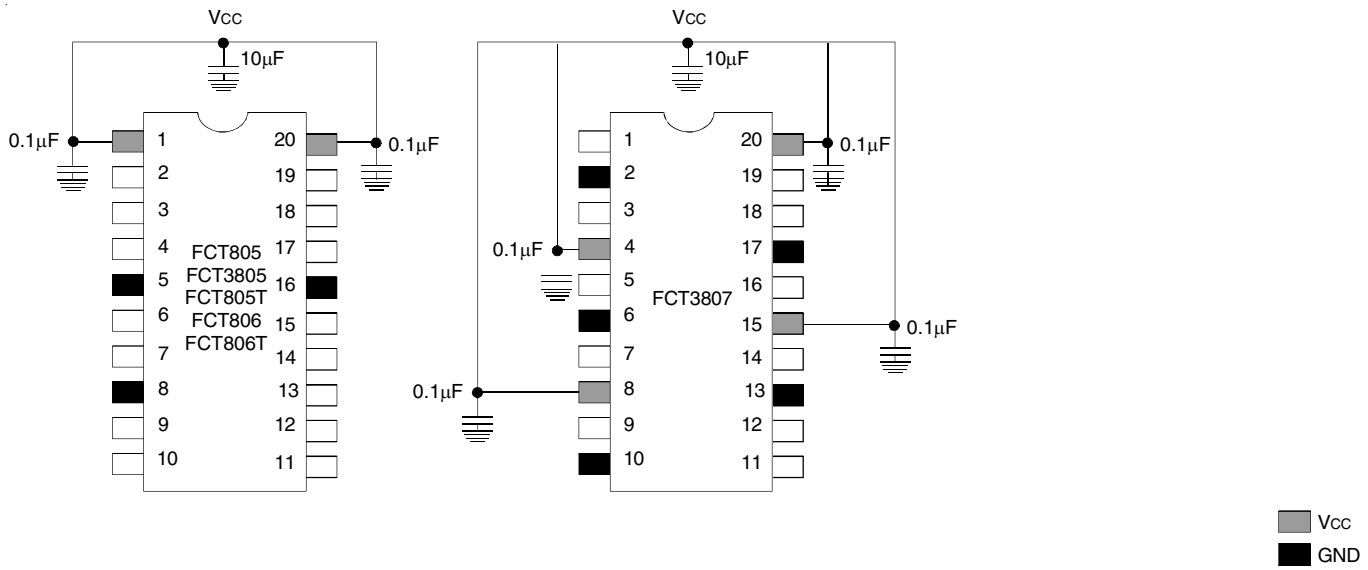


Figure 6: Recommended Decoupling

For lower values of line impedance, I increases and therefore a higher capacitor value may be required. Figure 7 shows decoupling schemes for IDT clock buffers.

EMI

There is a strong correlation between noise and EMI, so all precautions discussed in previous sections should be reviewed carefully when seeking to reduce EMI. In addition, some simple rules pertaining to board layout can help in reducing EMI.

A rule of thumb for reducing EMI is to ensure that the clock driver is located towards the center of the PCB rather than at the periphery. The magnetic dipole moments tend to be higher when the clock traces are located at the periphery of the board or card worsening the risk of EMI. Burying the clock traces in inner signal layers sandwiched between ground and Vcc planes is also a good precaution. For clock signals that are routed on a surface layer, additional EMI protection can be achieved by routing ground traces parallel to and on either side of the clock trace. Refer to REFERENCES for recommendations on spacing the vias connecting these ground traces to the ground plane.

Narrow signal traces tend to increase high frequency damping and reduce capacitive coupling between traces. Thus 4 to 8 mil traces should be used for clock signals. Right angles should be avoided as they increase the trace capacitance and also introduce an impedance discontinuity that could effect signal integrity. Crosstalk can contribute to EMI, so ensure that there are no clock lines running on long traces parallel to each other. Spacing between traces should at least equal the trace width.

Designs today call for the use of high speed logic families whose faster edge rates tend to radiate more high frequency energy. It is important therefore that the board enclosure contain the radiated energy. Shielding plays an important role in reducing EMI and adequate shielding should be provided around openings in the board enclosure such as cable or wiring outlets, disk drives, etc.

Ferrites are commonly used to suppress high frequency common mode radiation. The impedance of a ferrite varies with frequency, so that at high frequencies it behaves more like a resistor than an inductor. Thus by choosing a ferrite with appropriate impedance characteristics over frequency the ferrite's resistive losses can be used to eliminate specific offending frequency radiation.

SUMMARY

This application note seeks to provide designers with information on the characteristics of IDT clock buffers and guidelines to reduce noise on the clock signals. The designer is advised to refer to current IDT datasheets for specifications on all IDT clock products.

REFERENCES

Printed Circuit Design Techniques for the control of EMI, Michael Conn. 1993 HP High Speed Digital Symposium.

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