# R4600™ POWER CALCULATIONS

APPLICATION NOTE AN-129

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## INTRODUCTION

The IDT R4600™ Orion™ RISC microprocessor is a full 64-bit architecture that is fully compatible with numerous 32-bit and 64-bit Operating Systems and applications. It is a highly integrated microprocessor designed to serve embedded applications. It incorporates large on-chip caches (16KBytes for both the instruction and the data caches); both two-way set associative. The R4600 implements a large TLB to map 96 virtual pages (raging from 4KB to 16MB in size) to their corresponding physical addresses. The R4600 has a four deep write buffer to isolate the high speed internal caches from the low speed external memory.

The R4600 uses advanced power management techniques to lower the peak and typical power consumption. The power saving is implemented through an intelligent scheme which turns off the power from the unused sections of the device (e.g. the FPU). A standby mode is also available which shuts down the internal clocks and freezes the pipeline, thus reducing the consumed power substantially. This feature is very desirable for power sensitive applications such as portable systems and notebooks.

This Application Note explains how to compute the R4600 power consumption under different working conditions and capacitive loading.

## TYPES OF POWER

The data sheet of the R4600 lists three different modes of power consumption in the Icc table: Standby mode, Active_Typical mode and Active_Max mode. The R4600 operates in any one of these three modes. The mode of operation of the R4600 is under the system control (both S/W and H/W).

### Standby Mode

The R4600 implements a Standby mode which is entered through software control using the WAIT instruction. Executing the WAIT instruction enables the interrupts and causes the CPU to enter the Standby mode. The Standby mode is actually entered when the WAIT instruction finishes the W stage of the pipeline. In this mode, the internal clocks are shutdown and the pipeline is frozen. No instruction advances through the pipeline and the external bus activity stops. However, the PLL, internal timer, some of the input pins (~Int[5:0], ~NMI, ~ExtReq, ~Reset, ~ColdReset, SyncIn and the MasterClock) and the output clocks (TClock[1:0], RClock[1:0], SyncOut, ModeClock and MasterOut) continue to run. In this mode, the R4600 consumes very little power which is reflected by the standby Icc values in the data sheet.

Once the CPU is in Standby mode, any unmasked interrupt, including the internally generated timer interrupt, will cause the CPU to exit the Standby mode.

### Active_Maximum Mode

In this mode the R4600 is fully functional. The pipeline is continuously running, instructions are advancing through the pipeline and the CPU is accessing the internal caches and the system resources. In this mode, the power to all the internal units may be turned on. This is achieved if the code sequence uses and accesses all the internal units (such as the integer unit, the FPU , etc.) continuously. This mode also represents the worst case power consumption values, with the supply voltage at its max limit (e.g. 5.25V). In this mode, the R4600 consumes its max power and this is reflected by the max Icc values in the data sheet.

### Active_Typical Mode

This mode is similar to the Active_Maximum mode with the exception that the instruction sequence doesn't fully exercise the internal resources (like the FPU for example). The R4600 implements advanced power management techniques to take advantage of such code sequences. In this mode, the unused sections of the device are powered down. For example, if the FPU is not used, it will be powered down to reduce the overall power consumption. This amounts to substantial power consumption savings compared to the maximum case. In this mode, the supply voltage is assumed to be at its mid-point nominal value (e.g. 5V or 3.3V). This mode is reflected by the typical Icc values in the data sheet. It represents the average (typical) power the device will consume in a typical application that is not fully utilizing the internal resources. In such typical applications, the CPU is usually executing instructions 75% of the time and stalled the remaining 25%.

## COMPONENTS OF POWER CONSUMPTION

The total power consumption of the R4600 in the previous three modes includes two components: the internal power consumption and the output power consumption of the device.

The sum of the internal and the output powers is the total power consumption of the R4600. The system designer must calculate these two values for any mode to obtain the total power consumption of the CPU in that mode.

**Note:**

In this Application Note, the power examples assume a system with the following attributes:

- 5V power supply for typical measurement
- 5.25V power supply for max measurement
- MasterClock is 50MHz, the pipeline clock is 100MHz and the SysAd bus operates in the divide by 2 mode (50MHz).
- The examples use the values of Icc published in the March 1994 revision of the R4600 Data Sheet. For the most accurate results, the system designer should use the values published in the most recent revision of the data sheet.

### Internal Power

The internal power is provided in the data sheet. It represents the power consumed by the internal logic of the device. However, it excludes the power consumed by the output buffers, since that is system dependent. Specifically, it depends on the capacitive loading of the output pins and the write pattern supported. The internal power is available in the data sheet and corresponds to the 0 pF loading condition on the output clocks and no SysAD activity. The internal power consumption (IP) is computed using the following equation:

IP = Icc * Voltage (Watts)

For the system example used in this Application Note with a supply voltage of 5V, the Standby internal power consumption is 920mWatts (175mA * 5.25V). Similarly, the Typical internal power consumption is 4375mWatts (875mA * 5V) while the Maximum internal power consumption is 6565mWatts (1250mA * 5.25V).

### Output Power

The output power is the power consumed by the output buffers of the R4600. It is completely system dependent. It is a function of the capacitive loading the output buffer is driving and the frequency of the signal. System designers should use the guideline provided in this Application Note to compute the output power for their particular applications.

The output power per output pin is computed using the following equation:

$OP = C * V^2 * f$ (Watts)

OP is the Output_Power
C is the capacitive loading on the output pin.
V is the supply voltage
f is the frequency (number of low-to-high transitions / sec) of the output pin.

The total output power consumed is the sum of the output power for every individual output pin.

## EXAMPLE OF OUTPUT POWER CALCULATIONS

The R4600 has two classes of output signals. The clock output signals and the bus signals (which include the SysAd and the output control signals). This example shows how to compute the output power for each class. Every calculation has to be done twice: to compute the Typical and the Max output power consumption. Remember that for the Typical power consumption, the power supply is assumed to be at its nominal value (5V in this case) and for the Max power consumption it is assumed to be at its max (5.25V in this case).

### Clocks Output Power

The R4600 has 6 different output clocks: MasterOut, SyncOut, TClock[1:0] and RClock[1:0]. The output power calculation for each clock should be done separately.

*SyncOut.* Typically SyncOut is connected to SyncIn or to a single buffer to match the delay on the TClock and RClock. This is about 20pF of loading. The frequency of SyncOut is the same as MasterClock (50MHz). So the typical output power consumed by the SyncOut clock is:

$OP_{SyncOut} = C * V^2 * f$ (Watts)

$OP\_Typical_{SyncOut} = (20*10^{-12}) * (5)^2 * (50*10^6)$ Watts

$OP\_Typical_{SyncOut}$ = 25 mWatts

The max output power consumed by the SyncOut clock is:

$OP\_Max_{SyncOut} = (20*10^{-12}) * (5.25)^2 * (50*10^6)$ Watts

$OP\_Max_{SyncOut}$ = 27.5 mWatts

*MasterOut.* Typically MasterOut is connected to a couple of loads (mostly to the reset logic). This is about 30pF. The frequency is the same as the MasterClock (50MHz). So the typical output power consumed by the MasterOut clock is:

$OP\_Typical_{MasterOut} = (30*10^{-12}) * (5)^2 * (50*10^6)$ Watts

$OP\_Typical_{MasterOut}$ = 37.5 mWatts

The max output power consumed by the MasterOut clock is:

$OP\_Max_{MasterOut} = (30*10^{-12}) * (5.25)^2 * (50*10^6)$ Watts

$OP\_Max_{MasterOut}$ = 41.3 mWatts

*TClock[1:0] and RClock[1:0].* Typically TClock[1:0] and RCLock[1:0] are connected to several loads; for this example assume that they add up to about 50pF. The frequency of TClock[1:0] and RClock[1:0] ($f_{TRClock}$) depends on the bus_clock_divisor which is selected at boot time (from 2 to 8). It is calculated using the following equation:

$$f_{TRClock} = \frac{MasterClock * 2}{bus\_clock\_divisor} \quad (MHz)$$

The bus_clock_divisor in this example is set to 2. The $f_{TRClock}$ is then:

$$f_{TRClock} = \frac{(50*10^6) * 2}{2} \quad MHz = 50\ MHz$$

There are 4 clocks (two TClocks and two RClocks). So the typical output power consumed by the TClocks and RClocks in this example is:

$OP\_Typical_{TRClock} = 4 * (50*10^{-12}) * (5)^2 * (50*10^6)$ Watts

$OP\_Typical_{TRClock}$ = 250 mWatts

The max output power consumed by the TClocks and the RClocks is:

$OP\_Max_{TRClock} = 4 * (50*10^{-12}) * (5.25)^2 * (50*10^6)$

$OP\_Max_{TRClock} = 275.5$ mWatts

The typical total output power consumed by the clocks is the sum of the typical output power consumed by the individual clocks:

$OP\_Typical_{Clock} = OP\_Typical_{SyncOut} + OP\_Typical_{MasterOut} + OP\_Typical_{TRClock}$

$OP\_Typical_{Clock} = 25 + 37.5 + 250 = 312.5$ mWatts

Similarly, the max total output power consumed by the clocks is the sum of the max output power consumed by the individual clocks:

$OP\_Max_{Clock} = OP\_Max_{SyncOut} + OP\_Max_{MasterOut} + OP\_Max_{TRClock}$

$OP\_Max_{Clock} = 27.5 + 41.3 + 275.5 = 344.3$ mWatts

Of course, the system designer should determine the power estimate for any given system, factoring in the loading, the clock frequency and the supply voltage.

**Bus Output Power**

The R4600 bus transactions consist of main memory accesses (read and write operations). The output power consumed by the bus signals differs from one transaction to the other. Read and block read transactions represent the best case since the R4600 consumes output power only during the address phase of the transaction. During the data phase, the system returns the data to the CPU and the R4600 doesn't consume much output power. The output power consumed in the read transactions can be obtained by computing the power consumed during the address phase of the bus. This case will not be demonstrated in this example; since in a typical system, the power contribution of the read transactions is negligible.

On the other hand, the write transactions tend to consume much more output power because the R4600 is continuously driving the bus with either the address or the data. The worst case output power consumption by the bus unit is when the R4600 does a stream of uncached write transactions or write -through stores when the address is the complement of the data. It also assumes that all the SysAd and the SysCmd bits need to toggle. This case represents the max output power consumed by the bus. The example in this Application Note will concentrate on this situation.

Further, there are two major cases to consider when calculating the bus max output power consumption during write transactions. The first is the R4xxx compatible bus write protocol and the second is the write-reissue or the pipelined write bus protocols.

Before starting the calculations of the bus output power consumption during the write transactions, a generic formula to compute the average SysAd_Data_Frequency ($f_{SysAd\_Data}$) is needed. This is the frequency that is used in the Output_Power equation. The average $f_{SysAd\_Data}$ is computed as follows:

$$f_{SysAd\_Data} = \frac{1}{2} * \frac{MasterClock * 2}{bus\_clock\_divisor} * \frac{n}{m} \text{ (MHz)}$$

MasterClock * 2 is the frequency of the output bus_clock_divisor clocks (TClock and RClock).

n is the number of transitions on the SysAd bus

m is the total number of bus clock cycles to complete a write transaction

1/2 The output clock frequency is divided in half because the max transitions on the SysAd bus are at half the output clock frequency.

*R4xxx compatible write protocol*. In this mode, the R4600 performs an uncached write transaction every 4 SysAD cycles (the actual pattern is ADxx). The number of transitions "n" is 2 and the total number of clock cycles "m" is 4 in this case. The bus frequency in the case of a bus_clock_divisor equals to 2 is:

$$f_{Compatible} = \frac{1}{2} * \frac{(50*10^6) * 2}{2} * \frac{2}{4} = 12.5 \text{ MHz}$$

There is a total of 81 output signals used during the write transactions (64 SysAD outputs, 8 SysADC outputs and 9 SysCmd outputs). There is also ~ValidOut which should toggle once in this case. However, for simplicity reasons it will not be part of the calculations. On the other hand, all the SysCmd bits are assumed to toggle which might not be the case. Assume a 50pF load on each. Then the max output power consumed by the bus in the R4xxx compatible mode is:

$OP\_Max_{BusCompatible} = 81*(50*10^{-12})*(5.25)^2*(12.5*10^6)$ Watts

$OP\_Max_{BusCompatible} = 1395.5$ mWatts

*Write reissue and pipelined write protocols*. In these modes, the R4600 performs an uncached write transaction every 2 SysAD cycles (the actual pattern is AD). The number of transitions "n" is 2 and the total number of clock cycles "m" is 2 in this case. The bus frequency in the case of a bus_clock_divisor equals to 2 is:

$$f_{Pipelined} = \frac{1}{2} * \frac{(50*10^6) * 2}{2} * \frac{2}{2} = 25 \text{ MHz}$$

There is a total of 81 output signals used during the write transactions (64 SysAD outputs, 8 SysADC outputs and 9 SysCmd outputs). ~ValidOut will not toggle in this mode and

is not counted. Assume a 50 pF load on each. Then the max output power consumed by the bus in the write reissue or the pipelined write modes is:

$OP\_Max_{BusPipelined} = 81 * (50*10^{-12}) * (5.25)^2 * (25*10^6)$ Watts

$OP_Max_{BusPipelined} = 2790$mWatts

*Typical-case bus output power*. In a more typical system, the bus output power consumption of the R4600 is much less than the worst case numbers. In normal operation, the R4600 performs primarily block write transactions. In this case, the non-block write transactions are a small percentage of the total bus activity and the output power consumed during non-block write transactions is irrelevant. The block write transactions represent the typical output power consumed by the bus.

The statistics from standard benchmarks indicate that a typical application, executing from the internal caches, requires the R4600 to perform a block write transaction every "l" processor cycles on the average. A processor cycle is executing at the speed of the internal pipeline (MasterClock * 2). The value of "l" is independent from the write back pattern in the block write transaction (because it is always 5 transitions no matter what). The total number of clock cycles to complete the transaction "m" is then actually equals to "l" divided by the bus_clock_divisor as stated in the following equation:

$$m = \frac{l}{bus\_clock\_divisor} \text{ (clock cycles)}$$

The number of transitions in a block write transaction "n" is 5 (address and 4 double words of data). In this case the frequency of the bus ($f_{BusTypical}$) in the case of a bus_clock_divisor equals to 2 and a value of "l" equals to 200 (for example) is:

$$f_{BusTypical} = \frac{1}{2} * \frac{(50*10^6) * 2}{2} * \frac{5}{(200 / 2)} = 1.25 \text{ MHz}$$

There is a total of 81 output signals used during the write transactions (64 SysAD outputs, 8 SysADC outputs and 9 SysCmd outputs). There is also ~ValidOut which might toggle or not depending on the write-back pattern selected. In this case, with a write back pattern of ADDDD, the ~ValidOut signal doesn't toggle and will not be counted. Assume a 50 pF load on each. Then the typical output power consumed by the bus during a typical write back mode (when all outputs switch) is:

$OP\_Typical_{BusTypical} = 81 * (50*10^{-12}) * (5)^2 * (1.25*10^6)$ Watts

$OP\_Typical_{BusTypical} = 126.5$ mWatts

The typical total output power consumed by the R4600 is the sum of the clocks typical output power and the bus typical output power. Similarly, the max output power consumed is the sum of the max clock output power and the max bus output power consumptions. The max output power consumption depends on the bus write protocol (R4xxx compatible or write reissue or pipelined write transactions). The typical output power consumption doesn't depend on the write protocol or the write back pattern.

## TOTAL POWER CONSUMPTION

The total power consumption of the R4600 is then the sum of the internal power and the output power consumptions. It depends on the system design in terms of the loading on the bus as well as on the application S/W and the mode of operation of the R4600. The system designers should compute the output power consumption for their particular application to obtain the total power consumption of the device. The Total Power (TP) is expressed in the following equation:

TP = IP + OP (Watts)

To finish the example started in this Application Note, the total typical power consumed by the R4600 in the system described is:

$TP\_Typical_{R4600} = IP\_Typical_{R4600} + OP\_Typical_{R4600}$ Watts

$TP\_Typical_{R4600} = 4375 + [126.5 + (25 + 37.5 + 250)]$ Watts

$TP\_Typical_{R4600} = 4814$ mWatts

Similarly, the total max power consumed by the R4600 in the system described using the R4xxx compatible write mode is:

$TP\_Max_{R4600} = IP\_Max_{R4600} + OP\_Max_{R4600}$ Watts

$TP\_Max_{R4600} = 6565 + [1395.9 + (27.5 + 41.3 + 275.5)]$ Watts

$TP\_Typical_{R4600} \approx 8305$ mWatts

## CORRELATION WITH THE DATA SHEET

The power consumption of the R4600 is listed in the data sheet in the Icc Table. There are several columns in the table that correspond to the internal pipeline frequency and to the external bus frequency (100/50MHz column as an example). For every column, the typical and the max current consumption is listed for the Standby mode and for the Active modes. The 0pF loading with no SysAd activity condition represents the internal power consumption of the device.

The 50pF loading condition in the Standby mode corresponds to the max power consumed in this mode with the active clocks loaded with 50pF. Remember that in this mode only a few external clock signals are active.

The 50pF loading condition for the Active mode for both the Typical and the Max case is the total power consumption of the device. These values are derived using the equations intro-

duced in this Application Note. However, the loading on the bus is different. The clocks are assumed to be driving a load of 50pF. This is substantially more than the 20 or 30pF assumed for SyncOut and MasterOut in this Application Note. Similarly, the R4xxx compatible mode and the pipelined or write reissue mode assume the number of output signals toggling to be 81. The ~ValidOut signal is not part of the calculations. The loading on every output pin is assumed to be 50pF. There is also a small added guard band in the published numbers.

System designers can use the values provided in the data sheet as a max upper limit for the possible power consumption of the R4600 under the mentioned conditions. However, it is always recommended for the system designers to compute the exact power consumption of their particular application. The values they obtain will be much more accurate than the upper limit presented in the data sheet, which reflect the worst case assumptions used during device testing.

## CONCLUSION

The R4600 is designed from the ground-up to consume as little power as possible while achieving very high performance. It incorporates advanced power management techniques to turn off the power from the unused units of the device. This reduces the typical power consumed compared to other microprocessor in its class. On the other hand, the R4600 doesn't sacrifice performance for the reduction in the power consumed. Several systems have shown the R4600 to outperform the R4400PC by at least 30% at a given frequency.

This Application Note explains how to compute the output power consumed for every situation and how to derive the total power of the CPU under different system conditions. The system designer should use it as a reference and a guideline in computing the power consumption for their particular application. In addition, the system designer can use this information to make power consumption trade-offs during system design.

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(Disclaimer Rev.1.01 Jan 2024)


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